Article

Contribution to the Physical Modelling of Single Charged Defects Causing the Random Telegraph Noise in Junctionless FinFET

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Abstract: In this paper, different physical models of single trap defects are considered, which are localized in the oxide layer or at the oxide–semiconductor interface of field effect transistors. The influence of these defects with different sizes and shapes on the amplitude of the random telegraph noise (RTN) in Junctionless Fin Field Effect Transistor (FinFET) is modelled and simulated. The RTN amplitude dependence on the number of single charges trapped in a single defect is modelled and simulated too. It is found out that the RTN amplitude in the Junctionless FinFET does not depend on the shape, nor on the size of the single defect area. However, the RTN amplitude in the subthreshold region does considerably depend on the number of single charges trapped in the defect.

Keywords: single defect; random telegraph noise; Junctionless FinFET; oxide layer; oxide–semiconductor interface

1. Introduction

Decreasing the critical metal-oxide-semiconductor field effect transistor (MOSFET) dimensions up to the nanometer-scale induces the increasing of the defect influence on carrier mobility, subthreshold swing, and threshold voltage. It also stimulates both instability and degradation of the transistor in active mode. Depending on certain conditions and the type of measurements, the instability may be responsible for bias temperature instability (BTI), random telegraph noise (RTN), and a hysteresis of characteristics [1]. Especially amongst these effects, a single interface or oxide defect on the drain current can be noticed. These single charged traps can induce instability in the operation of the transistor [2], generate RTN in the MOSFET and affect both stability and reliability of MOSFET-based circuits [3,4]. On the other hand, RTN can be used as a tool for analyzing and exploring the defect behavior of the oxide–semiconductor interface of the MOSFET [5,6].

Therefore, it is very important to investigate a single interface or the influence of an oxide charged trap on the characteristics of the MOSFET. One of the reliable simulation methods for studying such defects is the so-called atomistic approach [7]. However, this technique requires a magnificent effort in computation (in terms of time and memory), particularly while simulating integrated circuits on a MOSFET basis. Therefore, the development of a simple physical model of the single-trapped charge

useable in commercial widely used Technology Computer Added Design (TCAD) programs is an important task from the point of view of significantly reducing the computational time required for these types of simulation studies. The model should properly describe the processes related to the trapped charge influence on the charge transfer processes in these devices. The TCAD Sentaurus provides the opportunity of simulating the charge trapping in the oxide layer or at the interface in MOSFET (model of traps and fixed charges). However, to fully describe the trapped charge, a clear specification of both the boundary conditions and the density of charge is required. In the literature, usually, the single trapped charge is modeled as simple cell with appropriate boundary conditions [2,8]. However, there is no experimental research work indicating clear criteria for defining appropriate and specific sizes of the cell describing the single trapped charge. The sizes presented in various works differ by several orders of magnitude. Besides, to the best of our knowledge, no research has been carried out addressing the dependency and correlation between the single charge effect, the size and shape of the charged area. Therefore, in this work, the effect of a simple cell model is compared with other proposed models of single trapped charge with appropriate (i.e., using suitable) boundary conditions. The single trapped charge effect/ dependency on the size of the charged area are estimated. One of the important effects of the single trapped charge is generation of the Random Telegraph Noise. Therefore, the RTN amplitude dependency on the size and shape of the charged area is considered.

The influence of a single trapped charge on the noise characteristics has been widely investigated for the planar MOSFETs [9–12] and FinFETs [13,14], while very few works were devoted to investigating the RTN amplitude in the relatively new Junctionless FinFET [15,16]. Thus, the influence of both shape and size of the single trapped charge to noise characteristics of nanometer Junctionless FinFET is closely studied in this paper.

2. Modeling and Simulation Procedure

Nowadays, there is no universal physical model that describes the spatial distribution and sizes of the single charge trapped at the interface or in the oxide defects in a MOSFET. Moreover, it is very interesting to implement these models in commercial TCAD programs. There are many geometrical sizes, which describe spatial sizes of an elementary component of solid states such as the Bohr radius, Van der Vaals radius or atomic radius. All of the above might be used as a size-related single defect physical model.

We consider that the trap defect at the Si-SiO_2 interface or in the oxide is a broken connection between silicon atoms (or between silicon and oxygen atoms). In general, hydrogen atoms are introduced to recover the dangling bonds. However, because it (i.e., the recovery) is a statistical process, some broken bonds may not be recovered by hydrogen atoms. This case is very important in nanometer devices because the charged trap will have a significant impact on the device characteristics.

In some cases, the trap in oxide may be represented by a vacancy V^0, which can capture carrier according to the reaction

$$V^0 + e^- = > V^- \tag{1}$$

where e^- and V^- denote the elementary charge and charged vacancy, respectively. Hence, the defect will represent a local charged area with some spatial shape. It is expected that the single trapped charge will be distributed in that local area. It can be assumed that the sizes of this area will be restricted by atomic sizes as well as by interatomic distances inherent to the considered materials. Interatomic distances at the interface, as well as in bulk, vary depending on defect's position and layer's thickness. Thus, the distance between silicon and oxygen atoms $R_{Si\text{-}O}$ varies in the range from 0.154 nm to 0.162 nm, and the distance between neighboring oxygen atoms $R_{O\text{-}O}$ ranges between 0.248 and 0.265 nm at changing SiO_2 thickness from 0.4 nm to bulk [17] (Figure 1). However, in [18], it is stated that $R_{O\text{-}O}$ is equal to 0.227 nm, and the average distance between silicon and oxygen atoms is equal to 0.162 nm in SiO_2. Further, it is indicated that the distance between silicon atoms $R_{Si\text{-}Si}$ is equal 0.543 in crystal silicon and the atomic radius for silicon R_{Si} and for oxygen R_O ranges between 0.118 and 0.065 nm correspondingly. At the transition layer from Si to bulk SiO_2, the ratio of the number

of silicon and oxygen atoms is changed depending on the position. Therefore, the atomic distances indicated above, and, as a consequence, the interface defect sizes, can change in some range.

When decreasing the transistor dimensions to decrease the tunneling current through the gate oxide, HfO_2 with a high dielectric constant and the appropriate equivalent thickness is mainly used instead of SiO_2. Therefore, it is also interesting to notice the characteristic interatomic distances in this material. Depending on orientation and number of atomic layers from 3 to 11, the distances between oxygen atoms vary from 0.254 up to 0.265 nm. In addition, the distances between Hf and oxygen atoms vary from 0.202 nm up to 0.248 nm [19] (see Figure 2). In the transition layer Si-HfO_2, the average distance between Si and Hf atoms is 0.260 nm [20]. In this transition layer, the break of the connections between silicon atoms as well as the oxygen vacancies is responsible for the arising of the interface defects [21]. Due to the facts indicated above, it is obvious that the interatomic distances and, as a consequence, the trap defect linear sizes are in accordance with the ranges indicated above. In some papers, the trap sizes are considered in the electron (or hole) capture cross-section point of view. For the considered materials, often, the range of the capture cross sections is taken from 10^{-18} up to 10^{-13} cm^2 [22–24]. This range of the cross section fits to the range of the linear sizes of defects from 1.8 nm up to 0.005 nm and it covers the range of possible defect sizes indicated above. It can be summarized that for the substrate and oxide materials used for MOSFET, the typical atomic linear sizes and interatomic distances are in the range between 0.05 and 0.55 nm.

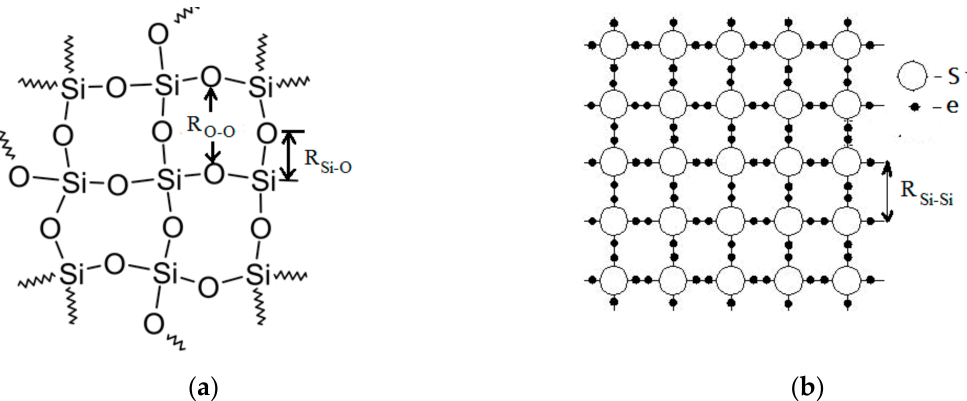


Figure 1. Model of the crystal lattices of (**a**) SiO_2 and (**b**) Si.

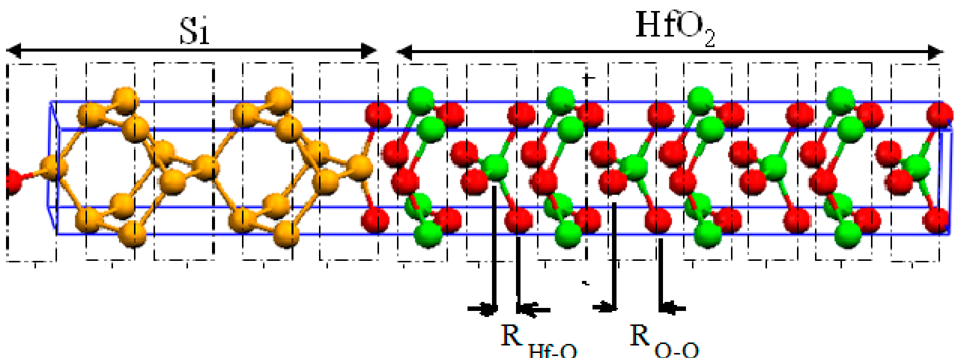


Figure 2. Model of the Si-HfO_2 structure.

However, these above described sizes do not allow for arguing the defect's shape and/or assessing the spatial distribution of single trapped charge in the defect. The spatial distribution of the single charge in the trap is described by the wave function of the carrier in the defect. The wave function depends on the excitation condition of the defect. Obviously, in the basic non-excited state, the charge distribution can be modeled by a simple homogeneously charged sphere with the center allocated in the defect's center (see Figure 3, form (a)). For comparison, the idealized forms of the charge

distribution, which would be appropriate to the wave function of the excited condition, are considered too (Figure 3, forms (b) and (c)). In many papers studying the influence of a single charged trap on the characteristics of the MOSFET, the charged area is considered as a homogeneously charged simple cell [3,8]. Therefore, for comparison, besides the forms indicated above, the single defect model in the form of a simple cell is also considered (see Figure 3, form (d)).

Our analysis is mainly based on the McWhorter model of RTN and we have considered only the steady state, but not dynamic features [25–27]. We have considered the influence of the size and shape of the defect area on the amplitude of the RTN in a Junctionless MOSFET. For this purpose, the RTN amplitude dependence on the gate voltage overload ($V_g - V_{th}$) is simulated by trapping the single defect with different sizes and forms at the interface, as well as in the oxide layer.

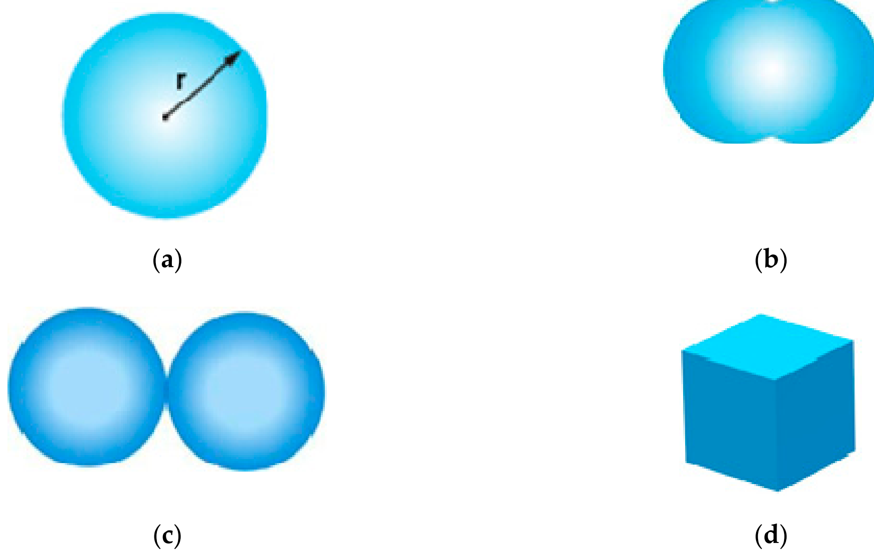


Figure 3. Models of a single charged defect with different forms of charge distribution. (**a**) is form of defect in basic state; (**b**,**c**) are forms of defect in excited state; (**d**) is simple cell form of the defect.

The spherical model of a single trapped charge is considered for the first time. It is therefore necessary to check whether this model is appropriate. In this context, we first compared the RTN simulation results induced by this model with the experimental results of a classic planar MOSFET, which were discussed in detail in [27]. The proposed physical model of the defect, and the transport model for the RTN simulation, are all calibrated by using experimental results. To calibrate the models, one considers the planar MOSFET structure with the same parameters as for the experimental sample [27], and for the model of the single defects, a sphere with radius r = 0.13 nm homogeneously charged by elementary charge (see Figure 3, form (a)) is used. Experiments carried out in [27] utilize silicon oxynitride (SiON) *n*-channel MOSFET devices with a physical dielectric thickness of 1.4 nm. The nominal channel widths are in the range 0.085 μm to 1 μm and the nominal channel lengths are between 0.055 μm and 1 μm. A full description of the RTN measurement apparatus and methods can be found in [27]. Indeed, source and gate electrodes are biased using battery-powered variable-voltage sources, while the substrate electrode is grounded for all measurements. The drain current is monitored by a low-noise current amplifier with 2 kHz bandwidth. The amplifier output is directly captured using a digital storage oscilloscope with a large memory depth (10^7 Samples). The experimental measurements (obtained in the form of time series data) are further analyzed offline. The parameters of the simulated transistor are shown in Table 1. In the simulation, SiON is used for gate oxide; the same is done in the experimental sample.

Table 1. The parameters of the simulated MOSFET.

Parameters	Designation	Value of the Parameters
The channel doping concentration	N_{ch}	2×10^{16} cm^{-3}
Gate oxide thickness	t_{ox}	1.4 nm
Gate width	W_{gate}	90, 130 nm
Gate length	L_{gate}	55 nm

The simulation and experimental results for a MOSFET with widths 90 and 130 nm are shown and compared in Figure 4. Regarding the RTN amplitude, it is seen that the simulation values are sufficiently close to the experimental ones when the gate overload lies in the range between −0.15 and 0.1 V for both gate widths. The RTN amplitude differences observed between simulation and experimental results outside of the previously specified range, obviously, are due to fluctuations in the experimental samples' parameters responsible for the drain current. This is confirmed by the significant differences observed in the RTN amplitude for two different experimental samples outside of the indicated range: the jumping increase is observed for the positive gate overload higher than 0.1 V for the sample with width 130 nm, and for the negative gate overload lower than 0.15 V for the sample with a width of 90 nm.

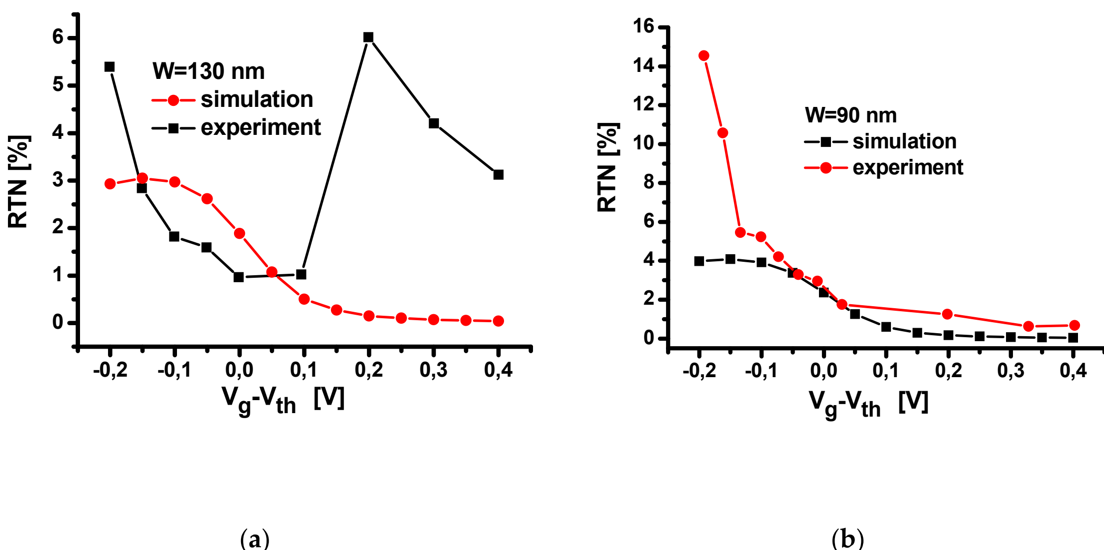
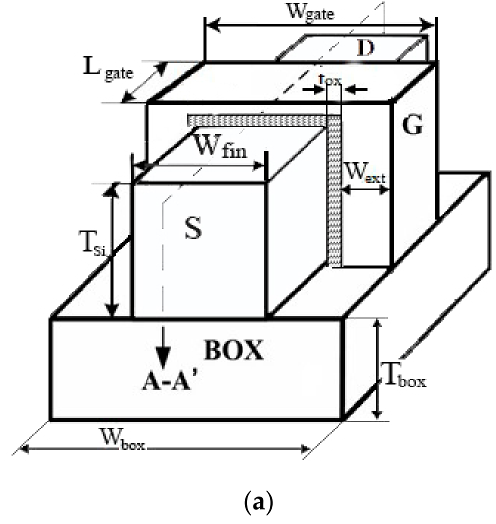


Figure 4. RTN amplitude dependence on the gate overload for the planar MOSFET with gate widths 130 (**a**) and 90 (**b**) nm.

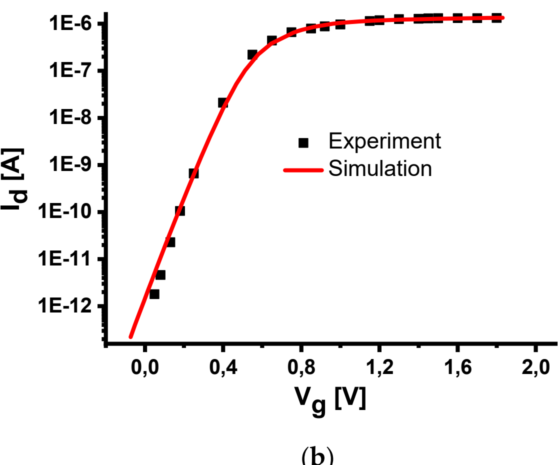
Reasonable agreement with the experimental results enables the use of this model in Junctionless FinFET and comparison with various other models, especially the conventional simple cell model. The proposed defect model was applied for simulating the RTN amplitude generated by single charges trapped at the oxide–semiconductor interface, as well as in the gate oxide layer of nanosized Junctionless (JL) Silicon on Insulator (SOI) FinFET. The RTN amplitude was calculated in steady state condition using the following expression

$$RTN = (|I_{d0} - I_d|)/I_{d0} \quad (2)$$

where I_{d0} and I_d denote the drain current before and after trapping the single charge, respectively. The structure of the simulated transistor is shown in Figure 5a and the corresponding parameters are presented in Table 2.



(a)



(b)

Figure 5. The structure of the simulated JL MOSFET (**a**) and comparison of I_d–V_g characteristics of the transistor carried out from simulation and experiment (**b**).

Table 2. Parameters of the simulated SOI FinFET.

Parameters	Designation	Value of the Parameters
The channel doping concentration	N_{ch}	5×10^{18} cm^{-3}
Equivalent gate oxide thickness (HfO_2)	t_{eff}	1.2 nm
Channel thickness	Ts_i	9 nm
Channel width	W_{fin}	22 nm
Gate width	W_{gate}	55 nm
Gate length	L_{gate}	13 nm

3D simulations were performed in the framework by a drift-diffusion model using the TCAD Sentaurus software. The influence of trapped charge in this model is accounted by trapped charge density ρ_{trap} in the Poisson equation, which is part of the transport model used [28]:

$$\nabla\varepsilon\nabla\varphi = -\,q(p - n + N_D - N_A\,) - \rho_{ytap} \tag{3}$$

where ε is the electrical permittivity, q is the elementary electronic charge, n and p are the electron and hole densities, N_D is the concentration of ionized donors, N_A is the concentration of ionized acceptors. Boundary conditions for ρ_{trap} are determined by the form of charged defect (Figure 3). In Sentaurus,

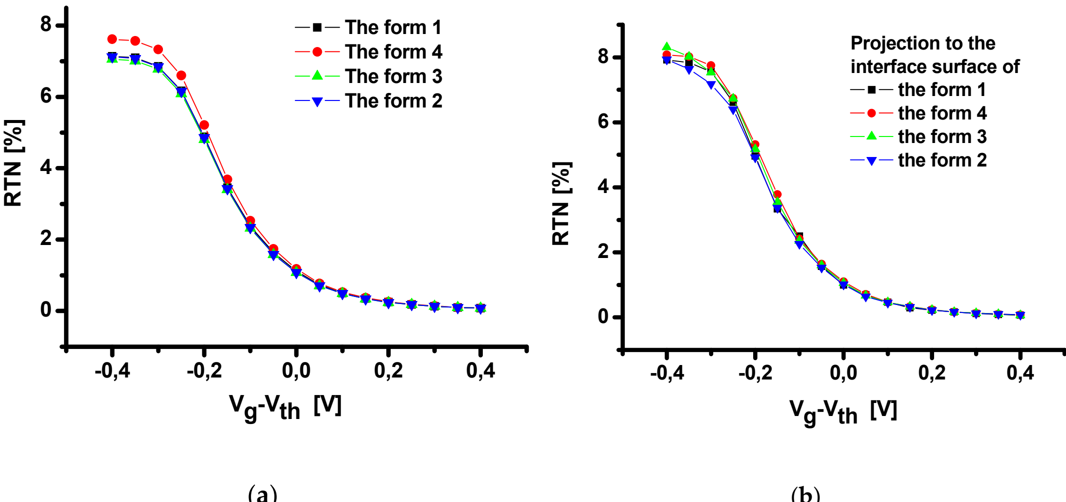
an area with a certain shape, size, and boundary was created in the oxide layer and at the boundary using the Sentaurus Structure Editor, which corresponds to the different single trapped charge models at stake (i.e., under consideration). In the "Physics" section of the Sentaurus Device, the parameters of a charge trap were defined for various models at stake (i.e., under consideration). The used transport model considered the influence of the doping level on the carrier mobility, the saturation of carrier velocity, and the influence of the normal field component on the drain current. Since the transistor had nanoscale dimensions, it was also necessary to take into account the quantum confinement effects. The present work employed quantum corrections with respect to the density gradient, which is preferred in the framework of drift-diffusion simulations [29,30]. The adopted transport model has been calibrated on experimental I_d–V_g characteristics carried out in [31]. The experimental transistor preparation and measurements details are described in [31]. According to this work, [110]-trigate nanowires with high-κ/metal gate stack were fabricated on (100) SOI wafers with a 12 nm top silicon layer and a buried oxide thickness of 145 nm. The SOI layer was thinned down to 10 nm. The silicon layer is patterned to create nanowires by using a mesa isolation technique. The gate stack consists of 2.3 nm CVD HfSiON, 5 nm ALD TiN, and polysilicon (50 nm) layers (equivalent oxide thickness (EOT) ≈ 1.2 nm). As for the active patterning, photoresist trimming is used to address gate lengths up to 13 nm.

The comparison of I_d–V_g characteristics obtained from both simulation and experiment is shown in Figure 5b. A good calibration between simulation and experimental characteristics in the subthreshold as well as in the superthreshold regions was obtained. Hereby, the trap at the interface of the defect area is modeled by the projection of the spatial defect to the interface surface with an appropriate density of charge.

For an adequate comparison of the effect of different defect forms, the volume of different spatial defect forms as well as the area of different forms of interface defects were correspondingly chosen to be equal. The radius of the spherical model of the defect in the oxide layer and that of the circle model at the interface surface were chosen to equal 0.15 nm.

3. Simulation Results and Discussions

The simulation results of the RTN amplitude dependence on gate voltage at single charge trapping in the oxide layer and at the interface are shown in Figure 6. It is seen that for both single oxide and interface defects, the RTN amplitude dependence on the gate voltage overload is not influenced by the considered form of the single defect. Figure 6 also indicates that a single defect trap in the oxide layer can be modeled by a homogeneously charged sphere (or circle at the interface) or by a simple cell.



(**a**) (**b**)

Figure 6. Random telegraph noise (RTN) amplitude dependence on the gate voltage overload generated by single charged defect with different forms: in the oxide layer (**a**) and at the interface (**b**).

The RTN amplitude dependence on the radius of spherical or circular area of defects in the oxide or at the interface, correspondingly, was simulated to study the influence of the defect size.

One has considered the radius range between 0.1 and 0.5 nm, which covers practically all featured linear sizes of atomic radius and interatomic distances in Si, SiO_2, and HfO_2. When changing the radius only, the charge density is modified because the trapped charge remains single and elementary. The results show that the RTN amplitude depends linearly, but very weakly, on the radius of the defect and practically does not change in the radius range under consideration (see Figure 7). When increasing the radius of the defect area, at a constant trapped charge, the RTN amplitude is practically not changed in all considered ranges of the gate voltage overload. The RTN amplitude in the subthreshold region is not as high as it is reported in some experimental works [14,25]. To find out a possible reason for creating the large RTN amplitudes in the subthreshold region, as observed in our experiments, we have studied the RTN amplitude dependence on single charge quantity in the spherical defect area at the constant radius 0.15 nm. We considered the repeatedly charged defect with constant size. In this case, the RTN is appreciably changed in the subthreshold as well as in the near-threshold region (see Figures 8 and 9a). The RTN amplitude in the subthreshold region is considerably increased when increasing the number of single charges N in the defect (see Figure 9b). Obviously, the main reason for creating the high RTN amplitude is not the size as well as the shape of the defects but the density or the number of trapped charges in the defect.

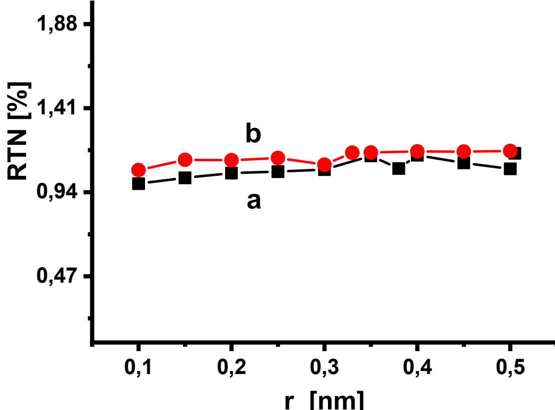


Figure 7. RTN amplitude dependence on the radius of (**a**) the oxide, and (**b**) the interface single charged defects at a constant trapped charge.

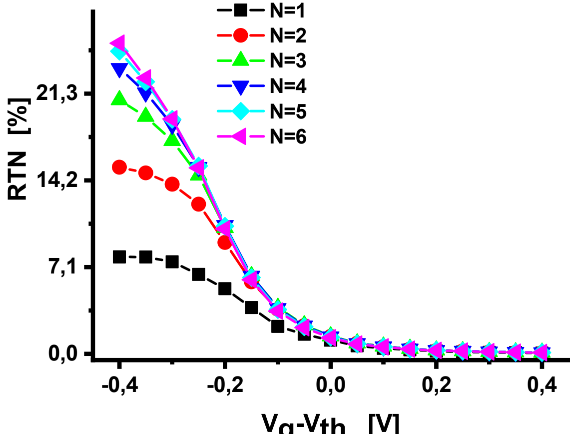
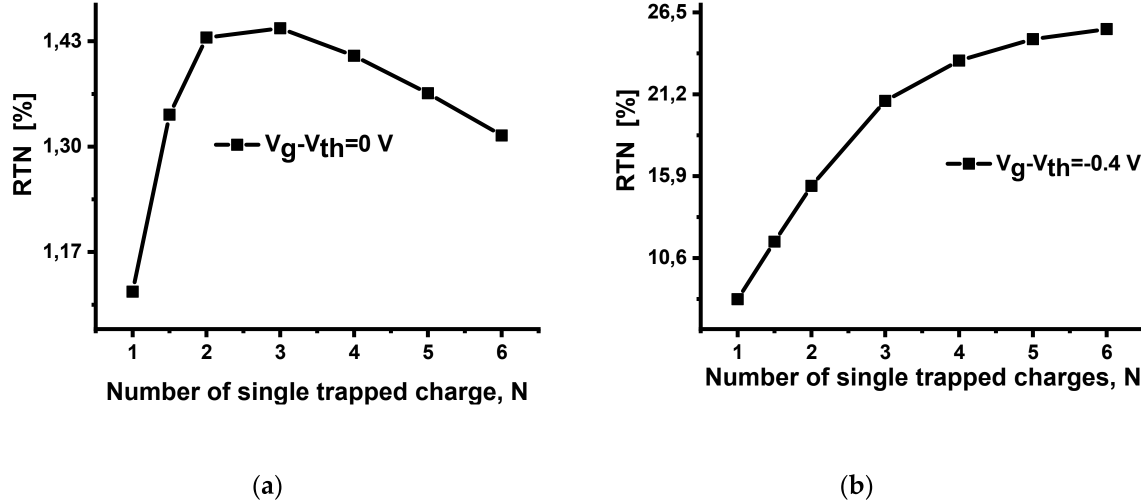


Figure 8. RTN amplitude dependence on the gate overload for different numbers of the single charges trapped N in the defect area.



(**a**) (**b**)

Figure 9. RTN amplitude dependence on the number of the single charge trapped in the defect area at gate overload 0 V (**a**) and −0.4 V (**b**).

4. Conclusions

We have found out that the RTN amplitude in a Junctionless FinFET does not actually depend on the single charge spatial distribution in the defect. A simplified simulation of the single trap can be modeled by the homogeneously charged simple cells in both the oxide and interface trap cases. Moreover, the RTN amplitude does not practically depend on the linear size of the charged area in the range from 0.1 up to 0.5 nm. However, the RTN amplitude is considerably increased with the increasing number of single charges trapped in the defect. In particular, a high amplitude is created at the subthreshold region, depending on the number of the trapped charge.

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