

Article

# A Hierarchical Coordinative Control Strategy for Solid State Transformer Based DC Microgrids

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Received: 31 August 2020; Accepted: 26 September 2020; Published: 29 September 2020



**Featured Application:** A solid state transformer (SST) is expected to serve as an energy router in the Energy Internet, so as to realize a large-scale utilization and coordinately optimized scheduling of renewable power sources. This paper improves the topology of SSTs, solving the problems of high cost and low energy transmission efficiency, to a certain extent. The hierarchical coordinative control strategy proposed in this paper improves the voltage stability problem of SST ports caused by the frequent fluctuation of renewable power output, which makes the practical application of SSTs in distribution networks possible.

**Abstract:** A solid state transformer (SST), as a kind of energy router in the Energy Internet, provides a unified access point for AC or DC distributed power subjects. However, the DC-link capacitors inside the SST will suffer huge voltage fluctuations when the output power of the microgrid changes dramatically. With respect to this problem, caused by the random and intermittent characteristics of distributed generation (DG), a hierarchical coordinative control strategy is proposed. Compared with the common independent control, the proposed method not only makes full use of the regulation capacity of super capacitors, but also enhances the dynamic power tracking speed and reduces the speed difference between different stages of an SST. The dynamic voltage response under the proposed method is analyzed in frequency domain and compared with the independent control. To validate the effectiveness of the coordinative control strategy, a simulation model of an SST-based grid-connected DC microgrid system is established, and the topology of the SST is improved. The voltage stability of the DC bus is compared under different control strategies, and the coordinative control strategy is also verified, effectively under transition conditions.

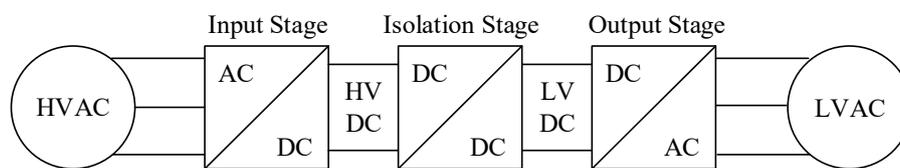
**Keywords:** microgrid; solid state transformer (SST); voltage stability; hierarchical coordinative control strategy

## 1. Introduction

The microgrid, as an economical and efficient form of electric energy organization, has attracted worldwide attention [1,2]. A solid state transformer (SST) can serve as a kind of energy router in microgrids [3], which not only coordinates the energy transmission between the utility grid and the microgrid, but also controls the interaction between the AC and DC microgrids. Compared with the traditional transformer, the multi-stage SST provides a direct interface to the DC microgrid, and the energy density can be improved through a high frequency transformer (HFT). The SST is expected as a crucial equipment for utilization of distributed generations (DGs) [4] and construction of the Energy Internet [5,6].

The multi-stage SST commonly contains three stages: input stage, isolation stage, and output stage, as shown in Figure 1. The input stage mainly adopts a modular multilevel converter (MMC)

and a cascaded H-bridge (CHB) [7]. A dual active bridge (DAB) converter is often employed as the isolation stage. At present, the main factors affecting the practical application of SSTs are low-energy transmission efficiency and high cost. The efficiency of an SST can reach 93.72% with a CHB-type input stage [8], which is relatively low for practical application. However, the required number of power electronic switches and high-frequency transformers can be reduced by using an MMC as the input stage, which can significantly reduce the switching losses of power transistors and the cost of the SST [9] as well. Under the voltage level of the distribution network, power loss of the SST isolation stage is usually much higher than that of the input stage. Before extensive commercial use of power devices such as SiC and GaN, CLLC resonant converters can effectively solve for the inherent inefficiency of the DAB converter, whose conversion efficiency exceeds 96% [10]. In [11], a 5 kV CLLC resonant converter prototype was built and its efficiency reached 97%. In this paper, the efficiency of the CLLC resonant converter can reach beyond 98% at the rated power.



**Figure 1.** Structure of a three-stage solid state transformer.

Due to the randomness and intermittence of DGs, the power flow direction of an SST will change frequently, and the voltage across the port of each stage will suffer fluctuation, flicker, sag, and interruption [12], which brings serious damage to electric motors and, precisely, operated power electronic instruments and other power equipment [13,14]. Integration of DGs requires a comprehensive control of the SST. As for the multi-stage SST, traditional control at each stage is independent: the input stage is responsible for the voltage stability of the high-voltage DC (HVDC) bus, and the isolation stage is responsible for the voltage stability of the low-voltage DC (LVDC) bus [15–18]. In [15], an all-SiC device-based multistage SST was established, where the input stage of the SST adopted a front-end converter (FEC) and the isolation stage was with a DAB. The HVDC bus voltage and LVDC bus voltage were set as the control target of FEC and DAB, respectively. The control strategies of FEC and DAB do not interact with each other, which lacks collaborative operation between them. A global system control structure is described in [16], which can handle the different power flow directions and DC voltage unbalance using battery energy storage. The global control strategy is based on independent control strategy, and DC voltage fluctuation can be suppressed with assistance of the battery contribution, but it may increase the investment. In [17], a SiC-based multiple active bridge was chosen as the isolation stage of the SST to reduce the number of power devices, and a first order approximation-based mathematical model was analyzed, which helped to simplify a voltage balance controller design. The balance control of submodule DC voltage was also researched in [18] to solve the problem of unbalanced submodule voltage after using multilevel converter modules. The addressed control strategy focused on the input stage of the SST without collaboration among different stages. However, such independent control strategy ignores the inherent differences in the power response speed between different stages, which is prone to cause power difference on both sides of the DC-link capacitors and exacerbate the DC voltage fluctuation. Many efforts have been made to solve this problem. A coordinated control strategy is put forward in [19], to reduce the voltage fluctuations of the LVDC bus, that combines the isolation stage and the output stage. However, it focuses on the dual active bridge cascaded with an inverter (DABCI), which does not consider the input stage in a complete SST. The coordinated control in three stages of the SST should be further studied. Based on a simple SST model, an energy feed-forward scheme for the isolation stage and a direct power feed-forward scheme for the rectifier are proposed in [20], which improve the dynamic performance of the DC-link voltage during load fluctuation. A data-driven coordinated controller architecture for a multiple active

bridge-based SST is proposed in [21]. This controller optimizes the target value by collecting and analyzing the global information of the SST, and improves the MVDC-link and LVDC-link voltage quality of the SST under grid-side abnormal conditions.

In this paper, a three-stage SST that adopts an MMC as the input stage and a CLLC resonant converter, as the isolation stage is modeled, and a hierarchical coordinative control strategy is proposed. The control strategy aims to improve the DC port voltage quality of the SST when the microgrid output is fluctuating. Compared with other control strategies, a coordinated control strategy between DGs and local energy storage equipment is designed by utilizing super capacitors, which can quickly compensate the power fluctuation of DGs. In addition, the control loop proposed in this paper can eliminate the current imbalance at both ends of the buffer capacitor caused by the power response speed difference of the MMC and CLLC. This control strategy is not only applicable to the situation of power fluctuation in microgrids, but also effective to other kinds of transient conditions, such as the microgrid isolation during fault and the islanding process.

The rest of this paper is organized as follows: in Section 2, an overview of an SST-based microgrid is presented. The mathematical model and problems existing in the independent control strategy are introduced. In Section 3, a hierarchical coordinative control is proposed to improve the DC bus voltage stability. A detailed frequency-domain analysis, compared with independent control, is discussed. Finally, simulation results under different conditions are demonstrated in Section 4, followed by the conclusions in Section 5.

## 2. Overview of the SST-Based DC Microgrid System

### 2.1. Mathematical Model of the SST

The topology of the solid state transformer used in this paper is shown in Figure 2. Compared with the traditional topology, a three-phase MMC is selected to replace the CHB as the input stage, and a CLLC resonant converter is used to replace the DAB converter as the isolation stage. As mentioned above, an MMC can reduce the number of power switching devices and high frequency transformers. Under the comparative conditions in the literature [22], an MMC can reduce the number of switching devices by 20% and the number of high-frequency transformers by 50%, in contrast to CHB. The CLLC resonant converter is a new type of structure, which has not been fully covered in the literature on SSTs.  $E_a$ ,  $E_b$ , and  $E_c$  are the voltages of the three-phase distribution network;  $i_a$ ,  $i_b$ , and  $i_c$  are the currents of distribution network;  $L_s$  and  $L_a$  represent the smoothing inductor on the grid side and the arm inductor of MMC, respectively;  $U_a$ ,  $U_b$ , and  $U_c$  are the AC output voltages of MMC;  $C_H$  and  $C_L$  are the series HVDC link capacitor and parallel CLLC output capacitor, respectively;  $C_s$  represents the MMC submodule capacitor;  $N$  denotes the number of arm submodules of MMC, and the same number for the CLLC submodule;  $i_o$  and  $i_L$  represent output-stage load current and inductance current, respectively; and  $L_f$  and  $C_f$  represent the LC filter parameters.

The topology of the SST-based DC microgrid is shown in Figure 3. In this system, the SST functions as an energy center to balance the power flow among the regional distribution network, DC microgrid, and the household LVAC load. The voltage level of the distribution network is 10 kV. The DC microgrid consists of photovoltaic (PV) power supply, energy storage system (ESS), and DC loads. It is connected to the distribution grid through the 700 V LVDC port of the SST.

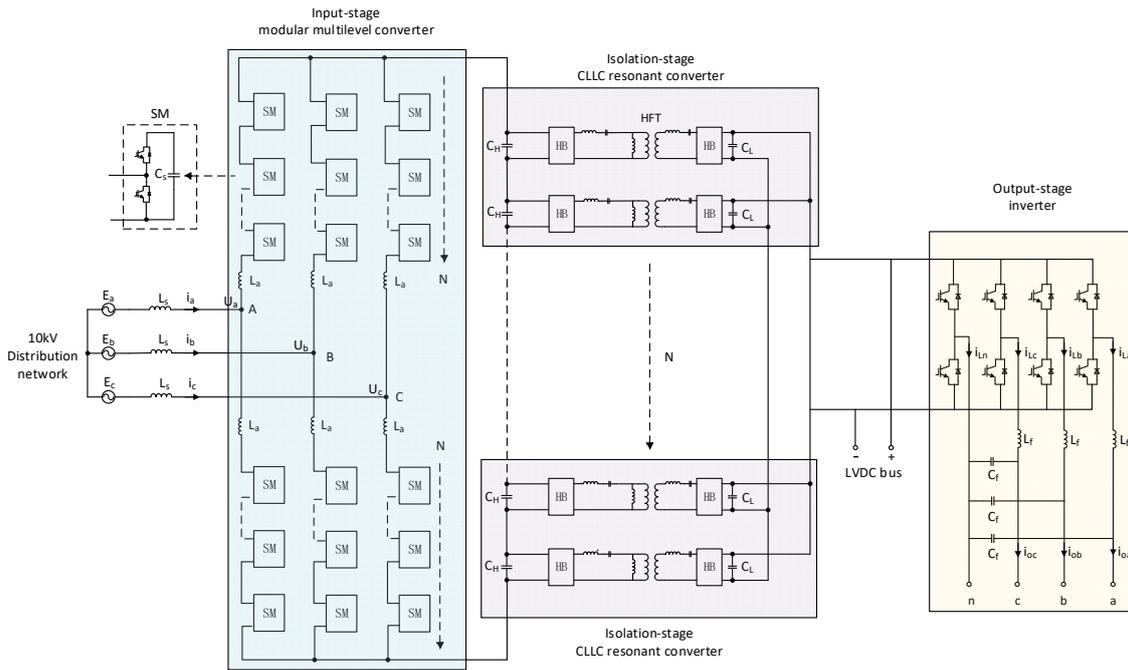


Figure 2. Topology of the solid state transformer (SST).

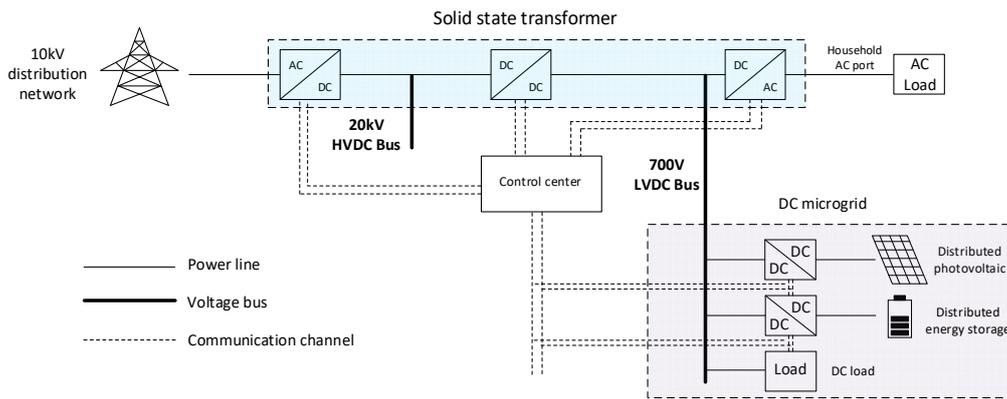


Figure 3. Topology of a DC microgrid system.

In synchronous rotating coordinates (d-q coordinates), the dynamic equations of the MMC can be described in Equation (1):

$$\begin{cases} (L_s + \frac{L_a}{2}) \frac{di_d}{dt} = E_d - U_d + \omega(L_s + \frac{L_a}{2})i_q \\ (L_s + \frac{L_a}{2}) \frac{di_q}{dt} = E_q - U_q - \omega(L_s + \frac{L_a}{2})i_d \\ C_{He} \frac{dU_{dc}}{dt} = \frac{3E_d i_d}{2U_{dc}} - \sum_{i=1}^N i_{1i} = \frac{3E_d i_d}{2U_{dc}} - i_1 \end{cases} \quad (1)$$

where  $E_d$  and  $E_q$  are the AC voltages of the distribution grid under d-q coordinates;  $i_d$  and  $i_q$  are the AC currents;  $U_d$  and  $U_q$  are the line-frequency output voltages of the MMC under d-q coordinates;  $\omega$  is the fundamental frequency;  $U_{dc}$  is the HVDC bus voltage;  $C_{He}$  is the equivalent shunt capacitor of the HVDC link;  $i_{1i}$  is the input current of the CLLC submodule  $i$ ; and  $i_1$  is the sum of the  $N$  submodule input currents of CLLC.

The topology of a single submodule of the CLLC resonant converter is shown in Figure 4, where  $i_{dc}$  is the input current of the HVDC link;  $U_{dci}$  and  $U_{out}$  are the input and output DC voltages of the submodule;  $i_{1i}$  and  $i_{2i}$  are the input and output currents;  $i_{Li}$  is the outlet current of submodule  $i$ , and  $i_L$

is the outlet current of the overall input-series–output-parallel (ISOP) CLLC resonant converter;  $C_{r1}$ ,  $L_{r1}$  and  $C_{r2}$ ,  $L_{r2}$  are the resonant capacitors and inductors on the primary and secondary sides;  $L_m$  is the magnetic inductor, which can be integrated inside the HFT;  $n$  is the transformation ratio of the HFT;  $NC_L$  represents the equivalent parallel capacitance of the LVDC link; and  $i_{inv}$  and  $i_{mc}$  are the input currents of the output stage and local DC microgrid.

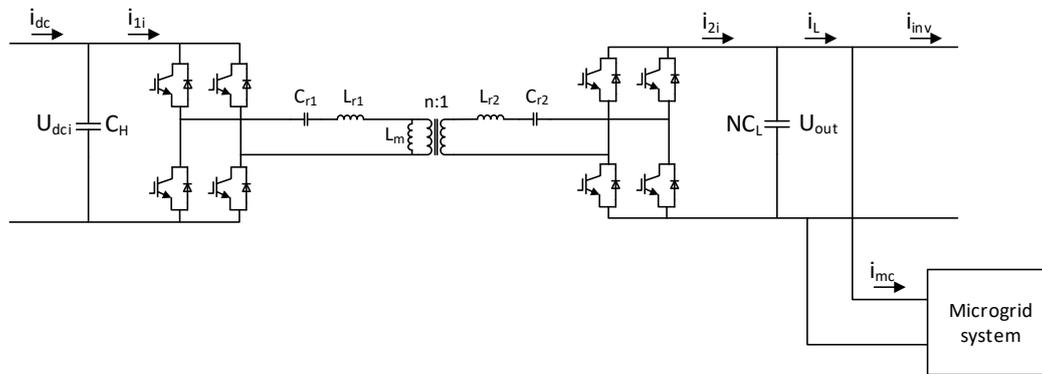


Figure 4. The submodule topology of the CLLC resonant converter.

Under single-phase-shift control, the transmission power of the CLLC resonant converter can be obtained as:

$$P_{CLLCi} = \frac{8nU_{dci}U_{out}}{\pi^2 |Z_{eqi}|} \cos(\varphi_i + \theta_i) \tag{2}$$

where  $P_{CLLCi}$  is the transmission power of submodule  $i$ ;  $\varphi_i$  is the phase shift angle between two H-bridges; and  $|Z_{eqi}|$  and  $\theta_i$  are the magnitude and phase of the equivalent impedance  $Z_{eqi}$ , which can be calculated as:

$$Z_{eqi} = \frac{Z_1(Z_m + Z_2 + \frac{8}{\pi^2}Z_{loadi}) + Z_m(Z_2 + \frac{8}{\pi^2}Z_{loadi})}{Z_m} = |Z_{eqi}| \angle \theta_i \tag{3}$$

where  $Z_1$ ,  $Z_2$ ,  $Z_m$ , and  $Z_{loadi}$  represent the primary-side LC resonant impedance, secondary-side resonant impedance, the excitation impedance of the HFT, and load impedance (all equivalent to the primary side). From Equations (2) and (3), the input and output currents of the isolation stage can be calculated as:

$$\begin{cases} i_{1i} = \frac{8nU_{out}}{\pi^2 |Z_{eqi}|} \cos(\varphi_i + \theta_i) \\ i_{2i} = \frac{8nU_{dci}}{\pi^2 |Z_{eqi}|} \cos(\varphi_i + \theta_i) \end{cases} \tag{4}$$

and the dynamic equation of output voltage can be expressed as:

$$NC_L \frac{dU_{out}}{dt} = \sum_{i=1}^N i_{2i} - i_{inv} - i_{mc} = i_2 - i_L \tag{5}$$

where  $i_2$  is the sum of the output currents of  $N$  CLLC submodules. Without loss of generality, the voltage and power balance control between the CLLC submodules are not considered in this paper, that is to say, the operating variables of  $N$  submodules are assumed to be the same, so the ISOP CLLC resonant converter can be equivalent to one submodule.

### 2.2. Problems Existing in the Independent Control Strategy

In the three-stage independent control, the input-stage MMC adopts voltage and current double-loop control to maintain the HVDC bus voltage and adjust the power factor on the distribution

grid side; the CLLC adopts single-phase-shift control to regulate the parallel output voltage of the isolation stage. The control diagram is shown in Figure 5. In this figure,  $Q$  is the reactive power of the distribution network;  $G_{udc}$ ,  $G_{id}$ ,  $G_q$ , and  $G_{iq}$  represent the double-loop controller functions of the MMC; and  $G_{uo}$  is the controller function for the CLLC, which adopts single voltage-loop control, so no high-precision current sensor is needed. The part inside the dotted box represents the relation between  $\varphi_i$  and  $i_{2i}$ , which has been given by the second line of Equation (4). It is obvious that  $G_{ps}$  is a nonlinear function, since the CLLC usually works near the resonant frequency point, which means that  $\theta_i \approx 0$ . Therefore, a linear approximation for  $G_{ps}$  is carried out in this paper. The approximate expression after linearization is as follows ( $0 < \varphi < \pi$ ):

$$\begin{cases} i_{2i} = a + b\varphi_i \\ a = \frac{8nU_{dc}}{\pi^2 |Z_{eqi}|} \\ b = \frac{16nU_{dc}}{\pi^3 |Z_{eqi}|} \end{cases} \quad (6)$$

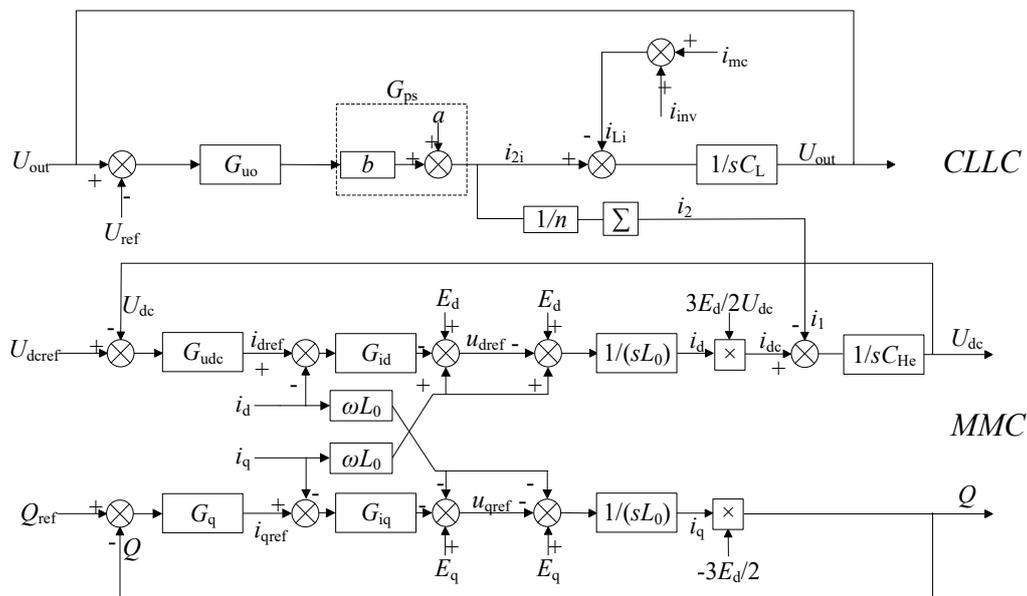
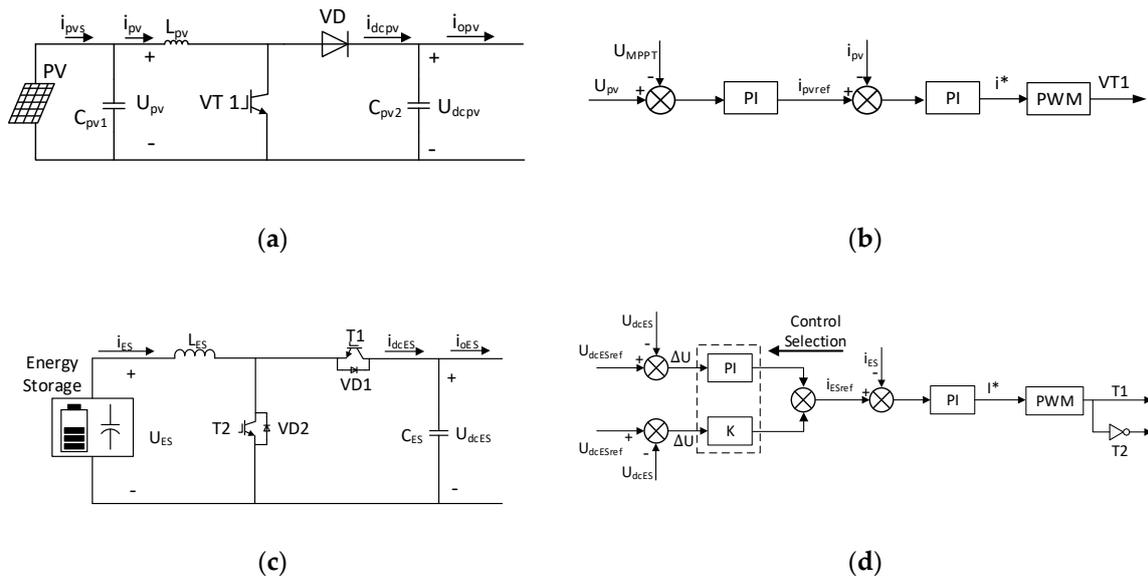


Figure 5. The independent control strategy of the SST.

As mentioned previously, the topology of the grid-connected DC microgrid system is shown in Figure 3. A boost chopper circuit is usually adopted as the interfacing converter for PV to realize the maximum power point tracking (MPPT) control [23,24]. The topology and control diagram are shown in Figure 6a,b. For the energy storage system, which includes batteries and super capacitors, the interface converter must realize a bidirectional power transmission, so the current reversible chopper circuit is usually used. Common control methods include constant DC voltage control and voltage droop control. The topology and control diagram are shown in Figure 6c,d.



**Figure 6.** Topology and control strategy of the photovoltaic (PV) and energy storage system (ESS): (a) the interface converter for the PV; (b) the maximum power point tracking (MPPT) control diagram for the PV; (c) The interface converter for the ESS; (d) The control strategy for the ESS.

In normal operation, the SST acts as the balance node of the system to provide the voltage and frequency support, the DGs output at maximum power, and the energy storage equipment responds to the control-center command. In this case, fast and continuous fluctuations of the distributed power output will be sufficiently compensated in real time by the SST. It can be seen from Figure 5 that the output current of the microgrid is the interference to the CLLC control loop, which means that the change of  $i_{Li}$  leads to the fluctuation of  $i_{2i}$  and  $U_{out}$ . The current of the CLLC port is the interference to the MMC active power control loop, which means that the change of  $i_{2i}$  will further lead to the fluctuation of  $U_{dc}$ . In addition, the difference of power response speed between the MMC and CLLC resonant converter will aggravate the situation. From Figure 5, the transfer function of the CLLC output DC current  $i_{2i}$  to its load current  $i_{Li}$  can be obtained. Since the CLLC can be equivalent to one submodule, so the transfer function of  $i_2$  to  $i_L$  will be the same as  $i_{2i}$  to  $i_{Li}$ , as illustrated in Equation (7):

$$\frac{i_2}{i_L} = \frac{G_{uo}G_{ps}}{G_{uo}G_{ps}-sNC_L} \tag{7}$$

Similarly, the transfer function of the MMC output DC current  $i_{dc}$  to the CLLC input current  $i_1$  can be expressed as:

$$\frac{i_{dc}}{i_1} = \frac{3E_dG_{udc}G_{idd}}{3E_dG_{udc}G_{idd}-2U_{dc}C_{He}} \tag{8}$$

where  $G_{idd}$  is the transfer function of the grid connected current in the d-axis, and its expression is:

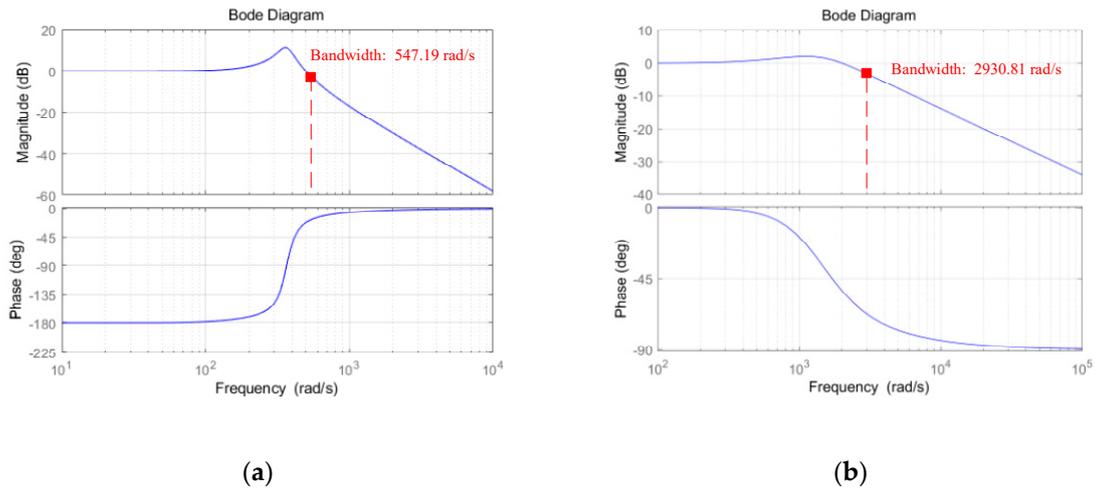
$$G_{idd} = \frac{i_d}{i_{dref}} = \frac{G_{id}}{G_{id}+L_0s} \tag{9}$$

According to the control parameters listed in Table 1 and the system hardware simulation parameters listed in Table 2 in Section 4, the current response Bode diagrams of HVDC and LVDC links can be drawn, as shown in Figure 7. In Table 1, the proportion and integral parameters of PI controllers are distinguished by the subscripts P and I. For example,  $K_{uo} = K_{Puo} + K_{Iuo}$ . It can be seen from Figure 7 that the closed-loop bandwidth of  $i_2$  to  $i_L$  is 2930.81 rad/s, which is much larger than the 547.19 rad/s of  $i_{dc}$  to  $i_1$ . It indicates that the power adjustment speed of the CLLC is much faster than that of the MMC. Therefore, when the output power of the microgrid fluctuates dramatically, such as

switching from absorbing electricity to generating electricity to the distribution network, the power response speed of the CLLC is much faster than that of the MMC.

**Table 1.** Parameters of the solid state transformer controller.

Variables	Value	Variables	Value
$K_{Puo}$	0.04	$K_{Iuo}$	40
$K_{Pudc}$	4	$K_{Idc}$	100
$K_{Pid}$	0.5	$K_{Iid}$	50



**Figure 7.** Current response Bode diagrams under independent control: (a) current response of the high-voltage DC (HVDC) link; (b) current response of the low-voltage DC (LVDC) link.

According to the dynamic Equation (1), the capacitance voltage fluctuation of the HVDC link depends on the current difference between its two sides, that is, the capacitance voltage itself is determined by the difference of the current integral value:

$$U_{dc} = \frac{1}{C_{He}} \int i_{dc} dt - \frac{1}{C_{He}} \int i_1 dt \tag{10}$$

### 3. Hierarchical Coordinative Control Strategy Design

#### 3.1. The Hierarchical Coordinative Control for the SST-Based DC Microgrid System

With respect to the problems existing in the independent control, a hierarchical coordinative control strategy for the SST and microgrid composite system is proposed. In general, the hierarchical coordinative control mitigates the local microgrid’s external power fluctuation and realizes a joint action of the MMC and the CLLC during the dynamic process. The comparison of control logic between independent control and coordinative control is shown in Figure 8.

The overall coordinative control diagram is shown in Figure 9. This novel control strategy contains two layers: the microgrid layer and the SST layer. In Figure 8a,  $G_{UES}$  and  $G_{IES}$  represent the ESS double-loop PI controller;  $G_{UPV}$  and  $G_{IPV}$  are the control functions for the PV controller;  $K_{PWMESS}$  and  $K_{PWMPV}$  are the equivalent gain of the pulse width modulation (PWM) links for ESS and PV, respectively ( $K_{PWMESS} \approx U_{dcES}$ ,  $K_{PWMPV} \approx U_{dcPV}$ ); and  $d_{ES}$  and  $d_{PV}$  are the equivalent duty cycles. The meaning of the remaining parameters of Figure 9 has been given in Figure 6.

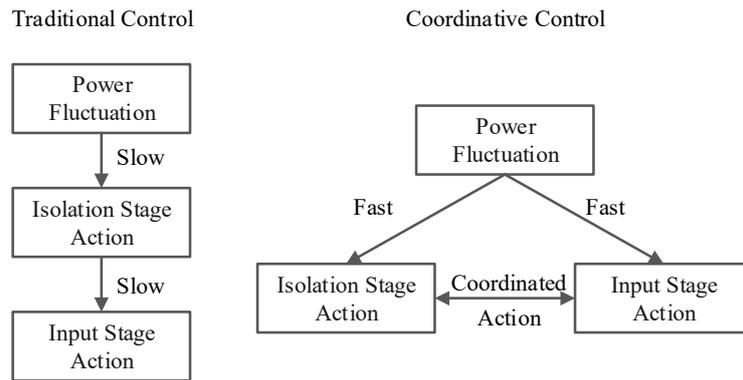


Figure 8. Control logic of the independent control and proposed coordinative control.

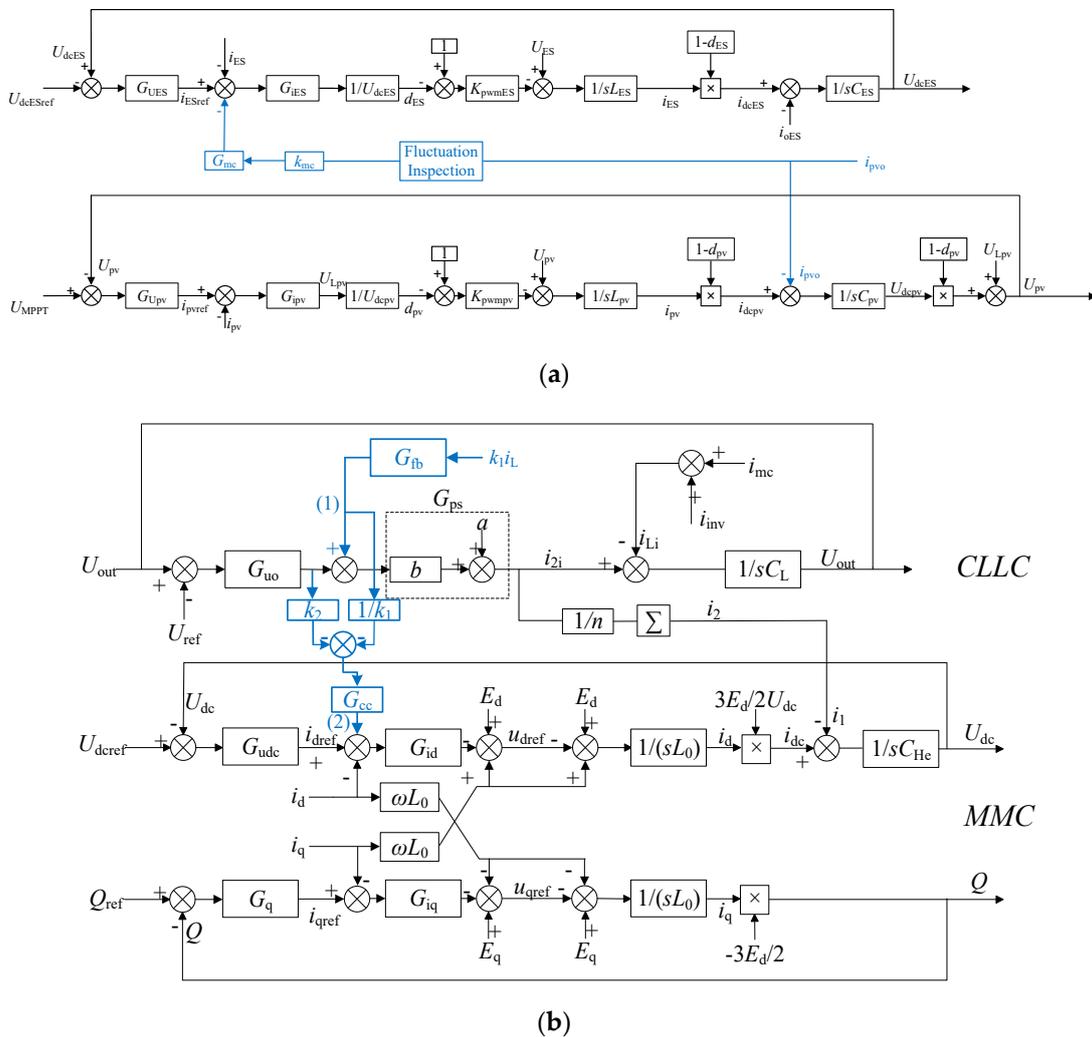


Figure 9. The hierarchical coordinative control diagram: (a) the microgrid layer control; (b) the SST layer control.

In the microgrid layer control, the additional control branch feeds the variation of PV outlet current back to the inner current loop of super capacitors inside the ESS, giving full play to the fast regulation capability of super capacitors. Although mechanical and battery energy storage systems are still the key elements in system operation, super capacitors nowadays are drawing an increasing

interest [25], due to the advantages of high efficiency and high power density [26]. This paper adopts a hybrid energy storage device combining super capacitors and batteries, as discussed in [27–29]. In the additional control branch,  $k_{mc}$  is the coordinative control coefficient, which reflects the compensation degree of PV output fluctuation by the ESS.  $G_{mc}$  is the coordinative transfer function, and the fluctuation inspection section represents the instruction-receiving and triggering module.

In the SST layer control, the control branch 1 feeds the load current of the CLLC forward to the inner current loop as a new control variable to improve the dynamic current response speed of the CLLC stage. The additional control branch 2 not only feeds the output of the CLLC voltage controller back to the inner loop of the MMC, bringing the two parts of the SST together to complete the task of LVDC bus voltage control, but also feeds the CLLC load current back, to eliminate the influence of the CLLC current fluctuation on the HVDC link at the same time. Similar to the microgrid layer control,  $k_1$  and  $k_2$  are additional control coefficients;  $G_{fb}$  and  $G_{cc}$  are the corresponding transfer functions. The expressions are as follows:

$$\begin{cases} G_{mc} = \frac{G_{iES} + sL_{ES}}{G_{iES}} \\ G_{fb} = \frac{1}{b} \\ G_{cc} = -\frac{2bU_{dc}(G_{id} + sL_0)}{3nE_dG_{id}} \end{cases} \quad (11)$$

### 3.2. Comparative Analysis of Microgrid Power Fluctuation Response of the DC Link

From Figures 4, 5 and 9b, the voltage response functions of the SST DC links to the CLLC load current  $i_L$  under the independent control can be given in Equation (12), where  $L_0$  is equal to  $L_s + \frac{L_d}{2}$  and is the equivalent inductance on the AC side of the MMC.

$$\begin{cases} \frac{U_{out}}{I_L} = \frac{1}{bG_{uo} - NC_L s} \\ \frac{U_{dc}}{I_L} = -\frac{bG_{uo}}{n(bG_{uo} - NC_L s)(sC_{He} + \frac{3E_dG_{udc}G_{idd}}{2U_{dc}})} \end{cases} \quad (12)$$

Since the independent control is only for three-stage SST converters, the proposed microgrid layer control is not considered in the comparative analysis. From Figure 9b, the corresponding disturbance response functions under the SST-layer coordinative control can be expressed as:

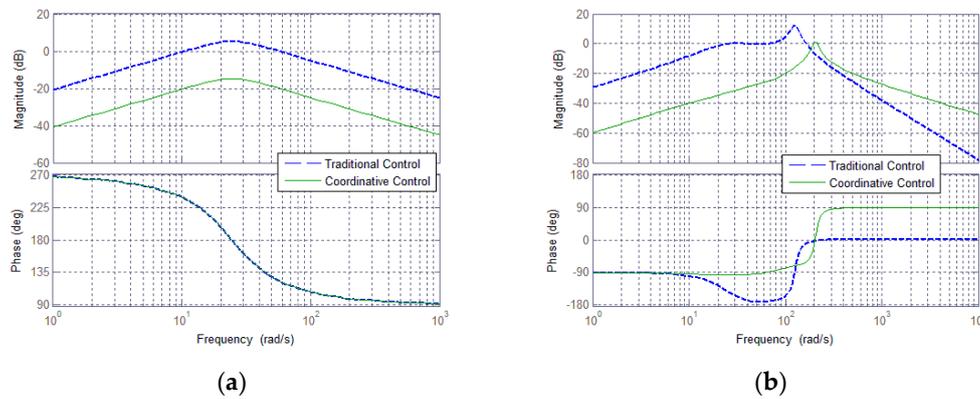
$$\begin{cases} \frac{U_{out}}{I_L} = \frac{1-k_1}{bG_{uo} - NC_L s} \\ \frac{U_{dc}}{I_L} = -\frac{(1-k_1)(bk_2G_{uo} - NC_L s)}{n(bG_{uo} - NC_L s)(sC_{He} + \frac{3E_dG_{udc}G_{idd}}{2U_{dc}})} \end{cases} \quad (13)$$

As can be seen from Equations (12) and (13), the additional control branches change the numerator of the disturbance response functions. If the value of the control parameter  $k_1$  is close to 1, the dynamic voltage fluctuation problem of HVDC and LVDC buses caused by microgrid output power swing can be completely solved in theory. The coefficient  $k_2$  aims to improve the dynamic power tracking speed difference between the MMC and the CLLC, so as to realize the joint regulation of these two stages in the dynamic process. Although this effect is not clearly reflected in the above formulas, it can be seen from the disturbance transfer function of HVDC bus voltage to the CLLC input current  $i_1$  before and after the introduction of the  $k_2$  branch, as shown in Equation (14). The introduction of  $k_2$  improves the tracking ability of the MMC to current  $i_1$ , and the whole coordinative control branch (2) does not need additional sensors.

$$\begin{cases} \frac{U_{dc}}{I_1} = -\frac{1}{sC_{He} + \frac{3E_dG_{udc}G_{idd}}{2U_{dc}}} \\ \frac{U'_{dc}}{I_1} = -\frac{1-k_2}{sC_{He} + \frac{3E_dG_{udc}G_{idd}}{2U_{dc}}} \end{cases} \quad (14)$$

The system simulation parameters are shown in Table 2. According to Equations (12) and (13), the Bode diagrams of the disturbance response functions can be obtained, as shown in Figure 10.

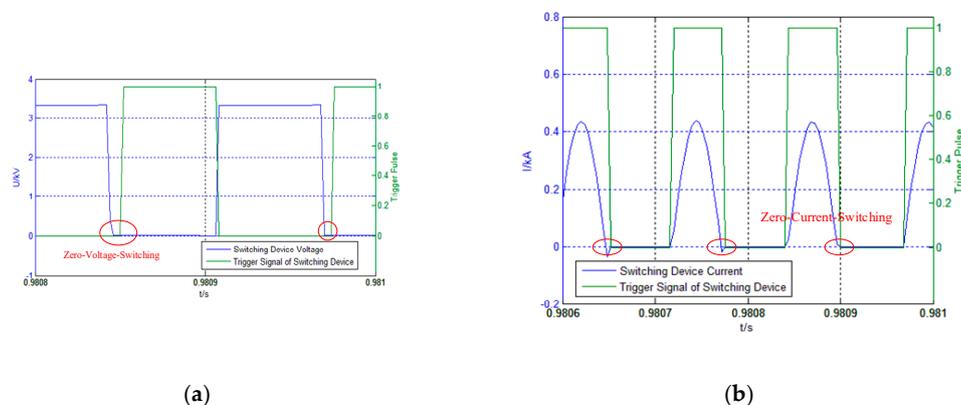
From this figure, it can be seen that the coordinative control strategy proposed in this paper can significantly improve the low-frequency amplitude gain, indicating that this coordinative strategy has a better suppression for the DC bus voltage fluctuating during a same dynamic process. The Bode diagram of Equation (14) is similar to that of Equation (12), since the coefficient  $k_2$  acts on the numerator, and so it is not repeated here.



**Figure 10.** The voltage response Bode diagrams of the HVDC and LVDC links to the CLLC load current: (a) the LVDC bus voltage response; (b) the HVDC bus voltage response.

#### 4. Simulation Results

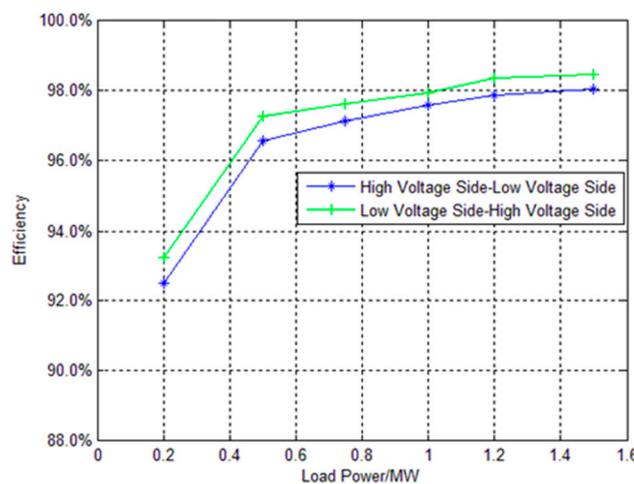
The model of the SST-based DC microgrid system, as shown in Figure 3, is built by PSCAD/EMTDC to verify the proposed coordinative control. PSCAD/EMTDC is a professional electromagnetic transient simulation software, which is also suitable for power electronics system simulations. The simulation parameters are listed in Table 2. The rated capacity of the SST is 1.5 MVA, and the distribution grid keeps running under unity power factor. In steady-state operation, the output stage of the SST has a 1 MW three-phase unbalanced load. At this time, the working waveform of the CLLC is shown in Figure 11. It can be seen that the voltage zero-crossing point of the primary-side switch is ahead of the turn-on signal, and the current zero-crossing point of the secondary-side switch is ahead of the turn-off signal, thereby reducing switching losses. Figure 12 shows the efficiency curve of the CLLC resonant converter under different load conditions. It can be seen that, when the power is transmitted bidirectionally, the half-load efficiency can reach above 97%, and the efficiency can reach above 98% at a rated power of 1.5 MW.



**Figure 11.** The steady-state working waveform of the CLLC: (a) the zero-voltage-switching waveform of the primary-side switching device; (b) the zero-current-switching waveform of the secondary-side switching device.

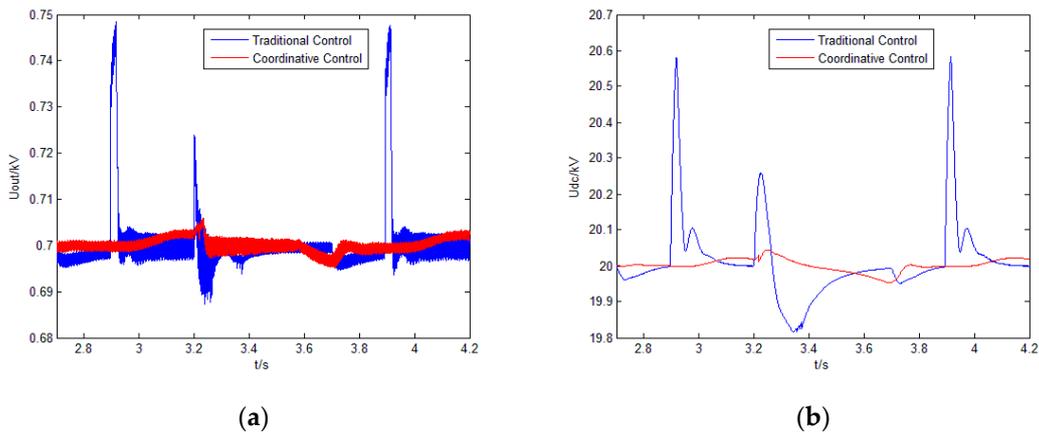
**Table 2.** The simulation parameters of the SST-based DC microgrid system.

Variable Description	Value
Distribution network voltage level	10 kV
Distribution grid side filter inductor ( $L_s$ )	10 mH
Three-phase arm inductance of MMC ( $L_a$ )	20 mH
Number of submodules of MMC and CLLC ( $N$ )	6
Reference value of HVDC voltage ( $U_{dcref}$ )	20 kV
Primary-side voltage of CLLC submodule ( $U_{dci}$ )	3.33 kV
Secondary-side voltage of CLLC submodule ( $U_{out}$ )	700 V
Turns ratio of HFT ( $n$ )	4.76:1
HVDC-link series capacitance ( $C_H$ )	3000 $\mu$ F
LVDC-link shunt capacitance ( $C_L$ )	3000 $\mu$ F
Primary-side resonant inductance ( $L_{r1}$ )	15 $\mu$ H
Primary-side resonant capacitance ( $C_{r1}$ )	19 $\mu$ F
Secondary-side resonant inductance ( $L_{r2}$ )	0.216 $\mu$ H
Primary-side resonant capacitance ( $C_{r2}$ )	1319.42 $\mu$ F
CLLC excitation inductance ( $L_m$ )	2300 $\mu$ H
Coordinative control coefficient $K_1$	0.9
Control coefficient $K_2$	0.9



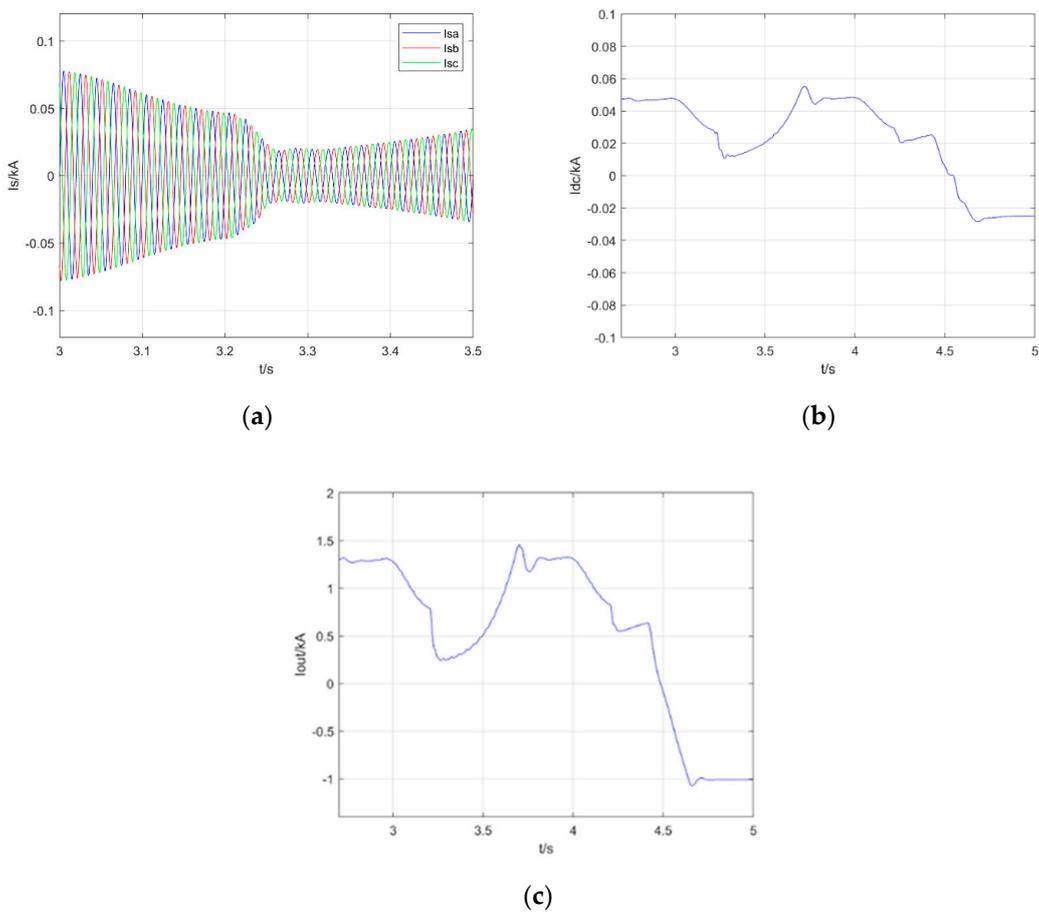
**Figure 12.** Efficiency curve of the CLLC under different load conditions.

At 1.5 s, the DC microgrid is connected to the system, the PV output is 0.3 MW, and the DC load is 0.2 MW. Starting from 2.7 s, the output power of the PV supply in the microgrid fluctuates continuously in a wide range, and the variation rule is 0.3 MW–2 MW–0.3 MW–2 MW. In this process, the power flow direction of the SST will change frequently under independent control. Figure 13 shows the response of the LVDC and HVDC bus voltages. It can be seen from the comparison that the hierarchical coordinative control strategy proposed in this paper can quickly stabilize the bus voltage and greatly improve the power quality in the dynamic process. Using traditional control strategy, the maximum transient voltage changes of the LVDC and HVDC links are about 47 V and 580 V, respectively. However, under the proposed coordinative control strategy, the DC bus voltage has almost no fluctuation.



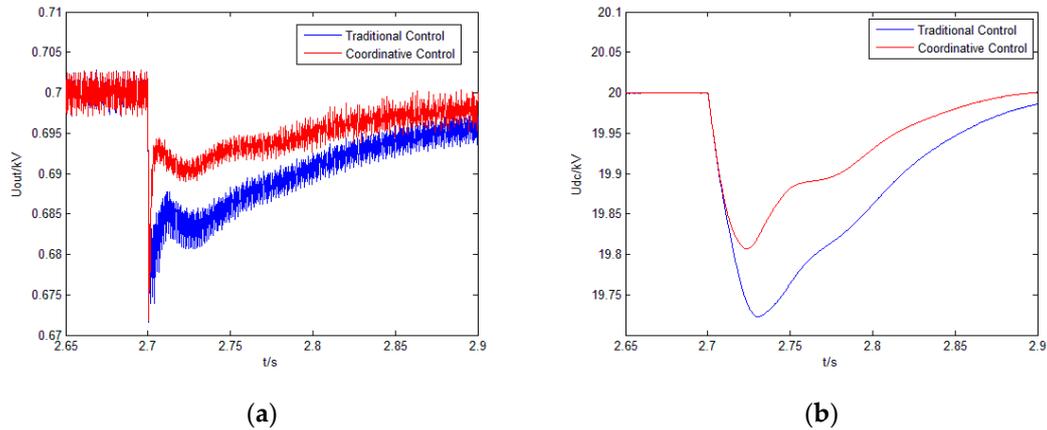
**Figure 13.** The comparison of voltage response under continuous power fluctuation: (a) the LVDC bus voltage response; (b) the HVDC bus voltage response.

The microgrid layer control utilizes the fast power response of super capacitors to smooth the power fluctuation of the DGs. The current waveform of the SST during power fluctuation is shown in Figure 14. It can be seen that the compensated DG output current does not cause frequent fluctuations in the SST power transmission direction, and the change of SST current is relatively smooth.



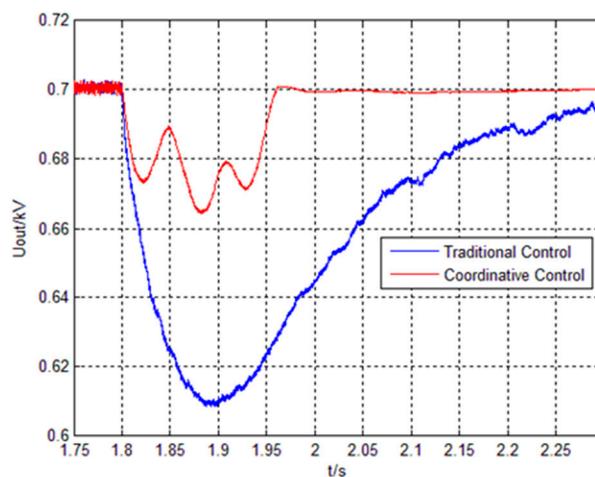
**Figure 14.** The current waveform of the SST under continuous power fluctuation: (a) the distribution network current; (b) the HVDC-link current; (c) the LVDC-link current.

It is worth noting that the proposed coordinative control strategy can actually be applied to mitigate dynamic voltage fluctuation conditions. For example, when the system detects a fault in the DC microgrid and trips it off at 2.7 s, the corresponding voltage response is shown in Figure 15. Before removal, the output of the PV power supply is 1 MW. It can be seen from the figure that the SST layer coordinative control at this time can rapidly compensate for the power shortage and restore the DC link voltages to the given value more quickly.



**Figure 15.** The comparison of voltage response after the DC microgrid is tripped off: (a) the LVDC bus voltage response; (b) the HVDC bus voltage response.

When the control strategy shown in Figure 9a is slightly changed to make the super capacitors dynamically compensate for the input current of the output-stage inverter in the island switching process, i.e.,  $i_{inv}$  in Figure 4, the coordinative control can also smooth the island switching process. The voltage waveform of the LVDC bus under this condition is shown in Figure 16. Although only the microgrid layer coordinative control plays a role at this time, the bus voltage fluctuation could still be suppressed by a considerable extent. Under the microgrid layer coordinative control, the maximum voltage sag is about 37 V. While under the independent control, the maximum voltage sag is about 90 V, and the voltage needs longer time to recover.



**Figure 16.** The comparison of voltage response during the island switching process.

The strategies to improve the SST power quality in previous studies are mostly considering the power-side disturbances [30] and load fluctuations [31]. However, power-side disturbances and load fluctuations do not directly act on the DC buses of the SST, and they can always be isolated by adjacent

inverters. In both cases, independent control strategies can maintain good power quality. At present, there are few researches on the power quality problem of SST DC ports caused by the output fluctuation of microgrid.

## 5. Conclusions

In this paper, the topology of the SST is improved, and a hierarchical coordinative control strategy for an SST integrated DC microgrid system is proposed to solve the dynamic voltage quality problem of SST DC ports caused by the random and intermittent characteristics of distributed generators. Through mathematical analysis and simulation, conclusions can be drawn as follows:

- (1) At present, the main factors affecting the practical application of SSTs are high cost and low energy transmission efficiency. The adopted input-stage MMC instead of cascaded H-bridge can significantly reduce the required number of power electronic switches and high-frequency transformers in the SST, thus reducing the system cost. As for the isolation stage that accounts primarily for SST power losses, the efficiency of the CLLC resonant converter adopted in this paper can reach above 98% at rated power, which is greatly improved, compared with the DAB converter, whose efficiency is only about 90%.
- (2) Under the independent control, the power response speed of the SST is slow, and the output fluctuation of the microgrid cannot be compensated quickly and timely, bringing serious dynamic voltage stability problems for the DC link voltages. The hierarchical coordinative control strategy proposed in this paper can not only improve the external power characteristics of the DC microgrid, but also realize a coordinated action between the input stage and isolation stage of the SST, which can greatly suppress the voltage fluctuation of the HVDC and LVDC bus.
- (3) The coordinative control strategy is not only applicable to the microgrid output fluctuation situation, but also effective to other transient conditions, such as the removal of the microgrid under fault, and the island switching process.

**Author Contributions:** conceptualization: Z.L. and T.Z.; methodology: Z.L. and Y.W.; software: Z.L., Y.W., and C.Y.; validation: Z.L.; formal analysis: Z.L.; writing—original draft preparation: Z.L., Y.W., and C.Y.; writing—review and editing: Z.L., C.Y., and T.Z.; visualization: Z.L. and C.Y.; supervision: T.Z.; project administration: T.Z.; funding acquisition: T.Z. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the Key Research and Development Program of Shaanxi Province, grant number 2019ZDLGY18-06.

**Conflicts of Interest:** The authors declare that there are no conflicts of interest.

## Abbreviations

CHB	Cascaded H-bridge
DAB	Dual active bridge
DABCI	Dual active bridge cascaded with inverter
DG	Distributed generation
ESS	Energy storage system
FEC	Front-end converter
HFT	High frequency transformer
HVDC	High-voltage direct current
ISOP	Input-series output-parallel
LVDC	Low-voltage direct current
MMC	Modular multilevel converter
MPPT	Maximum power point tracking
PV	Photovoltaic
PWM	Pulse width modulation
SST	Solid state transformer

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