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Power Line Interference Reduction Technique with a Current-Reused Current-Feedback Instrumentation Amplifier for ECG Recording

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Featured Application: A portable two-electrode ECG monitoring application.

Abstract: This paper presents a power line interference (PLI) reduction technique with a current-reused current-feedback instrumentation amplifier (CFIA) for electrocardiogram (ECG) recording. In a portable two-electrode ECG monitoring application, the presence of undesired PLI may severely corrupt the quality of ECG recording. Since PLI can be over a few volts, the input signal including the ECG signal can exceed the supply or ground level by an electrostatic discharge (ESD) diode in input/output (I/O) pad. To prevent this problem, this paper presents a continuous-time input common-mode current feedback loop that can limit displacement current from a capacitive coupling between the human body and a power line. The continuous-time input common-mode current feedback loop can clamp an input common-mode voltage to the saturation region of the input transistor of the current-reused CFIA. After the clamping procedure, the clamped input signal is amplified by the current-reused CFIA. The proposed circuit was designed using a 0.18-μm bipolar-complementary metal semiconductor–double-diffused metal oxide semiconductor (BCDMOS) process with an active area of 1.8 mm^2. The total power consumption is 18 μW with 1.8 V. The input-referred noise and noise efficiency factor (NEF) of the current-reused CFIA is 2.68 μV_{RMS} and 4.28 with 107 Hz, respectively.

1. Introduction

A portable electrocardiogram (ECG) monitoring system allows for the long-term identification of an individual's heart condition for the early detection of cardiovascular disease, such as cardiac arrhythmia and heart failure. In a conventional ECG measurement configuration with three or more electrodes, an additional reference electrode or the driven-right-leg (DRL) technique is widely used to reduce power line interference (PLI) [1,2], however, in portable or wearable applications, a two-electrode configuration is preferred because of its portability and its long-term ECG monitoring ability [3–6].

The main drawback of a two-electrode configuration is that the human body is severely affected by PLI when the floated body lacks a grounded electrode [7]. The frequency range and dynamic range of an ECG signal are approximately from 0.05 to 100 Hz and from 1 to 10 mV, respectively [8].

Considering that PLI has a frequency component of 50–60 Hz, over a few volts, the PLI can lead to serious problems in ECG monitoring.

The generation of PLI and the saturation effect of the electrostatic discharge (ESD) diode is shown in Figure 1. The PLI is mainly generated by a displacement current, I_{PL}, through a capacitive coupling between a human body and the power line. Since the PLI can be more than a few volts, depending on the mismatch of skin–electrode contact impedance, the ESD diode of an input/output (I/O) pad can be put into a turned-on state by the PLI. A turned-on ESD diode makes an input CM signal reach the supply and ground level, which means that input CM voltage is out of the saturation range of the input transistor of the ECG amplifier. In this case, the ECG amplifier cannot amplify the raw ECG.

To solve this problem, a discrete-time PLI reduction circuit was previously reported [9]. However, raw ECG signal processing prior to amplification in the discrete time region requires a wider bandwidth of the ECG amplifier, which has more than a few kHz. In terms of power consumption, a wider bandwidth feature leads to a shorter battery time. When the long-term use of a portable ECG monitoring device is required, this power consumption problem must be solved.
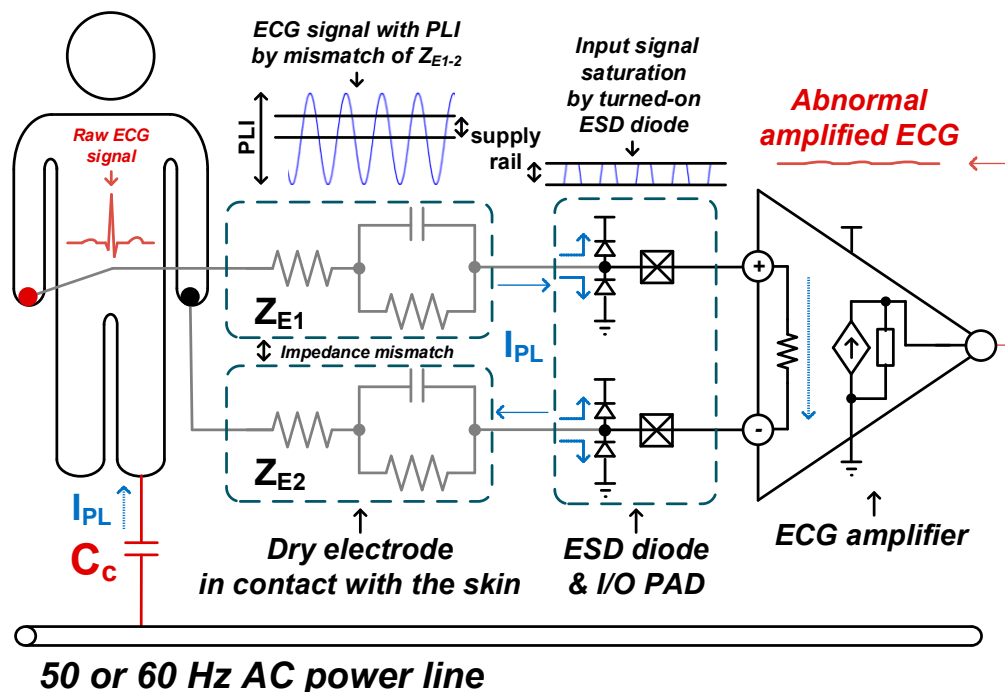

Figure 1. Generation of power line interference (PLI) and the saturation effect of the electrostatic discharge (ESD) diode.

The ECG amplifier is one of the key building blocks of the current consumption, common-mode rejection ratio (CMRR), input-referred noise, and gain in an entire ECG monitoring system. For long-term monitoring of an ECG, ultra-low current consumption is essential to maintaining the function of ECG measurement. To achieve accurate ECG signal acquisition, a low enough input-referred noise and high CMRR is demanded. An instrumentation amplifier (IA) is suitable for the ECG amplifier. A capacitively coupled IA (CCIA) is widely used for high-power efficiency and low noise [10–12]. In particular, the current-reused CCIA can achieve a good noise efficiency factor (NEF) [13]. However, the CCIA has a low input impedance, which can lead to excessive PLI and a lower CMRR. Since this problem degrades the ECG signal, the ECG amplifier demands a high input impedance while having low noise, a high CMRR, and ultra-low current consumption.

This paper presents a PLI reduction technique with a current-reused current-feedback IA (CFIA) for ECG recording. To prevent exceeding the saturation range of an input transistor of the current-reused CFIA by PLI, the proposed circuit implements a continuous-time input CM current-feedback loop.

The continuous-time input CM current-feedback loop consists of a CM detector, a window comparator, and current sinking and sourcing blocks. The continuous-time input CM current-feedback loop can clamp the input CM voltage to the saturation region of the input transistor of the current-reused CFIA. After the clamping procedure, the clamped input signal is amplified by the current-reused CFIA. The proposed PLI reduction circuit is also operated in the continuous-time domain, which makes the current-reused CFIA realize an ultra-low power.

The current-reused CFIA has very high input impedance by the current-feedback topology, therefore, it can be robust to signal distortion. In addition, due to the structural characteristics of a fully differential difference amplifier (FDDA), a high CMRR can be achieved. To reduce low frequency noise, such as baseline wander, which is another main source of noise in ECG measurement, an alternating-current (AC)-coupled capacitive feedback loop is implemented in the current-reused CFIA.

The current-reused CFIA implements the inverter-based differential-difference cascode input stage to enable high-power efficiency. The floated class-AB biasing is merged with the input cascode stage; it enables it to achieve high G_m/I_d efficiency. The class-AB output stage in the current-reused CFIA can achieve high load-driving capability and high-power efficiency.

2. Circuit Implementation

A block diagram of the proposed overall structure is shown in Figure 2. The proposed overall circuit consists of the continuous-time input CM current-feedback loop, ECG monitoring channel, and current/voltage (I/V) reference. As low power is an important feature in portable ECG monitoring, the proposed circuit was designed in the sub-threshold region.
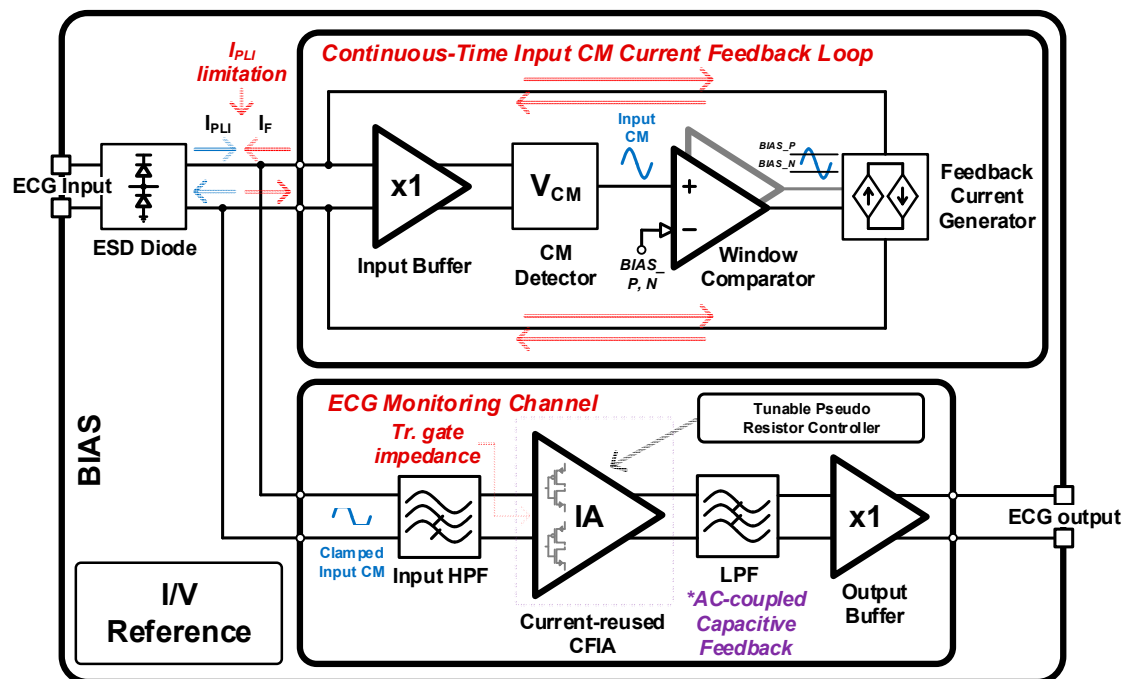

Figure 2. Block diagram of the proposed overall structure.

2.1. The Continuous-Time Input Common-Mode Current-Feedback Loop

A block diagram of the proposed continuous-time CM input current-feedback loop is shown in Figure 3. The proposed circuit is implemented to clamp unwanted PLI in the saturation range of the input transistor, which can normally be amplified by the current-reused CFIA. The main idea of the proposed circuit is that the sourcing and sinking feedback current can limit the input displacement

current caused by PLI if an input CM voltage is out of the bias range between bias voltages, BIAS_P and BIAS_N. Through this procedure, an input CM voltage including PLI is clamped.

2.1.1. Detailed Description and Operating Principle

For clamping PLI, it is essential to detect the input CM voltage. The PLI has sinusoidal 50–60 Hz AC and harmonic components as the PLI is mostly non-sinusoidal. To detect the input CM voltage well within the effective frequency range, including PLI components, a resistive and capacitive voltage divider is implemented as the CM detector.
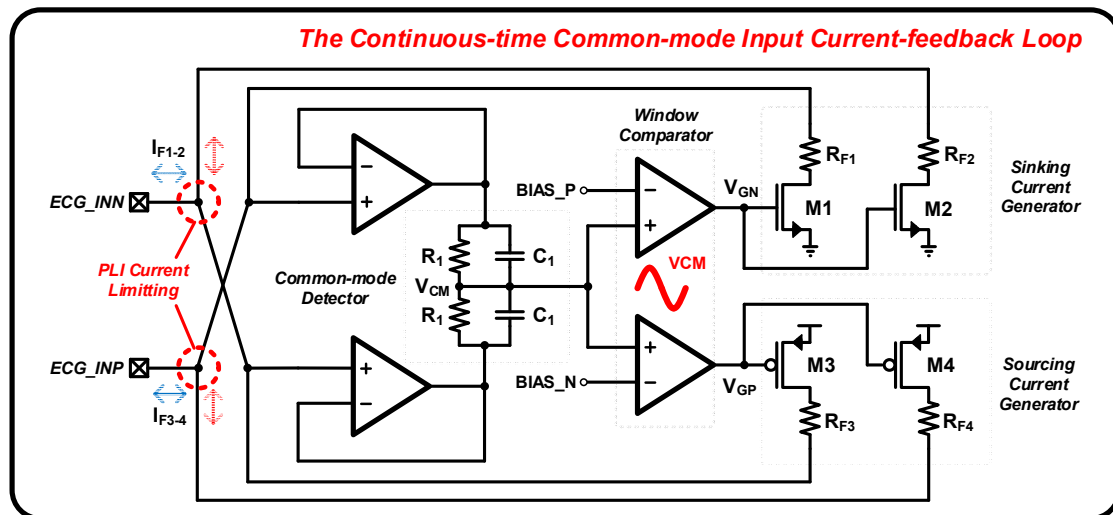

Figure 3. Block diagram of the proposed continuous-time common-mode (CM) input current-feedback loop.

The operating principle of the continuous-time CM input current-feedback loop is shown in Figure 4. The V_{CM} enters the positive input of the two-window comparator. Subsequently, the V_{CM} is compared with a reference value, BIAS_P, and BIAS_N, which is entered as negative input. Reference values can be also chosen as the external voltage within the transistor saturation range by the analog mux. The compared outputs, V_{GN-P}, are connected to the gate node of the negative-channel metal-oxide semiconductor (NMOS) (M1, M2) and the positive-channel metal-oxide semiconductor (PMOS) (M3, M4).
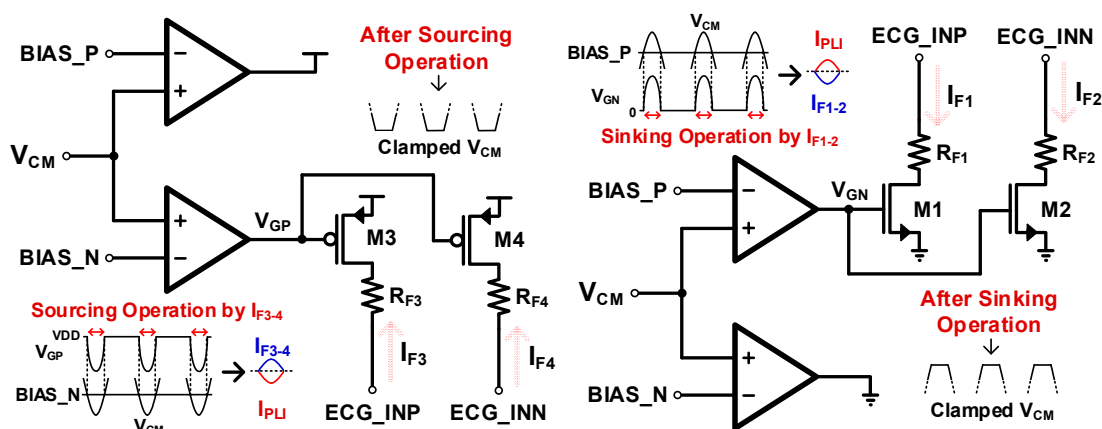

Figure 4. Operating principle of the continuous-time CM input current-feedback loop.

If V_{CM} is over BIAS_P, the feedback sinking current from the NMOS flows into ECG input nodes, ECG_INP and ECG_INN, which leads to I_{F1-2} limitation so that V_{CM} is the same BIAS_P.

Likewise, if V_{CM} is under BIAS_N, the feedback sourcing current from PMOS limits I_{F3-4} so that V_{CM} is the same BIAS_N. In the case that V_{CM} is in a range between BIAS_P and BIAS_N, each $V_{GP, N}$ is determined to ground and supply voltage, which means that all transistors are in the "off" state and cannot flow input feedback current.

The I_{F1-4} can be varied by the skin–electrode contact impedance, dry electrode impedance, and a measurement environment. If I_{F1-4} are larger than the feedback current, V_{CM} cannot be clamped by the proposed feedback loop and can be saturated to supply rails. To prevent the saturation by a large I_{F1-4}, the feedback currents of the proposed feedback loop are controlled by programmable R_F between 11 KΩ and 1.3 MΩ.

Assuming the M1-4 is ideal and has the same transconductance, the transconductance of the output current feedback loop, GM_F, is expressed using the following equation:

$$GM_F = \frac{gm_{M1-4}}{1 + R_F \times gm_{M1-4}}. \tag{1}$$

According to Equation (1), GM_F can be changed using programmable R_F, which means that the feedback current can be adjusted by the R_F. For example, assuming gm_{M1-4} is 50 μA/V, the GM_F can change from 0.7 μA/V to 32.3 μA/V. If the maximum absolute value of I_{F1-4} is 3 μA, the small signal of V_{SGP} and V_{GNS} is 0.5 V and the R_F is 14.3 kΩ, and the maximum absolute feedback current is 3.07 μA, which can lead to limiting I_{F1-4} accordingly.

Good matching of the feedback current is important. If there is a large discrepancy in the feedback current, unwanted differential-mode (DM) components may occur and adversely affect the input signal. Therefore, a careful layout is demanded for the feedback current generator.

Since all of this clamping process of the input CM voltage is part of the continuous-time domain operation, it is not necessary for the ECG amplifier to have a wide bandwidth of more than several kHz.

An input buffer is utilized to isolate electrode impedance and the proposed circuit. The isolation between the electrode and the proposed circuit prevents the loading effect, which can cause signal distortion.

2.1.2. Buffer and Window Comparator

A schematic of an amplifier utilizing a buffer and window comparator is shown in Figure 5.

The amplifier is implemented in three stages in terms of the input range, driving CM detector, and high enough gain. Since the input CM signal can be over the supply rail, the buffer and window comparator must have a wide input range. For this reason, the rail-to-rail input stage is implemented.

In the case of the input buffer, the input buffer must drive the CM detector, and the open-loop gain should be large for high buffer linearity. To gain a heavy load driving capability and high open-loop gain, folded cascode stage merged floated class-AB biasing and a class-AB output stage are implemented.

The phase margin is the key feature in terms of the stability of an amplifier. In the case of a three-stage amplifier, the number of poles is increased, which leads to difficulties in achieving enough phase margin. Since nested miller compensation (NMC) can be a good solution in this case, NMC is implemented in the amplifier.
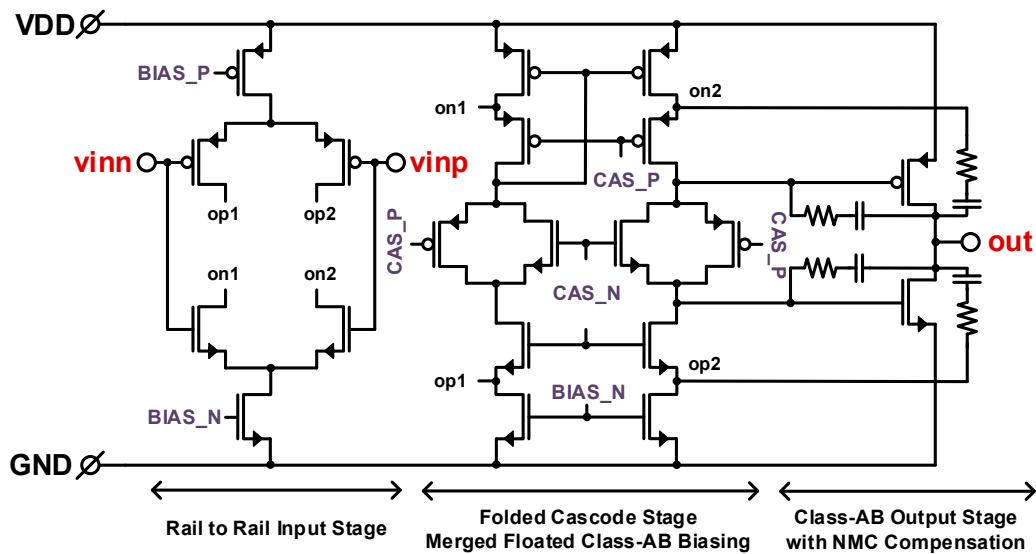
Figure 5. Schematic of the amplifier utilizing a buffer and window comparator.

2.2. ECG Monitoring Channel

A block diagram of the input high pass filter (HPF) and the current-reused CFIA is shown in Figure 6. The input HPF is implemented to reduce the baseline wander. Since baseline wander has a low-frequency noise of less than 1 Hz, the input HPF should be designed to have a cutoff frequency of several Hz, demanding a very large resistance. Considering the HPF design in terms of area, a pseudo-resistor is used in the input HPF due to the fact that it is much less than the area of consumption when compared with a passive resistor with the same resistance value. The input HPF also determines the input reference voltage, VREF.
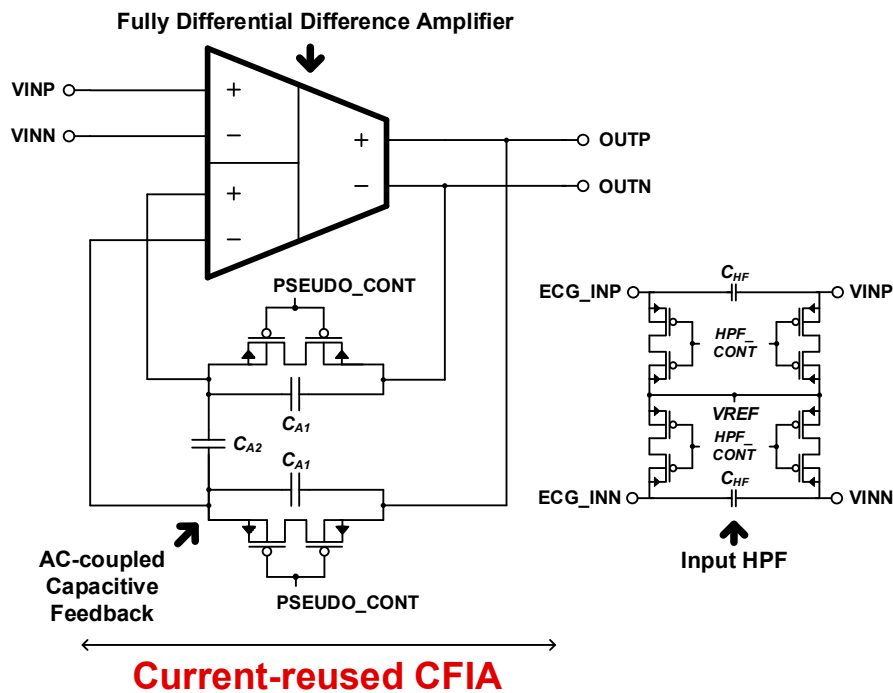

Figure 6. Block diagram of the input high pass filter (HPF) and current-reused current-feedback instrumentation amplifier (CFIA).

The current-reused CFIA has a very high input impedance (more than 10 GΩ) as the CFIA topology receives the input signal as a gate oxide of the input transistor. It is about 20 times larger than the CCIA [11]. Due to the very high input impedance, it is possible for the proposed CFIA to achieve a high CMRR and to prevent signal distortion.

The current-reused CFIA also adopts the AC-coupled capacitive feedback loop connected to the fully differential difference amplifier (FDDA). The capacitive feedback is not only amplification, but also has an HPF function, which can help to eliminate the residual baseline wander. The lower cutoff frequency of the feedback loop is controlled by the voltage of current bias, PESUDO_CONT, connected to the gate of the tunable pseudo resistor.

Assuming the FDDA is ideal, the closed-loop gain by the capacitive feedback is expressed using the following equation:

$$\text{closed loop gain} \approx \frac{2 \times C_{A2}}{C_{A1}} + 1. \tag{2}$$

The FDDA in the Current-Reused CFIA

A detailed schematic of the FDDA in the current-reused CFIA is shown in Figure 7.

The current-reused CFIA adopts an inverter-based differential-difference cascode input stage combined with floating class-AB biasing. To gain the driving capability of the capacitive feedback load and a wide output range with high-power efficiency, a class-AB output stage is implemented. To ensure to stability, NMC is adopted. In the fully differential output structure, the output CM voltage should be V_{REF} to enable a high CMRR and a wide output range. To maintain the output CM voltage at V_{REF}, a common-mode feedback (CMFB) circuit is adopted.
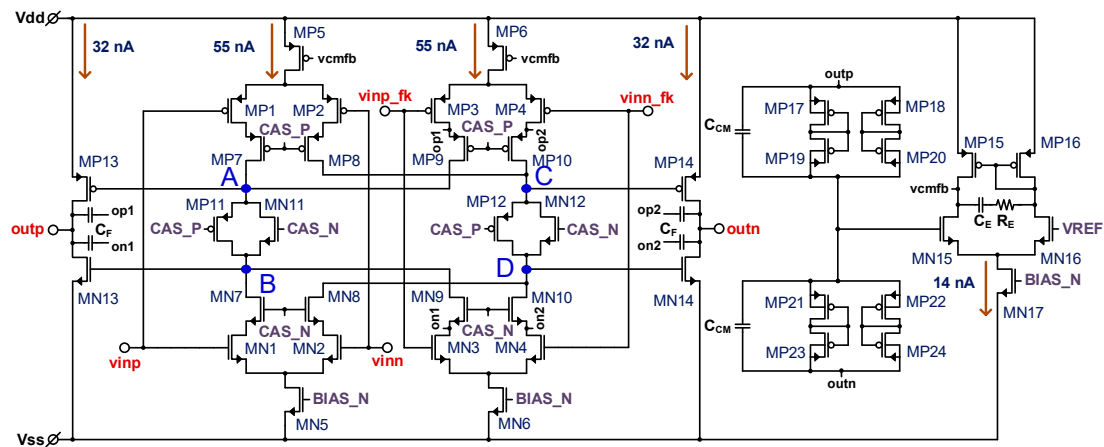

Figure 7. Detailed schematic of the fully differential difference amplifier (FDDA) in the current-reused CFIA.

The inverter-based differential-difference cascode input stage is cooperatively biased by the current sources MP_{5-6} and MN_{5-6}. After biasing, the trans-conductances of the stacked NMOS and PMOS differential input pair are merged, which leads to amplification of the input signal with high G_m/I_d efficiency. In addition, the cascode amplifiers MN and P_{7-10} are implemented to obtain high open-loop gain by increasing the impedance at nodes A–D. Assuming symmetric elements have the same small signal parameter, the impedance at nodes A–D is briefly expressed using the following equation:

$$R_{A-D} \approx \frac{gm_{p11}}{gm_{n11}} \times \frac{gm_{p,n7} \times r_{op,n1} \times r_{op,n7}}{2}. \tag{3}$$

When $gm_{P11} = gm_{N11}$, Equation (3) can be re-expressed as the following equation:

$$R_{A-D} \approx \frac{gm_{p,n7} \times r_{op,n1} \times r_{op,n7}}{2}. \tag{4}$$

Equation (4) shows that the cascode amplifier leads to an increase in the impedance of nodes A–D.

To express the closed-loop gain using open-loop gain, the feedback input voltage vinp_fk and vinn_fk can be expressed by the following equation using Equation (2):

$$\text{vinp}_{fk} - \text{vinn}_{fk} = -\frac{C_{A1}}{2C_{A2} + C_{A1}} \times (\text{outp} - \text{outn}) \tag{5}$$

$$A_{FC} = \frac{\text{vinp}_{fk} - \text{vinn}_{fk}}{\text{outp} - \text{outn}} = -\frac{C_{A1}}{2C_{A2} + C_{A1}}. \tag{6}$$

Using Equation (6), Equation (2) is briefly re-expressed using following equation:

$$\text{closed loop gain} = \frac{\left(\text{gm}_{p1} + \text{gm}_{n1}\right) \times \left(\text{gm}_{p13} + \text{gm}_{n13}\right) \times r_{o13} \parallel r_{o14} \times R_A \parallel R_B}{1 - A_{FC} * \left(\text{gm}_{p1} + \text{gm}_{n1}\right) \times \left(\text{gm}_{p13} + \text{gm}_{n13}\right) \times r_{o13} \parallel r_{o14} \times R_A \parallel R_B}. \tag{7}$$

3. Simulation Results

Simulated Results Using the Equivalent Circuit Model for a Dry Electrode–Skin Interface

A photograph of the layout of the proposed circuit is shown in Figure 8. The proposed circuit was designed using 0.18-μm bipolar-complementary metal semiconductor–double-diffused metal oxide semiconductor (BCDMOS) technology. The active area of the proposed circuit is 1.8 mm^2.
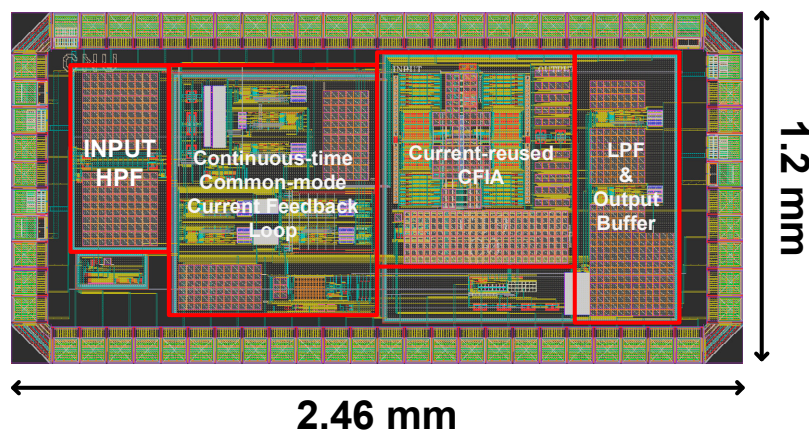

Figure 8. A photograph of the layout of the proposed circuit.

A simulation of the setup for ECG monitoring that considers dry electrode–skin contact is shown in Figure 9. For simulation of the ECG monitoring, an ECG/PLI signal generator, a capacitive coupling for PLI, and an equivalent circuit model of the dry electrode–skin interface were used [14]. The word "subcutan" expressed in Figure 9 is a shortened form of "subcutaneous".

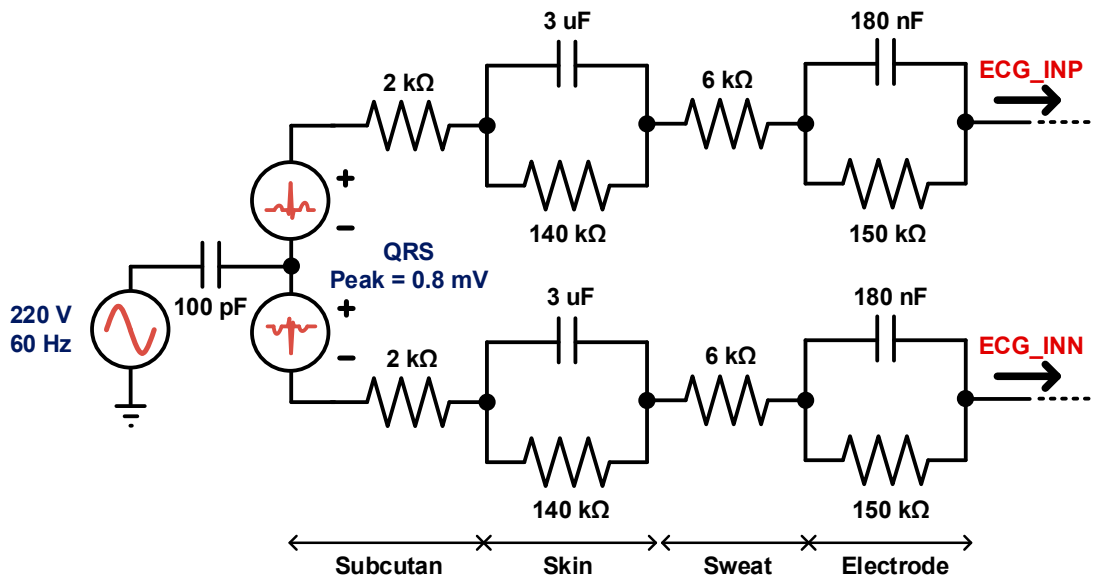The simulated total power consumption is 18 μW and the current-reused CFIA consumes only 185 nA.

Figure 9. Simulated setup for ECG monitoring considering dry electrode–skin contact.

Simulated results of the transient response at the ECG input and the differential output with and without the proposed PLI reduction circuit are shown in Figure 10. The gain of the current-reused CFIA is 40.55 dB. Figure 10a shows the raw ECG signal, including PLI with or without the proposed PLI reduction circuit. Without the proposed PLI reduction circuit, the saturation effect of the ECG input is caused by the PLI through the ESD diode.

However, with the proposed PLI reduction circuit, the ECG input is clamped with BIAS_P and BIAS_N, and the saturation effect does not occur. Figure 10b shows the amplified ECG signal by the current-reused CFIA according to the presence or absence of the proposed PLI reduction circuit. Abnormal ECG amplification occurs when the proposed PLI reduction circuit does not exist, but if the proposed PLI reduction circuit does exist, normal ECG amplification is possible.

Simulated results of the input-referred noise of the current-reused CFIA are shown in Figure 11. The input-referred root mean square (RMS) noise of the current-reused CFIA has 2.68 μV_{RMS} with the 107 Hz of bandwidth.
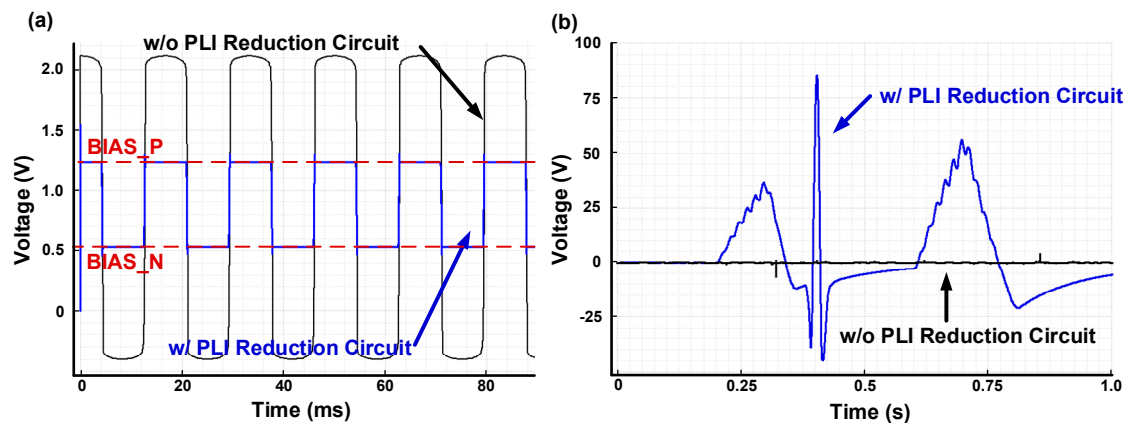

Figure 10. Simulated results of the transient response at the ECG input and output node before and after PLI clamping: (**a**) the ECG input voltage including PLI, (**b**) the output differential voltage amplified by the current-reused CFIA.
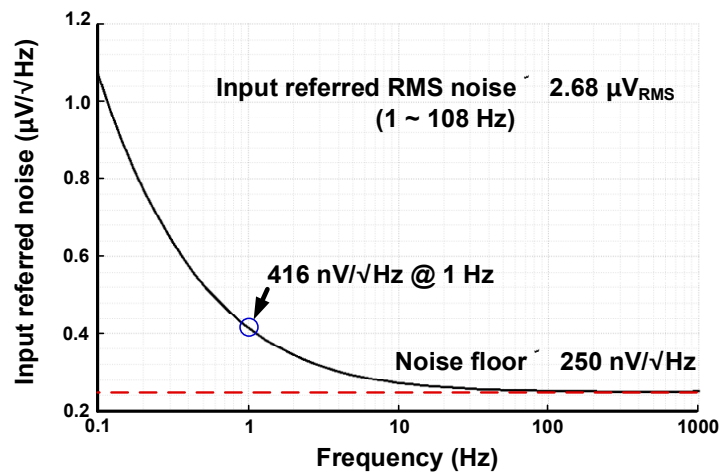
Figure 11. Simulated results of the input-referred noise of the current-reused CFIA.

Simulated results of the CMRR of the current-reused CFIA are shown in Figure 12. The measured CMRR is above 105 dB, and the mid-band gain measures 40.5 dB with a bandwidth of 107 Hz.
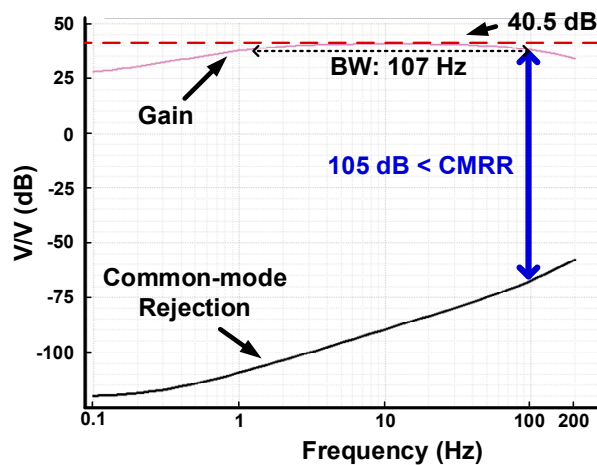

Figure 12. Simulated results of the gain and common-mode rejection ratio (CMRR) of the current-reused CFIA.

A performance summary and comparison of the proposed circuit is shown in Table 1.

Table 1. Performance summary and comparison.

	Parameter	This Work	Ref. [9]	Ref. [10]	Ref. [11]	Ref. [13]
	Supply voltage	1.8 V	1.2 V	1 V	1.3–1.8 V	2 V
	Technology	0.18 μm	0.18 μm	0.065 μm	0.18 μm	0.35 μm
	Power consumption	18 μW	27.8 μW	2.1 μW	680 nA	320 nW
	PLI limiting	Yes	Yes	No	No	No
	Type	CFIA	CCIA	CCIA	CCIA	CCIA
	Input impedance	>10 GΩ [1]	-	20–80 MΩ	>400 MΩ	20 MΩ
	Current consumption	185 nA	-	2.1 μA	150 nA	160 nA
IA	Mid-band gain	40.5 dB	35 dB	40 dB	-	39.8 dB
	Bandwidth	107 Hz	100 Hz	100 Hz	130 Hz	200 Hz
	Input-referred RMS noise	2.68 μV$_{RMS}$ (1–108 Hz)	5.05 μV$_{RMS}$ (1–100 Hz)	6.7 μV$_{RMS}$ (0.5–100 Hz)	4.9 μV$_{RMS}$ (1–130 Hz)	2.05 μV$_{RMS}$ (0.1–10 kHz)
	CMRR	>105 dB	68 dB	100–110 dB	90 dB	>65 dB
	NEF [2]	4.28	-	37.3	-	2.26

[1] Estimated gate oxide impedance, [2] NEF = Vni * $\sqrt{(2 \cdot Itot/\pi \cdot UT \cdot 4kT \cdot BW)}$.

4. Discussion

As mentioned in the introduction, the PLI is mainly generated by the displacement current between a human body and an AC power line. If a mismatch exists between the contact impedance of two skin electrodes, a potential divider effect occurs. The difference in impedance between the skin electrodes converts the PLI into an unwanted DM component. In this case, not even an amplifier with an infinitely high CMRR will make any difference. To minimize this problem, a user should carefully consider a skin–electrode contact impedance between electrodes.

5. Conclusions

This paper proposes a power line interference reduction technique with a current-reused current-feedback instrumentation amplifier for ECG recording. The proposed PLI reduction circuit can be a solution to prevent abnormal amplification of ECG amplifiers by ESD diode saturation caused by excessive PLI. As the proposed PLI reduction circuit clamps the input CM voltage within the saturation range of the amplifier's input transistor, the proposed ECG monitoring circuit can be robust to an excessive PLI. Also, the proposed current-reused CFIA has a higher input impedance (10 GΩ) compared with the CCIA used for conventional ECG monitoring, so it is robust against signal distortion. The proposed current-reused CFIA achieves a CMRR of over 105 dB. The input-referred RMS noise with a bandwidth of 107 Hz and NEF achieves 2.68 μV_{RMS} and 4.28, respectively. The proposed overall circuit is designed with BCDMOS technology and the total power consumption and active area are 18 μW and 1.8 mm^2, respectively.

Author Contributions: Conceptualization and supervision, H.K. (Hyoungho Ko); investigation and writing—original draft preparation, D.Y.; writing—review and editing, H.H., H.K. (Hyungseup Kim), Y.K., and S.L. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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