

Review

Development of an Epitaxial Growth Technique Using III-V on a Si Platform for Heterogeneous Integration of Membrane Photonic Devices on Si

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Featured Application: Optical interconnects for data centers.



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Abstract: The rapid increase in total transmission capacity within and between data centers requires the construction of low-cost, high-capacity optical transmitters. Since a tremendous number of transmitters are required, photonic integrated circuits (PICs) using Si photonics technology enabling the integration of various functional devices on a single chip is a promising solution. A limitation of a Si-based PIC is the lack of an efficient light source due to the indirect bandgap of Si; therefore, hybrid integration technology of III-V semiconductor lasers on Si is desirable. The major challenges are that heterogeneous integration of III-V materials on Si induces the formation of dislocation at high process temperature; thus, the epitaxial regrowth process is difficult to apply. This paper reviews the evaluations conducted on our epitaxial growth technique using a directly bonded III-V membrane layer on a Si substrate. This technique enables epitaxial growth without the fundamental difficulties associated with lattice mismatch or anti-phase boundaries. In addition, crystal degradation correlating with the difference in thermal expansion is eliminated by keeping the total III-V layer thickness thinner than ~350 nm. As a result, various III-V photonic-device-fabrication technologies, such as buried regrowth, butt-joint regrowth, and selective area growth, can be applicable on the Si-photonics platform. We demonstrated the growth of indium-gallium-aluminum arsenide (InGaAlAs) multi-quantum wells (MQWs) and fabrication of lasers that exhibit >25 Gbit/s direct modulation with low energy cost. In addition, selective-area growth that enables the full O-band bandgap control of the MQW layer over the 150-nm range was demonstrated. We also fabricated indium-gallium-arsenide phosphide (InGaAsP) based phase modulators integrated with a distributed feedback laser. Therefore, the directly bonded III-V-on-Si substrate platform paves the way to manufacturing hybrid PICs for future data-center networks.

Keywords: epitaxial growth; direct bonding; semiconductor lasers; silicon photonics; photonic integrated circuits (PICs)

1. Introduction

Increased data transmission between and within data centers requires high-capacity and low-cost optical links. To meet the requirement for a tremendous number of photonic components for such short-distance applications, the integration of various photonic devices into a single chip becomes key because the assembly process can be dramatically simplified. Therefore, photonic integrated circuits (PICs) using Si photonics technology are

promising because mature complementary-metal-oxide-semiconductor (CMOS) fabrication technology enables the integration of various optical devices into a compact chip [1–10]. A limitation of a Si-photonics-based PIC is the lack of a reliable, efficient and low-power-consumption light source due to its indirect bandgap. Accordingly, the integration of direct-bandgap III-V semiconductors on Si is desirable. In particular, indium phosphide (InP) and its related materials are widely used for developing high-performance optical transmitters such as directly modulated lasers (DMLs), electro-absorption modulator-integrated distributed feedback (EADFB) lasers and Mach-Zehnder modulators (MZMs) [11–18]. Therefore, several hybrid integration techniques are used to develop III-V/Si hybrid PICs [4,19–22].

Among the hybrid integration techniques, direct epitaxial growth of III-V materials on a Si substrate has been attracting much attention for over 30 years because it is the most promising technique in terms of cost and scalability. However, there are fundamental difficulties that limit crystal quality such as differences in lattice constant, differences in the coefficient of thermal expansion (CTE), and the formation of anti-phase boundaries (APBs). In 1990, Sugo et al. demonstrated the room-temperature (RT) operation of indium-gallium-arsenide phosphide (InGaAsP) lasers directly grown on a Si substrate [23]. However, a buffer layer thicker than 15 μm was required, making them difficult to optically connect to Si-photonics devices. Much effort has been made to improve the crystal quality of multi-quantum wells (MQWs) with thinner buffer layers [24,25]. In addition, III-V quantum dot (QD) lasers directly grown on a Si substrate that exhibit >100 mW optical output power have been demonstrated [26,27]. This can be achieved because QDs are insensitive to threading dislocations (TDs) compared with QWs. However, these “blanket” epitaxial growth techniques still require a thick buffer layer (typically >2 μm). In contrast, direct selective epitaxy using defect filtering with selective-area growth masks enable the integration of high-quality III-V layers on a Si substrate without requiring a thick buffer layer [28–32]. Using the defect filtering method, various lasers with optical pumping have been demonstrated. On the other hand, electrically driven lasers that can emit output power required for data-center application have yet to be reported. This seems to correlate with the difficulty of growing ternary and quaternary compound materials, such as indium-gallium arsenide (InGaAs), InGaAsP, and indium-gallium-aluminum arsenide (InGaAlAs), because the crystal composition of these materials depends on both the mask structure and distance from the mask edge [33]. In addition, the structural limitation of the III-V device layer due to the selective-area growth masks makes it difficult to fabricate a *p-i-n* junction, which is necessary for current injection.

Direct- and adhesive-bonding techniques are another possible solution to achieve wafer-scale heterogeneous integration because bonding prevents the formation of TDs and APBs in III-V layers [34,35]. By using direct bonding of III-V active layers, III-V/Si hybrid lasers that have III-V active regions optically connected to Si waveguides have been demonstrated [36–38]. In addition, micro-transfer-printing has attracted attention as a promising means to integrate III-V optical devices on Si-photonics components [19,39–41]. This is because it enables the manipulation of micron-size III-V layer coupons on a donor III-V substrate, and the substrate can be used repeatedly. With these bonding techniques, III-V/Si hybrid PICs have been demonstrated and the directly bonded III-V lasers exhibit sufficient optical output power as a continuous wave light source for Si-photonics modulators. As transmitters for data-center application, however, the footprint and power consumption of DMLs on a Si substrate should be further improved. This is due to a lack of epitaxial regrowth in III-V/Si bonding; an InGaAlAs/InP or InGaAsP/InP buried-heterostructure (BH) fabricated by epitaxial regrowth of InP is essential for reliable, low-power-consumption DMLs because a BH enables high optical- and carrier-confinement into the active region [42,43].

Consequently, direct bonding of III-V membrane layers on a Si substrate followed by epitaxial regrowth of InP-based material is an effective technique [44–52]. This technique overcomes the problems with direct epitaxial growth and bonding techniques. In terms

of epitaxial growth, a III-V membrane layer on Si as an epitaxial template prevents lattice mismatching and APBs. Regarding device fabrication, the capability of epitaxial growth on Si offers high flexibility of the III-V device design. In particular, it enables the integration of different III-V mediums on the same plane such as BHs, butt-joint (BJ) structures [15,53], and multi-wavelength gain structures. However, most studies suffered from the strain induced by the mismatch of the CTE, and threading dislocation densities (TDDs) of epitaxial layers are not as low as those of a standard InP substrate ($<1 \times 10^4/\text{cm}^2$). This is because the thickness of the total III-V layer after regrowth is thicker than the critical thickness, which is determined by the product of temperature change and mismatch of CTE between Si and InP. It is calculated to be ~ 430 nm when we assume the bonding temperature and epitaxial growth temperature are 200 and 600 °C, respectively [46,54], which is much thinner than the total thickness of typical InP-based lasers with vertical *p-i-n* structure for electrical pumping.

In this context, we developed an epitaxial growth technique that uses an InP membrane layer formed on a Si substrate for lateral *p-n* or *p-i-n* membrane structure. Since we keep the total III-V thickness less than the critical thickness determined by the thermal strain throughout the process, a superior-quality III-V epitaxial layer that has a TDD as low as the standard InP substrate can be achieved. In this paper, we discuss the evaluations on epitaxial growth technique and lasers fabricated using a III-V membrane on a Si-based substrate. Section 2 first describes our integration procedure to obtain high-quality III-V membrane photonic devices on a Si substrate. After discussing the critical thickness of the III-V membrane on a Si substrate at the epitaxial growth temperature, the crystal quality of epitaxial grown InP and InGaAlAs is evaluated in detail. Section 3 provides the detailed characteristics of membrane lasers, including an InGaAlAs DML array on Si fabricated using epitaxial grown MQWs on an InP-on-insulator substrate. In addition, recent efforts to integrate multi-bandgap III-V photonic devices using epitaxial growth on the Si-photonics platform, such as a wide-wavelength-range laser array and InGaAsP-MZM integrated with a DFB laser, are reported.

2. Epitaxial Growth on InP-on-Insulator Substrate

For III-V/Si hybrid integration, the crystal quality of the III-V layer after heterogeneous integration is important. To achieve high crystal quality, several low-temperature bonding techniques that enable stable and strong bonding at annealing temperatures below 400 °C were developed. Compared to conventional high-temperature fusion bonding, they enable significant improvements in crystal quality of the III-V layer, resulting in high-performance hybrid PICs. On the other hand, to avoid thermal degradation, process temperatures higher than 400 °C are still prohibitive after bonding, meaning that the epitaxial regrowth of III-V material cannot be carried out on a Si substrate.

High-quality epitaxial growth has recently become possible by limiting the total III-V layer thickness. We focus on how epitaxial growth on a III-V-on-insulator substrate is achieved.

2.1. Integration Method of III-V Photonic Devices on Si

Figure 1 shows the process flow of fabricating membrane photonic devices on Si using epitaxial growth technique on III-V-on-insulator platform. The process begins with the epitaxial growth of a III-V epitaxial layer including InP membrane layer and InGaAs etch-stop layer on standard InP substrate. Next, the epitaxial InP wafer and a Si wafer are bonded. Then, the InP membrane layer is left on the SiO₂ layer by removing the InP substrate and InGaAs etch-stop layer (InP-on-insulator substrate). After that, a III-V active layer such as InGaAsP/InGaAsP- or InGaAlAs/InGaAlAs-MQW double-heterostructure (DH) sandwiched between the InP layer is grown on InP-on-insulator substrate as an active region for photonic devices. The MQW-DH is then etched by dry- and selective wet-etching, which leaves an InP layer except for under the SiO₂ mask (mesa-stripe). After that, undoped InP is selectively grown on the InP membrane to fabricate the BH, which

enables high optical- and carrier-confinement into the active region. Finally, formation of the lateral *p-i-n* or *p-n* junction and metallization are carried out to fabricate the membrane photonic devices.

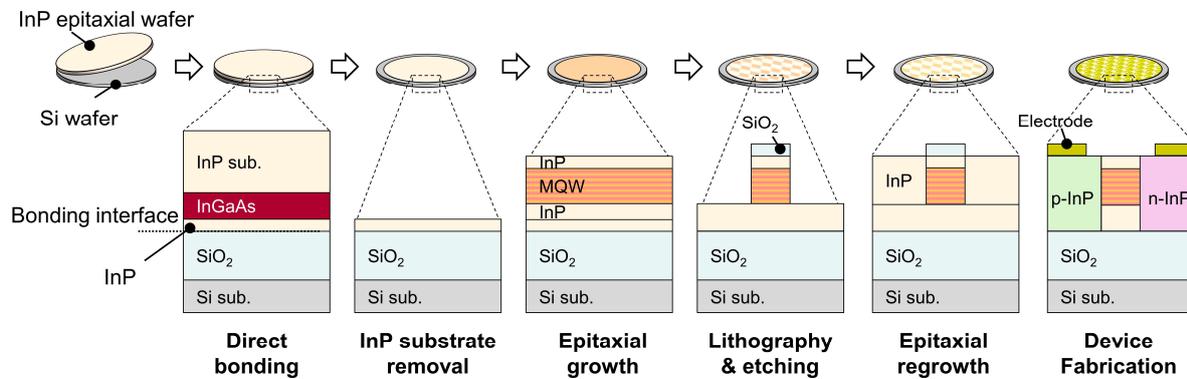


Figure 1. Process flow of fabricating membrane photonic devices on Si using epitaxial growth technique on a III-V-on-insulator platform.

2.2. Assessment of Thermal Strain at Epitaxial Growth Temperature

To grow a high-quality epitaxial layer using a III-V/Si integrated substrate, the total III-V layer thickness is critical [46]. This subsection describes the calculation model of the critical thickness of the InP layer on an InP-on-insulator substrate. Since the process temperature of metalorganic vapor phase epitaxy (MOVPE) for InP-based materials is about 600 °C, the difference of the CTEs between InP-based materials and SiO₂/Si causes thermal strain. Thermal strain ϵ is given by the product of the difference between the CTEs $\Delta\alpha$ and temperature change ΔT . The CTEs of Si and InP at 25 °C are 2.62 and 4.56 ppm/K, respectively [55]. For simplification, we disregard the SiO₂ layer because it is much thinner (typically 2 μm) than the Si substrate. Since we apply pressure to the bonded wafer at 200 °C, we assume that the directly bonded InP membrane layer is free standing at 200 °C. On the basis of the above, epitaxial growth temperature (600 °C) induces a compressive strain of approximately 780 ppm to the InP membrane layer on Si.

Next, the critical thickness was calculated based on the thermal strain applied at epitaxial growth temperature. When the total InP-based layer is thicker than the critical thickness, a dislocation should be generated in both the original InP membrane and regrown layer, resulting in degradation of photoluminescence (PL) and electroluminescence characteristics. There are two types of models to calculate critical thickness, mechanical equilibrium models and strain–energy–density equilibrium models. The thickness at which the dislocations appear in the actual strained crystal tends to be between the critical thicknesses calculated using these models [56].

Figure 2 compares the critical thickness versus strain calculated using one of each type of calculation model. The mechanical equilibrium model expresses the critical thickness h_c as follows [57]:

$$h_c = \frac{b(1-\nu/4)}{4\pi f(1+\nu)} \left(\ln \frac{h_c}{b} + 1 \right), \quad (1)$$

where ν is Poisson's ratio for strained material, b is Burger's vector of dislocation, and f is strain. On the other hand, the strain–energy–density equilibrium model expresses the critical thickness as follows [54]:

$$h_c = \frac{\sqrt{6}b(2-\nu)}{8\sqrt{3/2}\pi f(1+\nu)} \left\{ \ln \left(\frac{8\sqrt{3/2}ah_c}{b} \right) - 2 \right\}, \quad (2)$$

where a is a parameter that is related to the dislocation energy (typically $a \sim 4$). On the basis of the two models, the critical thickness of InP on a SiO₂/Si substrate is calculated to

be between approximately 200 nm (mechanical equilibrium model) and 430 nm (energy equilibrium model) for a thermal strain of about 800 ppm. Therefore, high-temperature MOVPE growth should not induce the formation of dislocation even though the III-V/Si hybrid substrate is used, unless the InP membrane thickness after the growth exceeds 200 or 430 nm.

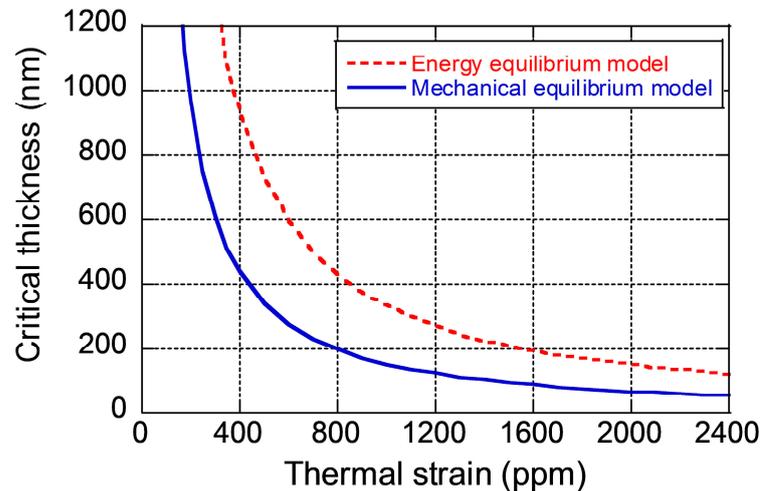


Figure 2. Strain dependence on calculated critical thickness of indium phosphide (InP) directly bonded on Si.

To experimentally evaluate the critical thickness, we fabricated III-V membranes that are bonded to SiO₂/Si substrates [46]. Figure 3a shows the process flow. The fabrication began with the epitaxial growth of an InP buffer layer, InGaAs etch-stop layer (100 nm), and MQW double-heterostructure (DH) sandwiched between the InP layer on a 2-inch standard InP (001) substrate by MOVPE. The growth was undertaken at 630 °C and 6.7 kPa, and the precursors for In, Ga, As and P were trimethyl-indium (TMI), triethyl-gallium (TEG), arsine (AsH₃) and phosphine (PH₃), respectively. The DH included six-period strained InGaAsP MQWs (PL peak wavelength: 1520 nm). The epitaxial InP wafer and a 2-inch Si (001) wafer with a 2- μ m-thick thermal silicon dioxide (SiO₂) layer (SiO₂/Si substrate) were treated with oxygen plasma. This process grew the ultra-thin oxide layer, which makes the bonding surface very smooth and hydrophilic [58]. The wafers were then directly bonded at RT under atmospheric pressure. After that, post-annealing was carried out at 200 °C while pressure from 1.0 to 6.1 MPa was applied. To leave the InP-based membrane layers on the SiO₂ layer, the InP substrate side was mechanically polished and chemically etched using the InGaAs etch-stop layer [59]. Finally, the InGaAs etch-stop layer was chemically etched to obtain a 250-nm-thick MQW-DH on the SiO₂ layer. Figure 3b shows a typical PL intensity maps for the 250-nm-thick MQW-DH on the SiO₂/Si substrate at 25 °C, measured with the excitation laser irradiation at a wavelength of 980 nm. The PL intensity distribution was very uniform (standard deviation: 1.31%), excluding the peeled region at the wafer edge.

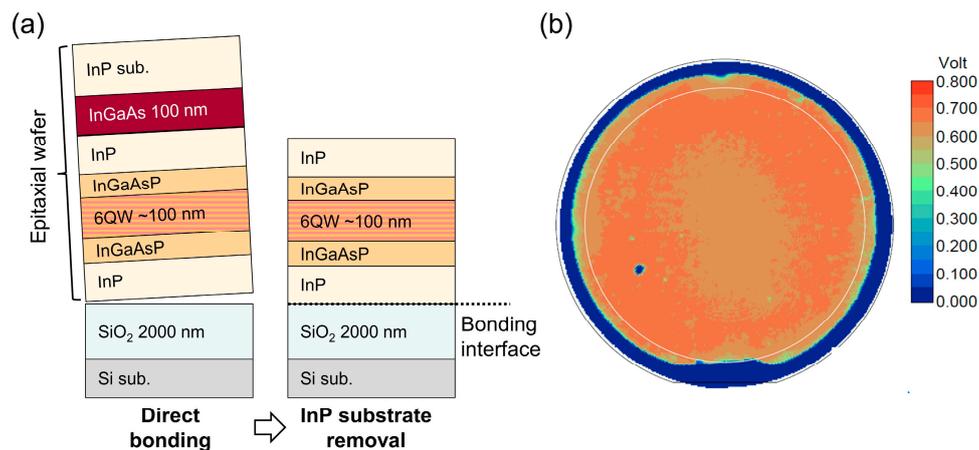


Figure 3. (a) Process flow of fabricating a multi-quantum well (MQW)-double-heterostructure (DH) on SiO_2/Si substrate; (b) photoluminescence (PL) intensity map for 2-inch 250-nm-thick MQW-DH transferred to SiO_2/Si substrate.

Next, we prepared three MQW-DHs on SiO_2/Si substrate with various III-V layer thicknesses and characterized their PL before and after 610°C annealing (epitaxial regrowth temperature). The three epitaxial wafers included almost the same MQWs, but the total III-V layer thicknesses were varied from 250 to 850 nm. We annealed these wafers in an MOVPE reactor for 30 min under the PH_3 -atmosphere epitaxial-regrowth condition. The temperature was 610°C and the pressure was 4.0 kPa. Figure 4a–c compares the PL spectra before (solid lines) and after (dashed lines) the MOVPE annealing for the samples with three different thicknesses, respectively. The median PL intensity for the wafer with a total thickness of 250 nm degraded only 8% after annealing. In contrast, for samples with total thicknesses of 500 and 850 nm which are thicker than the critical thicknesses calculated with the two models, degradation increased to 31 and 68%, respectively. To evaluate the degradation in the epitaxial wafers, we also evaluated the PL-intensity map with a PL microscope that can visualize dislocations and clacks. Figure 4d–f compares the PL-intensity distributions measured with PL microscope for these three samples. They clearly show that there were neither dark line nor dark spots in the $100 \times 100 \mu\text{m}^2$ area for the 250-nm-thick sample, whereas dark lines were observed for the 500- and 850-nm-thick samples [46]. We also confirmed that a dark line did not appear when the total III-V thickness was 350 nm [60]. These results clearly show that the actual critical thickness for an InP-based membrane layer on a Si substrate at 610°C should be between 350 and 500 nm; therefore, epitaxial regrowth using an InP-on-insulator substrate should not induce dislocation when the total III-V thickness is less than 350 nm.

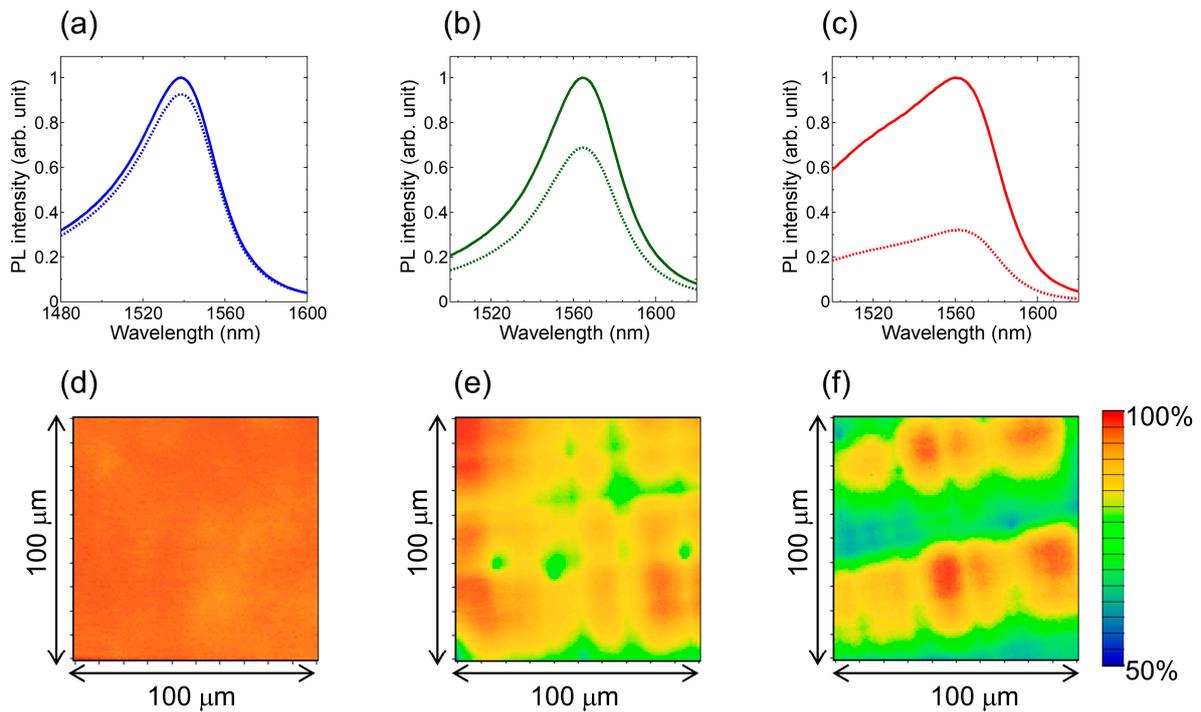


Figure 4. (a–c) PL spectra for MQW-DHs with different total thicknesses on SiO₂/Si substrates before (solid lines) and after (dashed lines) annealing; (d–f) PL-intensity map measured with PL microscope after annealing.

2.3. Regrowth of InP

The epitaxial regrowth of InP on an InP-on-insulator substrate is an important process because it enables the fabrication of a BH on a SiO₂/Si substrate, which makes it possible to integrate low-power-consumption-membrane optical devices on a Si substrate. Figure 5a–c shows the process flow of fabricating a BH. First, an MQW-DH was grown on standard InP substrate and transferred to thermally oxidized Si substrate by using a direct bonding technique. Next, a SiO₂ layer was deposited using plasma-enhanced chemical vapor deposition (p-CVD). An ~800-nm-wide SiO₂ mask was formed using lithography and reactive ion etching (RIE). The MQW-DH was then etched by dry- and selective wet-etching, which leaves a 50-nm-thick InP layer except for under the SiO₂ mask (mesa-stripe) [59,61,62]. After that, undoped InP was grown on the InP membrane, except for the SiO₂ mask, to fabricate the InGaAsP/InP BH. The epitaxial growth temperature was 610 °C and the pressure was 4.0 kPa. The growth rate was ~0.4 μm/h. Figure 5d shows a cross-sectional scanning electron microscope (SEM) image of a BH on the SiO₂/Si substrate. The 150-nm-thick and 800-nm-wide active region was successfully buried in InP. Figure 5e shows an atomic force microscope (AFM) image of the surface of a regrown InP layer on a SiO₂/Si substrate. Clear atomic steps were observed, and the root-mean-square roughness was 0.22 nm, which are comparable to the surface morphology of a standard InP epitaxial layer on an InP substrate.

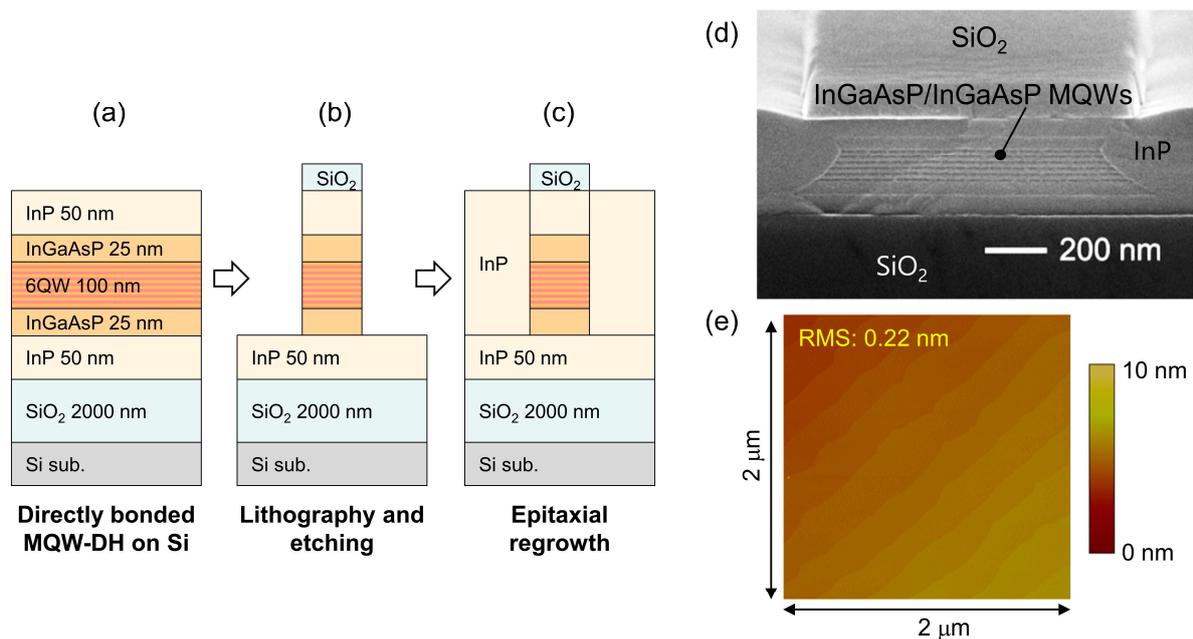


Figure 5. (a–c) Process flow of fabricating buried-heterostructure (BH) using MQW-DH on SiO₂/Si substrate; (d) cross-sectional SEM image of BH on SiO₂/Si substrate; (e) atomic force microscope (AFM) image of surface of InP membrane on SiO₂/Si substrate after epitaxial growth.

2.4. Growth of Multi-Quantum-Well Double-Hetero Structure

To integrate III-V photonic devices with different bandgap active regions on a Si substrate, the growth of a ternary or quaternary compound semiconductor is also necessary. In particular, a strained MQW is widely used as an active region for state-of-the-art DMLs and electro-absorption modulators [63–66]. We demonstrated the growth of MQWs on InP-on-insulator followed by epitaxial regrowth of InP to fabricate a BH, by keeping the total thickness to less than 350 nm. We prepared an InP-on-insulator substrate that includes 50-nm-thick InP membrane layer by direct bonding. Then, a 120-nm-thick InP buffer layer, 6-period MQW, and 30-nm-thick InP cap layer were grown on it. Both InGaAsP/InGaAsP and InGaAlAs/InGaAlAs have been demonstrated as MQW material [47,67,68]. The growth temperature was estimated to be around 630 °C, and the pressure was about 6.7 kPa under hydrogen carrier gas. The precursors for In, Ga, Al, As, and P were TMI, TEG, trimethyl-aluminum, AsH₃, and PH₃, respectively. The epitaxial layer quality was characterized by PL measurements. Figure 6a compares the PL spectra of an InGaAlAs MQW grown on an InP-on-insulator substrate and the same MQW grown on a standard InP substrate as a reference. To achieve high crystal quality, we controlled the residual strain in the MQW on InP-on-insulator substrate to be -680 ppm (tensile), which almost cancels the compressive thermal strain induced at the growth temperature [47,69]. The peak PL intensity of the MQW grown on the InP-on-insulator substrate was 7.2 times greater than that of the reference grown on the InP substrate because both the excitation and collection efficiency of PL were enhanced due to the underlying InP/SiO₂/Si interfaces [46,51]. The slightly broadened full width at half maximum of the PL (30.0 to 33.4 meV) seems to be because of the higher excitation energy density, and there were no significant differences for spectral shapes or peak PL wavelength. Figure 6b shows the PL-intensity map measured with a PL microscope. The PL intensity was uniform and there were neither dark spots nor dark lines over the 500 × 500 μm² area, corresponding to a TDD of less than 4.0 × 10²/cm². After the growth of the MQW on the InP-on-insulator substrate, the BH was formed using epitaxial regrowth of undoped InP. Figure 6c shows the PL-intensity map of an 80-μm-long and ~0.8-μm-wide MQW-BH after regrowth of the InP layer. The PL intensity was very

uniform in the active region. These PL characteristics clearly represent the superior quality of the MQW, although the growth was carried out on an InP-on-insulator substrate.

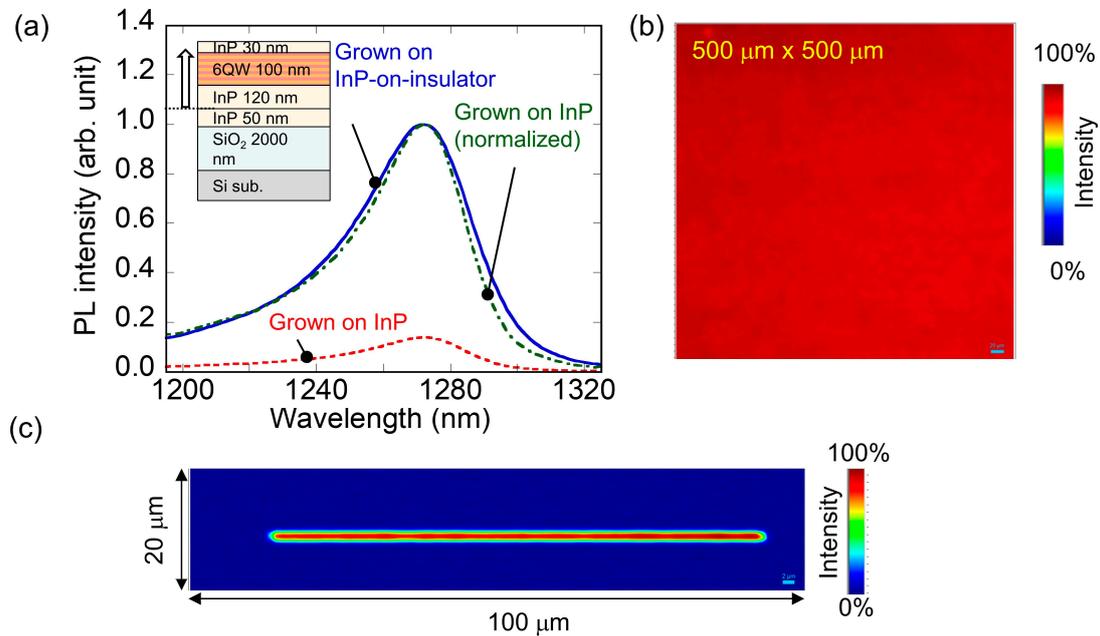


Figure 6. (a) PL spectra of indium-gallium-aluminum arsenide (InGaAlAs) MQW grown on InP-on-insulator substrate and same MQW grown on standard InP substrate; (b) PL-intensity map for MQW grown on InP-on-insulator substrate measured with PL microscope; (c) PL intensity-map for MQW-BH after regrowth of InP layer.

To structurally evaluate the MQW-BH on the InP-on-insulator substrate, we carried out transmission electron microscope (TEM) observation. Figure 7a shows a cross-sectional bright-field scanning transmission electron microscope (BF-STEM) image of the BH fabricated using selective etching of the MQW followed by regrowth of InP. The BF-STEM image clearly shows that the BH was successfully fabricated on the InP-on-insulator substrate without dislocations. The relatively dark region along the original surface of the InP-on-insulator is attributed to the existence of As and Ga that originate from the etch-stop layer. Figure 7b,c show high-angle annular dark-field STEM (HAADF-STEM) images of the BH fabricated on the InP-on-insulator substrate and of MQWs grown on an InP substrate, respectively. Note that the former is the fabricated laser (i.e., after the epitaxial regrowth of InP, thermal diffusion of Zn, ion implantation of Si, etc.), whereas the latter is an as-grown sample. Figure 7d,e show the moving average of the contrast profiles extracted from the HAADF-STEM images, respectively. The contrast profiles are normalized because the signal intensity depends on the thickness of the sample lamella. The size of each pixel is 0.12 nm, and each well/barrier level (red line) is determined by averaging 21 pixels. We evaluated the transition width between the 10 and 90% contrast level of each well/barrier to compare the steepness. The average transition width was 2.91 nm for the MQW grown on the InP-on-insulator substrate and 2.40 nm for the MQW grown on the InP substrate. In terms of the steepness of the well/barrier interfaces, we observed no significant degradation. A possible reason for the relatively larger transition width is the thicker MQW lamella for the one grown on the InP-on-insulator substrate. A thicker lamella results in a larger number of atoms along the electron-transmission direction. Therefore, the TEM contrast profile becomes more sensitive to both the depth-directional crystal distribution and misalignment of the crystal orientation to the electron transmission angle.

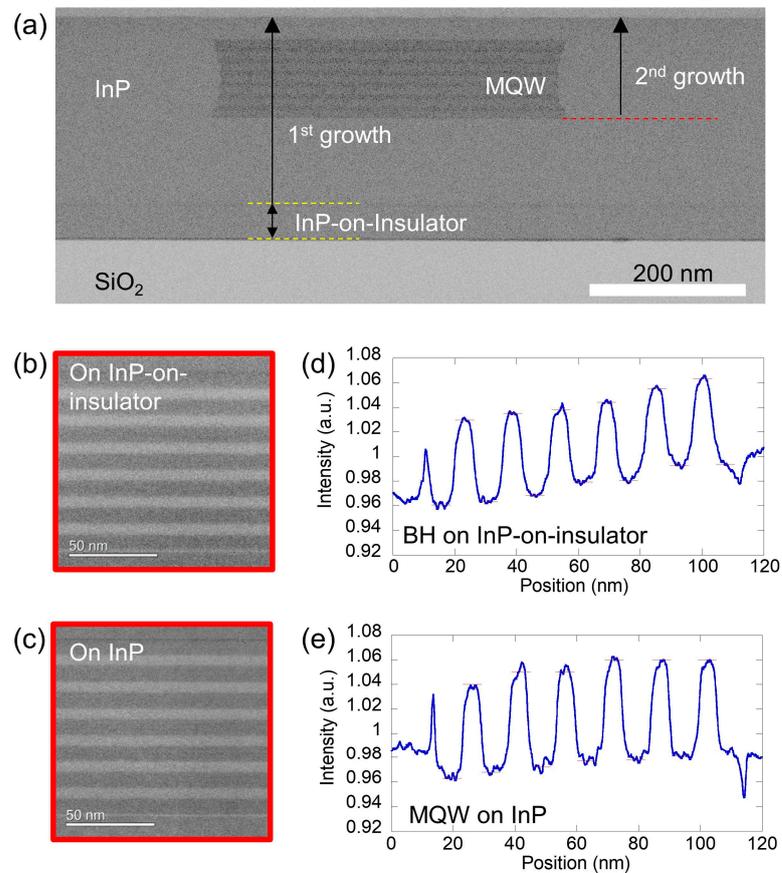


Figure 7. (a) Cross-sectional bright-field scanning transmission electron microscope (BF-STEM) image of BH on Si substrate; (b,c) high-angle annular dark-field (HAADF)-STEM image of MQW-BH grown on InP-on-insulator substrate and MQW grown on InP substrate; (d,e) moving average of contrast profile extracted from HAADF-STEM images.

We also investigated the distribution of Al, P, Ga, As, and In by energy dispersive X-ray spectrometry (EDX). Figure 8 shows the cross-sectional EDX map of the MQW-BH on the InP-on-insulator substrate, together with the extracted line profile along the depth direction. The crystal composition of each MQW stack was almost the same. Together with the contrast profile using HAADF-STEM, we conclude that there is no significant structural degradation in InGaAlAs MQWs grown on an InP-on-insulator substrate.

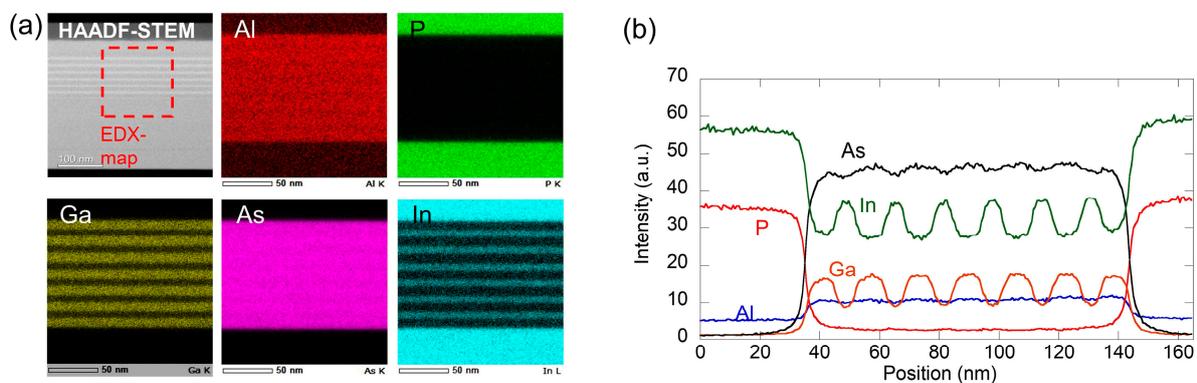


Figure 8. (a) Cross-sectional energy dispersive X-ray spectrometry (EDX) map of MQW-BH on InP-on-insulator substrate; (b) extracted line profile along depth direction.

3. Membrane Photonic Devices on Si Substrate

A thin-membrane MQW-BH structure is not only important to achieving high crystal quality but also advantageous in terms of fabricating low-power-consumption photonic devices with a small footprint. This is because a BH sandwiched between low-refractive-index silica-based materials provides high optical confinement in an active region. It provides low energy consumption, high modulation efficiency and small footprint for DMLs [49,60] and MZMs [70,71]. We describe the fabrication of low-power-consumption membrane DMLs and MZMs on a Si substrate. The fabrication of active photonic devices also verifies the crystal quality of the III-V layer grown on an InP-on-insulator substrate.

3.1. InGaAlAs Membrane Laser Array Grown on InP-on-Insulator Substrate

Figure 9a–d show the fabrication procedure of a membrane distributed-reflector (DR) laser using InGaAlAs MQWs grown on an InP-on-insulator substrate [47]. The entire fabrication procedure (including the epitaxial growth of MQW, epitaxial regrowth of InP, and formation of the lateral *p-i-n* junctions) was carried out using an InP-on-insulator substrate. To fabricate an electrically pumped membrane-laser array using thin BHs on Si, thermal diffusion of Zn (*p*-doping) and ion implantation of Si (*n*-doping) were carried out to form lateral *p-i-n* junctions. The InP output waveguides were formed using RIE. To achieve single-mode lasing, gratings were formed by dry-etching the InP surface just above the BH and a rear output waveguide using RIE. Both InP waveguides have a laterally tapered structure at the edges. After metallization, the silicon oxynitride (SiON) layer was deposited by electron-cyclotron-resonance p-CVD. The SiON layer was functionalized as not only the core of the spot-size converter (SSC) but also the cladding of the III-V waveguide layer. After defining the SiON core structures by partial etching with RIE, a SiO₂ cladding layer was deposited by p-CVD. Finally, the contact-hall was formed to electrically drive the lasers.

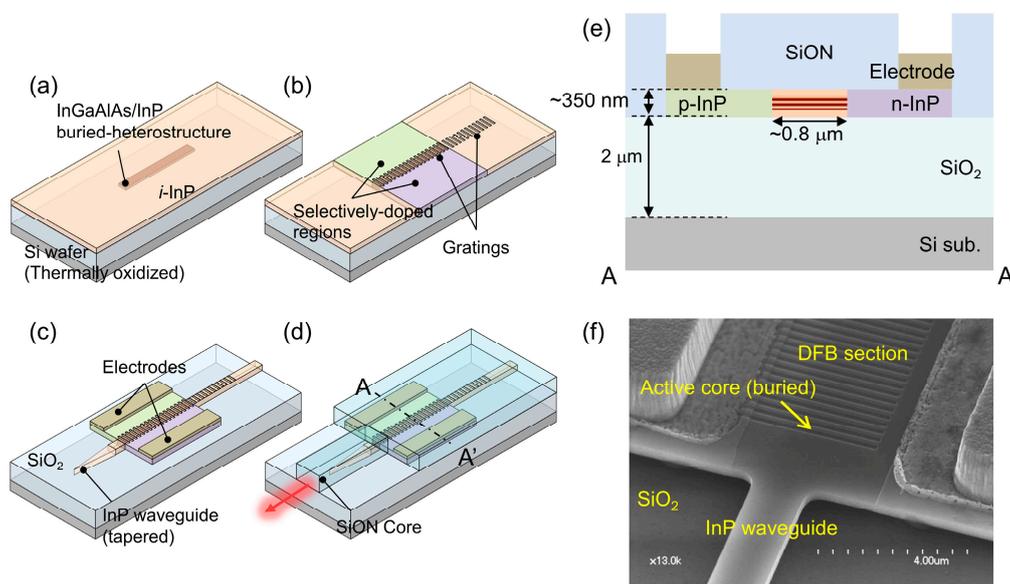


Figure 9. (a–d) Fabrication procedure of membrane distributed reflector (DR) laser using InGaAlAs MQWs grown on InP-on-insulator substrate; (e) schematic of cross-section of DR laser; (f) bird's eye view of laser before integration of the spot-size converter (SSC).

Figure 9e shows a schematic of cross-section of the fabricated laser, and Figure 9f show a bird's eye view of the fabricated membrane laser before integration of the SSC. The device has a buried active core that is 80 μm long and 0.8 μm wide. The DFB surface grating was formed just above the BH, and the distributed Bragg reflector (DBR) grating was also formed on the rear-side of the BJ InP waveguide. Since the Bragg wavelength of the DBR

grating is slightly longer compared with that of the DFB grating, the longer side-mode of the uniform DFB grating was selected and the asymmetric optical output from the front InP waveguide was achieved. The coupling coefficient was set to $\sim 800 \text{ cm}^{-1}$.

The fabricated membrane laser is an eight-channel array and each laser has the same lasing wavelength. Figure 10a shows a photograph of the diced wafer that includes four eight-channel laser arrays (32 lasers). Figure 10a also shows a top-view photograph of an eight-channel laser array. The separation of each laser (laser pitch) was $250 \mu\text{m}$, the length of the tapered InP waveguide was $300 \mu\text{m}$, and total SSC length was $660 \mu\text{m}$. The overall chip size was $2.0 \times 1.0 \text{ mm}^2$. Figure 10b shows the measured optical output power and applied voltages of an eight-channel DR laser array as a function of injected current (L-I-V characteristics). The optical output power was first measured with a photodetector placed in front of the device facet. The fiber-coupled output power was then measured by butt-coupling the single-mode high numerical aperture fiber (HNAF) to the SSC facet. The reflection at the SSC facets originally caused kinks in the light-current (L-I) curves but were successfully suppressed when the HNAF was butt-coupled. The average fiber-coupling loss was 2.98 dB. The threshold current was $\sim 1.35 \text{ mA}$ for all eight channels and the I-V characteristics were almost the same. Figure 10c compares the lasing spectra of the eight lasers at a bias current of 4.0 mA. We achieved single-mode lasing at wavelengths from 1301.5 to 1301.8 nm with an average side-mode suppression ratio of 42.7 dB. The small wavelength deviations indicate the lasers' potential for use in wavelength division multiplexing (WDM) systems.

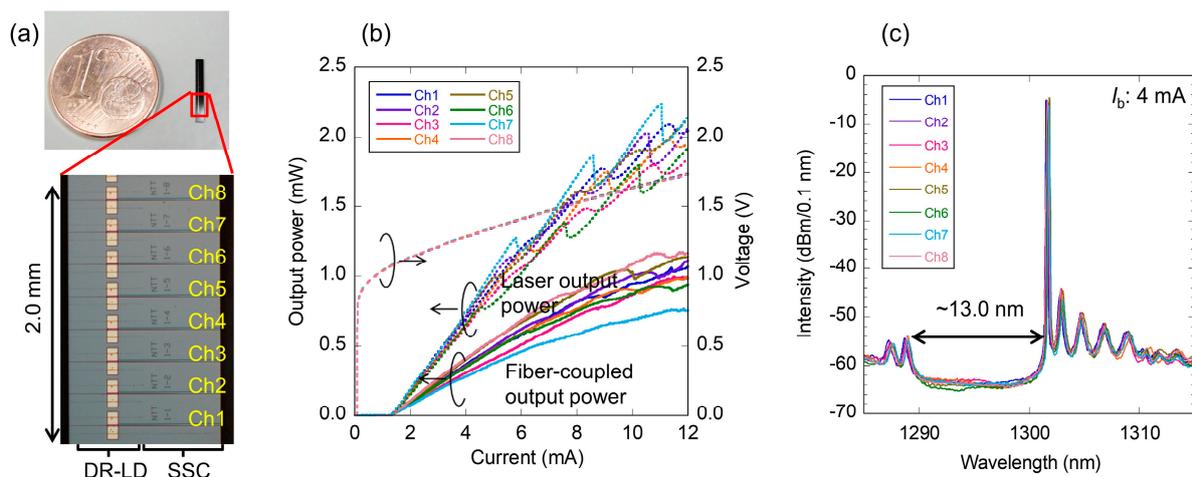


Figure 10. (a) Photograph of diced wafer that includes 4 8-channel laser arrays, together with top-view photograph of one 8-channel laser array; (b) bias-current dependence of optical output power and bias voltages at 25°C ; (c) lasing spectra with bias current of 4 mA at 25°C .

We also demonstrated 25.8-Gbit/s direct modulation with a $2^{31}-1$ pseudo-random bit sequence (PRBS) non-return-to-zero (NRZ) signal. Figure 11a shows the measured eye diagrams at 50°C . Three adjacent lasers were simultaneously modulated, and the eye diagram of the middle laser was observed to evaluate the effect of electrical crosstalk. The bias currents were from 8.0 to 8.3 mA, the bias voltages were from 1.51 to 1.62 V, and the applied voltage swings were $\sim 0.50 V_{p-p}$. We observed clear eye openings for all eight channels at 25.8-Gbit/s direct modulation with dynamic extinction ratios greater than 5.0 dB. Figure 11b shows the measured bit-error-rates (BERs) with 2^7-1 PRBS and 25.8-Gbit/s NRZ signals for back-to-back (BTB) and after 10-km transmissions at 50°C . The bias current and voltage swing were kept constant at 9.5 mA and $0.553 V_{p-p}$, respectively. To evaluate the power penalty caused by the electrical crosstalk, two adjacent lasers were simultaneously modulated with a voltage swing of zero (discrete-device operation) or $0.553 V_{p-p}$ (simultaneous operation). We achieved BERs of $\sim 10^{-12}$ after the 10-km transmission with no significant penalty even when the adjacent lasers were simultaneously

modulated. Figure 11b also shows the BTB BER results at 25 °C with a bias current of 9.5 mA and voltage swing of 0.759 V_{p-p}. The power penalty due to the temperature increase from 25 to 50 °C was also negligible.

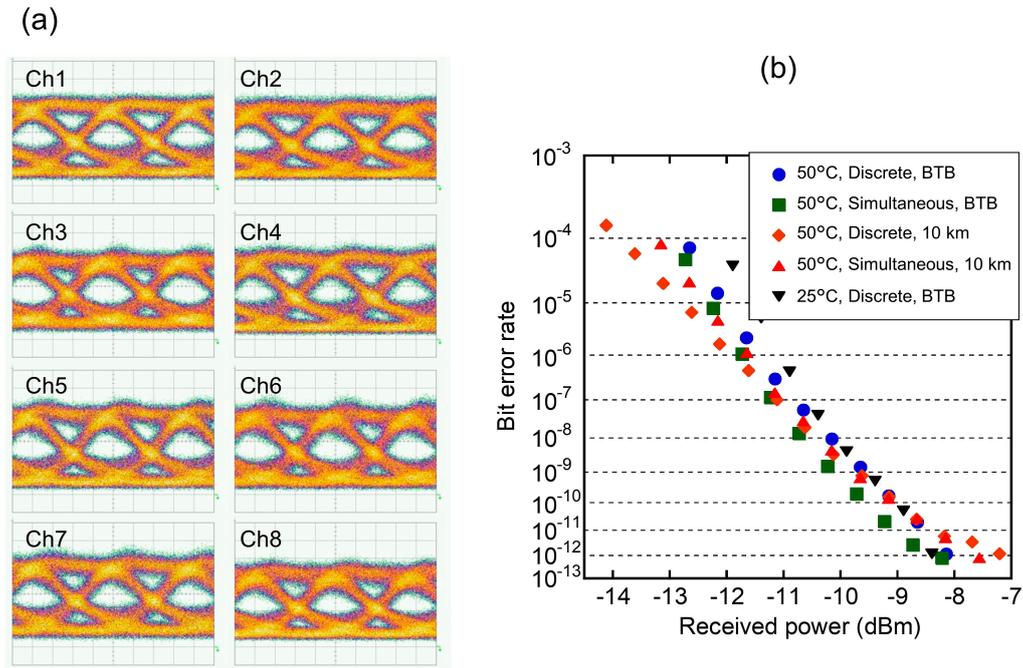


Figure 11. (a) Eye diagrams for directly modulated lasers (DMLs) with 25.8-Gbit/s non-return-to-zero (NRZ) signals at 50 °C; (b) bit-error-rates (BER) characteristics of back-to-back (BTB) and after 10-km transmissions at 50 °C.

Finally, we evaluated the static characteristics of discrete membrane lasers at high temperature [72]. Figure 12a compares the lasing spectra of two membrane lasers processed at the same time. The lasers have almost the same structure, but only the grating pitch is different to vary the lasing wavelength. The lasing wavelengths were 1303.4 and 1311.2 nm when a bias current was 10 mA, corresponding to wavelength detunings between the PL peak and lasing peak of 32.1 and 39.9 nm, respectively. Figure 12b,c compare the temperature dependence of the output power versus the injection current for these two lasers, measured with a photodetector placed in front of the device facet. The laser that has 39.9-nm-detuning exhibited lasing at up to a stage temperature of 95 °C, whereas the laser that has 32.1-nm-detuning exhibited lasing at up to 85 °C. This is attributed to the red shift of the material gain peak wavelength as the temperature increases; therefore, a larger detuning wavelength results in better performance at high temperature.

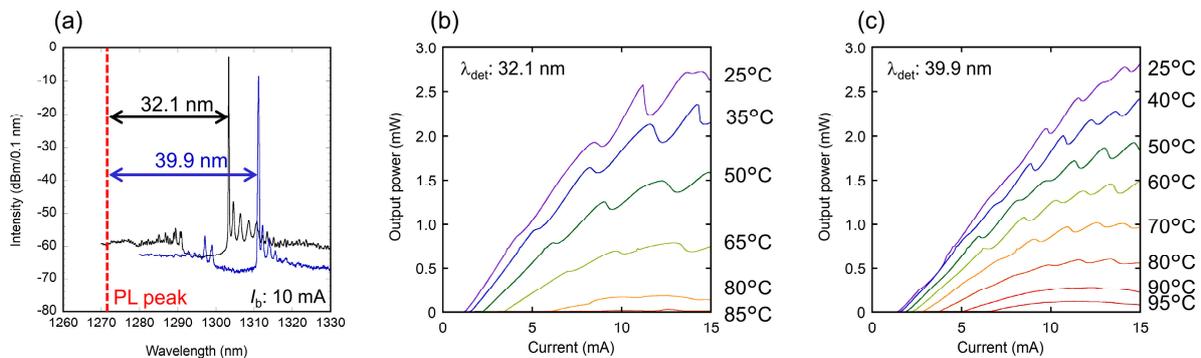


Figure 12. (a) Lasing spectra of two membrane lasers with different grating pitches; (b,c) temperature dependence of optical output vs. injection current for 32.1- and 39.9-nm-detuned laser.

3.2. Multi-Bandgap Photonic Devices Using Advanced Epitaxial Growth Technique

3.2.1. Multi-Wavelength Laser Array Using Selective-Area Epitaxial Growth

To support wide-wavelength range WDM systems, such as local area network (LAN) WDM or coarse WDM (CWDM), each laser in the array should be made of an MQW that has an optimized PL peak wavelength. This is because the typical full-width at half maximum of the MQW gain spectrum is ~ 50 nm, whereas LAN-WDM requires 35.6 nm and CWDM requires a 60- or 140-nm lasing wavelength range [73]. To integrate a WDM laser array with single epitaxy, we demonstrated the selective-area epitaxial growth of an MQW using an InP-on-insulator substrate. Figure 13a shows a schematic of the selective-area growth of the InGaAlAs MQW active layer. Due to the very high selectivity of the growth rate between the semiconductor surface and SiO₂ mask, the epitaxial layer thickness and crystal composition can be controlled by changing the mask width (w_m) and distance between the masks (w_g), which enables us to control the bandgap of the MQW layer. Therefore, the growth of the WDM laser array with a single growth becomes possible [33,74,75]. To control the PL wavelength for CWDM application, we selectively grew InGaAlAs 6-period MQWs on an InP-on-insulator substrate with the mask width ranging from 0 to 55 μm and the distance between the masks fixed at 40 μm . The epitaxial layer consists of an InP buffer layer (~ 70 nm), MQW layer, and InP cap layer (~ 25 nm) for blanket epitaxy (without selective growth mask). Figure 13b shows a cross-sectional SEM image of an MQW selectively grown on the InP-on-insulator substrate at the vicinity of the SiO₂ mask. The total III-V layer thickness with the largest mask was estimated as ~ 310 nm, which is less than the critical thickness determined by thermal strain. Figure 13c shows the PL spectra for eight MQWs measured with a PL microscope. Although the peak PL wavelength for the widest selective-area mask is unclear due to the H₂O atmospheric absorption peaks at around 1380 nm, we obtained multiple active regions with PL peak wavelengths over ~ 150 nm by carrying out only one selective epitaxial growth on the InP-on-insulator substrate. We also observed uniform PL intensity with and without selective masks for a $40 \times 200 \mu\text{m}^2$ area, as shown in Figure 13d, which is wide enough to fabricate active regions of lasers.

The eight-channel membrane DML array on a Si substrate was fabricated using the selectively grown MQWs [69]. We controlled the PL wavelength of the MQWs for LAN-WDM application. Figure 14a,b shows cross-sectional BF-STEM images of the selectively grown lasers on a Si substrate for the shortest wavelength channel and longest wavelength channel, respectively. Due to the different growth rate caused by selective epitaxy, each BH had a different total thickness but all were thinner than 350 nm. The lasers have a lateral-current injection structure and surface grating similar to those discussed in Section 3.1. The active-region length was 140 μm . Figure 14c shows the lasing spectra of eight channel DMLs with bias currents from 15 to 23 mA. The deviations between the designed wavelength and measured lasing wavelengths were less than 2 nm, and the mean channel spacing was 860 GHz. In addition, the wavelength detuning between the PL-peak and lasing spectra was almost constant (~ 35 nm) for all channels. As a result, the lasing wavelength of each channel being almost at the amplified spontaneous emission peak. This indicates precise controllability of the lasing wavelength of multi-wavelength lasers with optimal gain mediums using selective-area epitaxial growth. Finally, dynamic characteristics of the DML array were evaluated at 25 °C. We demonstrated 25.8-Gbit/s direct modulation with a $2^{31} - 1$ PRBS NRZ signal, and any pre-emphasis or equalization were not used. Figure 14d shows the eight-channel eye diagrams observed by a sampling oscilloscope. The bias currents were 15.0 to 26.5 mA, bias voltages were 1.84 to 2.65 V, and voltage swings were 0.89 to 1.58 V_{p-p}. We confirmed that all eight channels can be modulated at 25.8-Gbit/s with a dynamic extinction ratio of >4.0 dB. These results strongly indicate the potential for establishing wide-wavelength-range WDM-PICs for optical interconnects for future data-center networks using the III-V-on-insulator substrate.

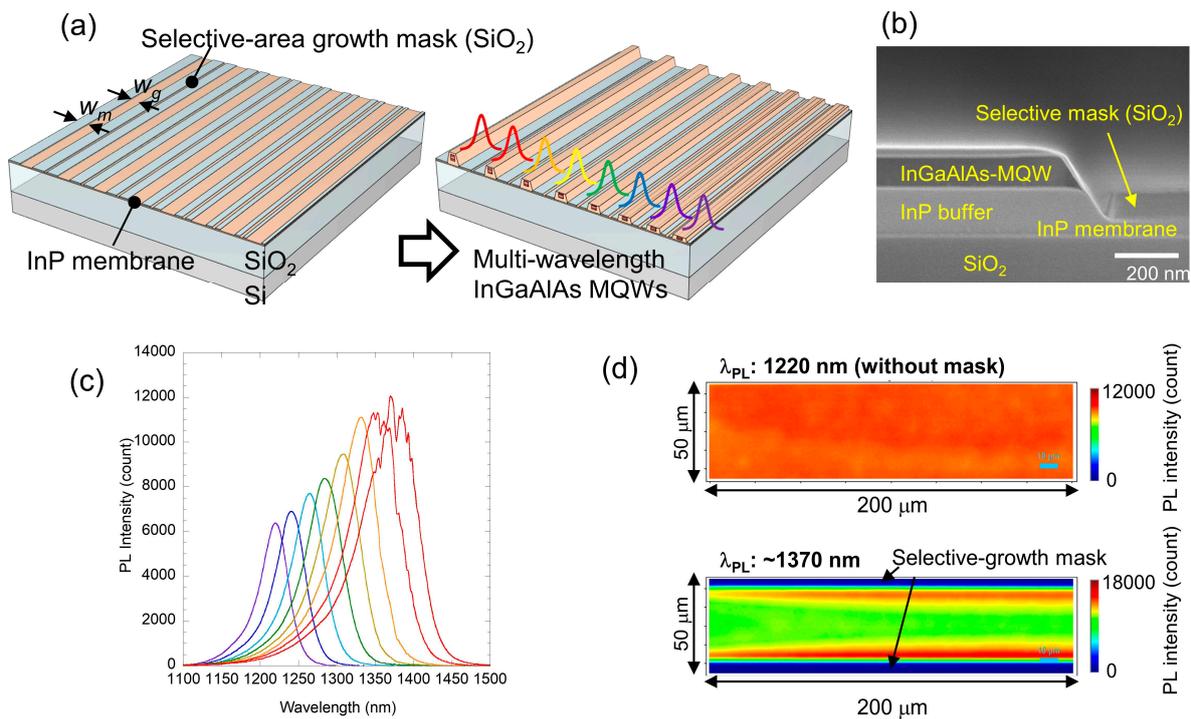


Figure 13. (a) Schematic of selective-area epitaxy of InGaAlAs MQWs with different bandgaps; (b) cross-sectional SEM image of an MQW selectively grown on InP-on-insulator substrate at the vicinity of selective growth mask; (c) PL spectra for selectively grown InGaAlAs-6-period MQWs on InP-on-insulator substrate; (d) PL-intensity distributions for MQWs without selective growth mask ($\lambda_{PL}: 1220 \text{ nm}$) and with selective growth masks ($\lambda_{PL}: \sim 1370 \text{ nm}$).

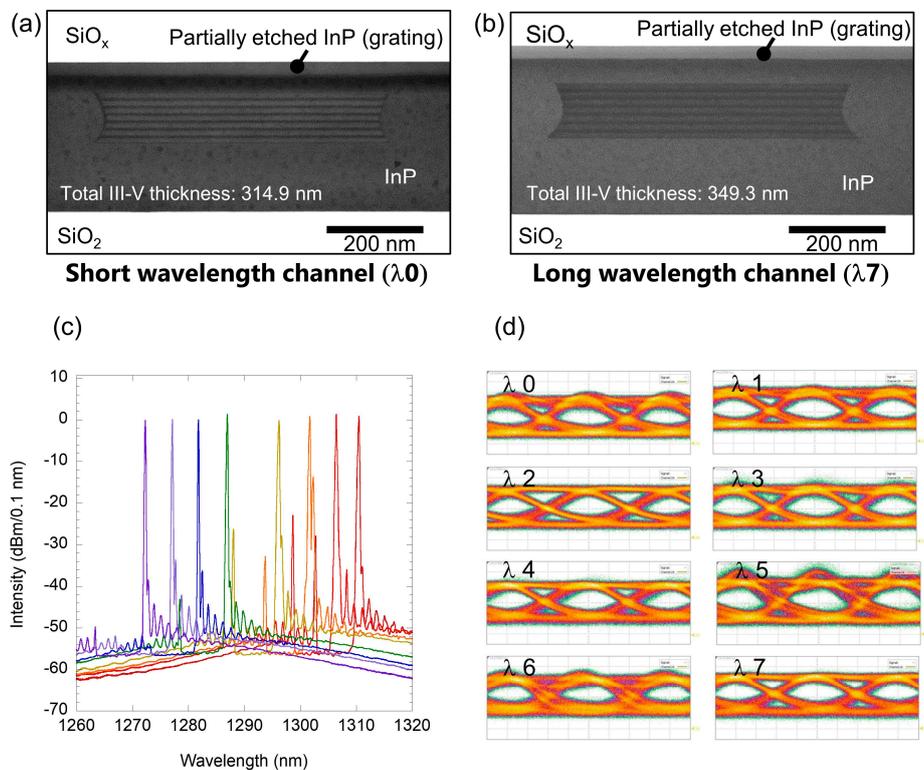


Figure 14. (a,b) Cross-sectional BF-STEM image of selectively grown lasers on Si substrate for shortest wavelength channel and longest wavelength channel; (c) lasing spectra of eight-channel membrane lasers with bias currents from 15 to 23 mA; (d) eye diagrams for eight-channel membrane lasers directly modulated with a 25.8-Gbit/s NRZ signal at 25 °C.

3.2.2. DFB Laser Integrated with MZM Using Epitaxial Regrowth of InGaAsP

To support advanced high-baud-rate modulation formats for data centers, a WDM transmitter PIC that includes an MZM with a distributed feedback (DFB) laser array is desirable. For this purpose, heterogeneously integrated PICs using low-loss Si photonics devices for optical multiplexer and Mach–Zehnder interferometers and III-V-based devices for laser and phase modulators are promising. Therefore, it is essential to use BJ regrowth on a III-V-on-insulator substrate, which enables the integration of different-bandgap active regions on the same plane. Figure 15a shows the process flow of integrating BHs that include different bandgap active regions [71]. A six-period InGaAsP MQW-DH optimized for DFB lasers was originally grown on an InP substrate and transferred to a Si-photonics platform using direct bonding. The 220-nm-thick Si waveguide layer was fabricated in advance underneath the MQW layer. After removing the excess MQW region, a 20-nm InP buffer layer, 100-nm-thick Si-doped InGaAsP bulk layer optimized for phase shifters, and 30-nm InP cap layer were regrown on an InP membrane. We adopted a thin InP buffer layer to obtain a high confinement factor in the membrane phase shifter (>40%) for high modulation efficiency. These two active regions were then simultaneously patterned to mesa-stripes and buried with undoped InP. The total III-V layer thickness was 230 nm, which was thinner than the critical thickness determined by thermal strain. Figure 15b shows the normalized PL spectra for two BHs measured with a PL microscope. Figure 15c shows the PL-intensity map and PL-wavelength map for the two BHs placed in close to evaluate PL at one mapping. The different bandgap materials for the C-band DFB laser (λ_{PL} : 1.52 μm), MZM (λ_{PL} : 1.3 μm) and passive InP waveguide were integrated on the Si-photonics platform. The PL signals observed at the vicinity of InGaAsP MQW corners originate from the remaining selectively grown InGaAsP bulk layer because the growth rate accelerates at these regions. The micro-PL map revealed that both the MQW-BH and InGaAsP-bulk BH were uniform, although the InGaAsP bulk layer was selectively grown on an InP-on-insulator substrate. Since the InP buffer layer was only 20 nm, this growth technique should also be applicable for BJ regrowth, which enables the fabrication of EADFB lasers.

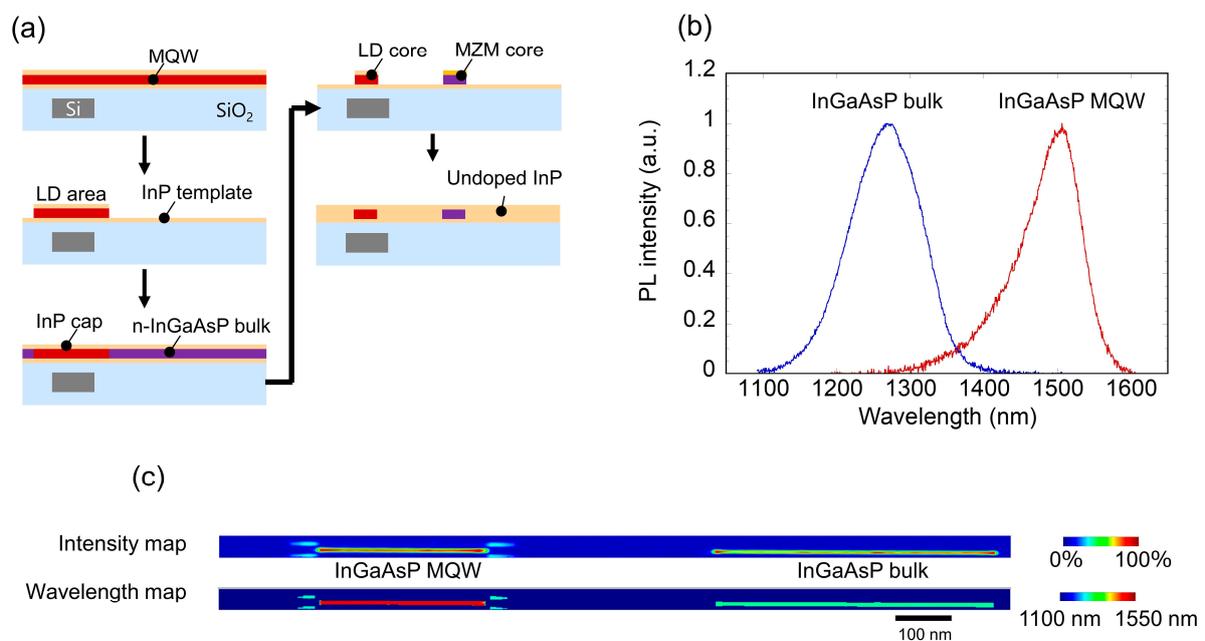


Figure 15. (a) Process flow of integrating different-bandgap BHs using epitaxial regrowth; (b) normalized PL spectra for directly bonded indium gallium arsenide phosphide (InGaAsP) MQW and epitaxially grown InGaAsP bulk buried with InP; (c) PL-intensity and PL-wavelength maps for both BHs.

Figure 16a shows a schematic of a DFB laser integrated with a MZM on a Si-photonic platform using our epitaxial regrowth technique. Both the DFB laser and phase shifters were 500- μm long and 230-nm thick and optically connected to the Si waveguides and Si multimode interferometers (MMIs) underneath the III-V membrane layer. The Si inverse-taper SSCs were also integrated for the low-loss fiber coupling. The lasing emission was obtained from both ends of the DFB laser, and two output waveguides were integrated so that the lasing characteristics with and without an MZM can be measured. Figure 16b,c shows cross-sectional SEM images of the fabricated chip for the DFB-laser section and phase-shifter section, respectively. The *p-i-n* and *p-n* diodes were fabricated using Zn thermal diffusion and Si ion implantation to the InP layers. Figure 16d shows the lasing spectrum of the output light measured by butt-coupling the HNAF. The laser current was 50 mA and MZM DC voltage was 4.5 V. These results indicate single-mode operation with a side-mode suppression ratio of around 55 dB. We also input radio-frequency signals to one arm of the MZM to evaluate its dynamic characteristics. Figure 16e shows the measured eye diagram for a 28-Gbit/s signal without 50- Ω termination. A clear eye opening was obtained with a laser current of 42 mA. In addition, the $V_{\pi}L$ estimated from the static V_{π} measurement was around 0.4 Vcm, which is almost three times smaller than that of a conventional Si MZM [71].

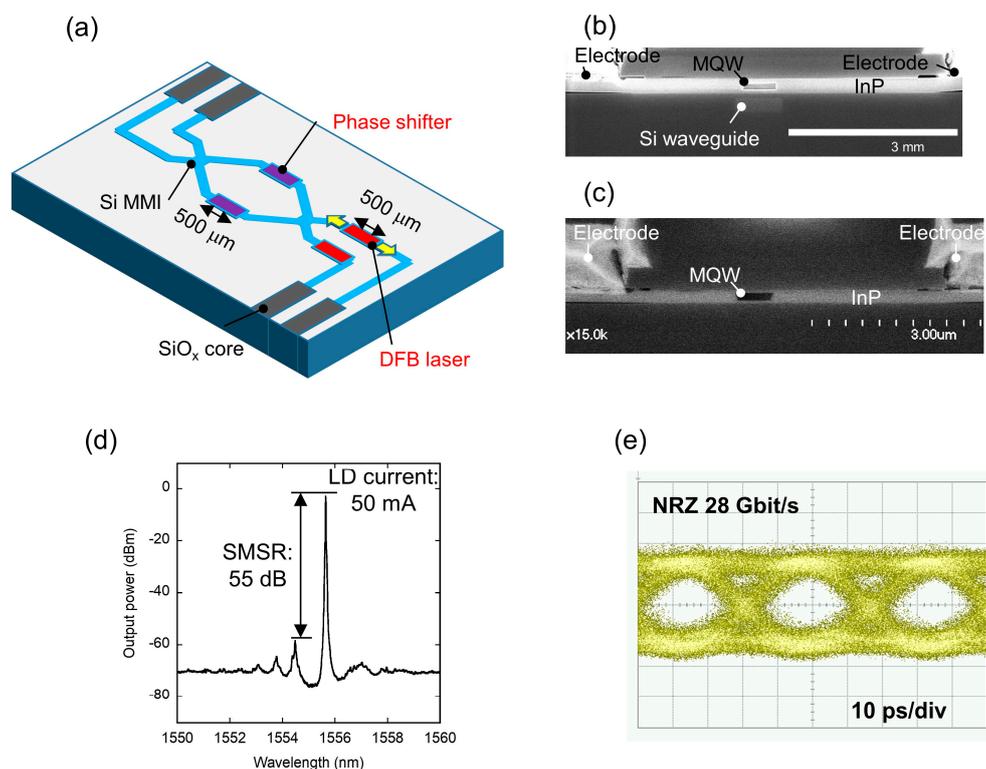


Figure 16. (a) Bird's eye view of a laser diode (LD)-Mach-Zehnder modulators (MZM) integrated chip; (b,c) cross-sectional SEM images of distributed feedback (DFB) LD and phase shifter; (d) lasing spectrum of output light from MZM output port; (e) eye diagram with 28 Gbit/s NRZ signal.

4. Conclusions

In this paper, the recent progress in the epitaxial growth technique using the InP-based membrane on a Si substrate and its contribution for integrating of low-operation energy membrane photonic devices on a Si substrate have been reviewed. Use of the thin III-V membrane structure makes it possible to carry out high-quality epitaxial growth on an InP-on-insulator substrate. The thickness-dependence of the high-temperature tolerance of a III-V-on-insulator substrate was revealed both theoretically and experimentally. In

addition, the growth of quaternary compound semiconductors such as InGaAlAs MQWs and InGaAsP bulk on an InP-on-insulator substrate was demonstrated. The TDD in InGaAlAs MQWs evaluated with a PL microscope was less than $4.0 \times 10^2/\text{cm}^2$, which is even lower than the typical commercially available InP wafer specification. TEM measurement also revealed that there is no obvious structural degradation in MQWs grown on an InP-on-insulator substrate. Using this growth technique, a 1.3- μm -range directly modulated laser array on a Si substrate was fabricated. The fabricated laser array exhibited 25.8-Gbit/s direct modulation at 50 °C with bias currents from only 8.0 to 8.3 mA and lasted up to 95 °C. In addition, a multi-wavelength DML array with optimized-bandgap MQWs was demonstrated using the selective-area growth of multi-wavelength MQWs on an InP-on-insulator substrate. Selective-area growth enables full-O-band bandgap control of InGaAlAs MQWs over 150 nm. Furthermore, integration of a DFB laser and InGaAsP MZM was demonstrated using selective regrowth of InGaAsP bulk material on the InP membrane on Si-photonics circuits.

To manufacture PICs using epitaxial regrowth techniques, demonstrating scalability will be the next important step. There is essentially no difficulty up to 150-mm wafer because both the InP wafer and MOVPE system are already available. To integrate InP on 200- and 300-mm Si wafer, die-to-wafer bonding technologies can resolve the wafer-size mismatch between Si and InP [76]. In addition, Smart Cut and epitaxial lift-off are promising technologies to fabricate InP-on-insulator substrate at low cost because these technologies enable reuse of the donor InP wafer [77,78]. We believe that the epitaxial growth techniques using an InP-on-insulator substrate are scalable and paving the way for providing a promising approach for establishing III-V/Si PICs for future data-center networks.

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