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A Transformer-Less Buck-Boost Grid-Tied Inverter with Low Leakage-Current and High Voltage-Gain

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Abstract: To improve the efficiency of photovoltaic (PV) grid-tied systems and simplify the circuit structure, many pseudo DC-link inverters have been proposed by combining a sinusoidal pulse-width modulation (SPWM) controlled buck-boost converter and a low-frequency polarity unfolder. However, due to the non-ideal characteristics of power diodes, the voltage-gain of a buck-boost converter is limited. To meet the needs of grid-connected systems with low input voltage and 220 V_{rms} utility, this paper uses two two-switch buck-boost converters with coupled inductors to develop a transformer-less buck-boost grid-tied inverter with low leakage-current and high voltage-gain. The proposed inverter is charging on the primary side of the coupled inductor and discharging in series on the primary side and the secondary side so that the voltage-gain can be greatly increased. Furthermore, the utility line can be connected to the negative end of the PV array to suppress leakage current, and the unfolding circuit can be simplified to reduce the conduction losses. High-frequency switching is only performed in one metal-oxide-semiconductor field-effect transistor (MOSFET) in each mode, which can effectively improve conversion efficiency. A prototype was implemented to obtain experimental results and to prove the validity of the proposed circuit structure.

Keywords: leakage-current; voltage-gain; transformer-less; buck-boost; inverter; grid-tied

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1. Introduction

In recent years, the amount of greenhouse gas emissions has risen rapidly along with the development of technology. On the premise of maintaining the natural environment, replacing petrochemical energy with non-radioactive and pollution-free renewable energy is an urgent and necessary work. Among the renewable energies that have been developed, the technology of PV power generation has been quite mature, making PV distributed power generation systems grow rapidly.

For PV power generation systems powered in parallel with the mains, an inverter is required to convert the PV output voltage into an AC output, so that many scholars focus on the investigation of the circuit structure of inverters [1,2]. The common H-bridge inverter is typed of buck. Since the output voltage of PV array is low level and varies greatly with the temperature and the intensity of sunlight, the general PV grid-tied system needs to insert a boost converter, as shown in Figure 1. This boost converter can achieve the functions of input-voltage regulation and maximum-power-point tracking [3]. However, except for increasing the number of components, increasing costs, and reducing reliability, the main shortcoming is lowering the system efficiency caused by multiple energy processing.

To overcome these problems, many single-stage inverters derived from boost or buck-boost converters have been proposed [4–6], but they are restricted by the usage of two input sources or the wide-range changes in input voltage. Therefore, high-efficiency pseudo DC-link inverters [7–13], as shown in Figure 2, are propose to overcome these shortcomings. As can be seen from Figure 2, a high-frequency DC–DC converter generates a unipolar half-wave and a low-frequency unfolder switches the polarity to produce AC

voltage. Since the high-frequency energy processing is only performed once, efficiency can be improved by reducing power losses. Among these inverters, the flyback and forward converters can be used as the front-end circuit to achieve high voltage-gain and electrical isolation [7–9]. To apply to PV grid-tied systems with wide-ranging input-voltage changes, non-isolated pseudo DC-Link inverters are usually implemented by buck-boost converters [10–13]. If the power switches of the two-switch buck-boost converter are switched independently, the non-isolated inverter can work with the principle of either buck type or boost type. Part of the energy could be directly transferred to the output, which can improve conversion efficiency. Theoretically, the buck-boost converter has extremely high voltage gain. However, in practice, due to the non-ideal characteristics of the power elements and the reverse-recovery issue of diodes under a high duty ratio, the voltage gain is restricted. When the input voltage is low, these inverters are not feasible for the mains with high AC voltage.

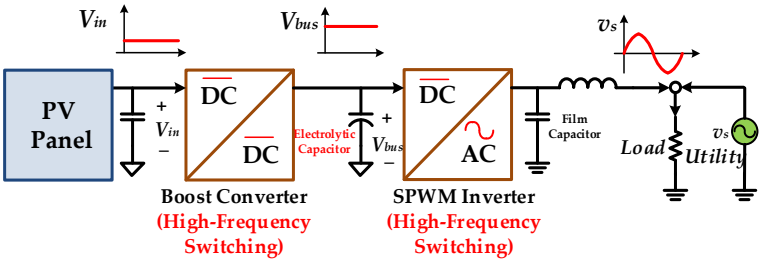


Figure 1. The PV grid-tied system with two stage of energy processing.

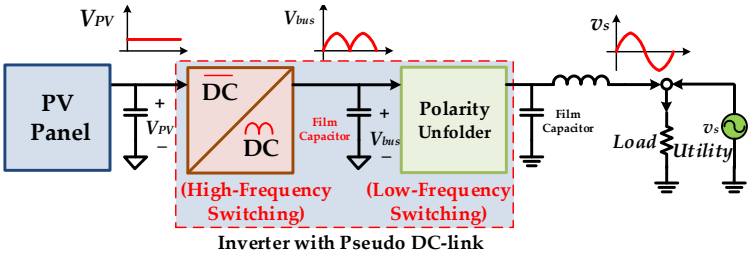


Figure 2. The PV grid-tied system with a single stage of energy processing.

Moreover, in the grid-tied applications, because of high efficiency, small size, and low cost, the transformer-less inverters are more attractive than those with transformers [14,15]. However, there is a parasitic capacitance between the PV panel and the frame ground, which may induce leakage current and cause electromagnetic interference, current harmonics, and power loss [16]. There are three main methods to suppress leakage current [17]: (1) Separating the PV array from utility-line in freewheeling mode; (2) Connecting the mains to the center of two DC-bus capacitors to limit the common mode voltage (CMV); (3) Connecting the mains directly to the negative end of the PV array. Distinguished by the circuit structures, transformer-less inverters with low leakage current can be classified as: (1) Diode-clamped architecture [18], (2) H5 [19], (3) HERIC [20], (4) oH5 [21], (5) H6 [22], and (f) HBZVR [23]. The H5 inverter suppresses the leakage current by adding one power switch to keep CMV as constant [19]. The oH5 inverter improves the voltage stresses of the power components by adding one additional switch to clamp CMV to be half of the H5 inverter [21]. A non-isolated inverter with step-up/down capability is proposed in the literature [17], in which a power switch is added to control the freewheeling path of inductor current. This inverter connects the utility-line to the negative end of the PV array, which can suppress leakage current. However, the disadvantage of this inverter is that it operates with the principle of buck-boost. The energy needs to be saved in the inductor before being transmitted; it reduces the conversion efficiency and limits the output power.

Based on the previous considerations, a transformer-less buck-boost grid-tied inverter with low leakage-current and high voltage-gain is proposed. Two dual-switch buck-boost converters with coupled inductors are connected in parallel to generate a unipolar half-wave, and two low-frequency switches are adopted to switch the output polarity. When the proposed circuit operates in the step-up mode, the primary side of the coupled inductor is charged first, and then the primary side and the secondary side are discharged in series, which can increase voltage-gain. In addition, due to the use of two buck-boost converters in parallel, the polarity unfolder is able to be effectively simplified as two switches to reduce conduction losses. The mains can be directly attached to the negative end of the PV array to suppress leakage current. In addition, the proposed inverter also has the following features:

1. Only single energy-processing is required, and high-frequency switching is only performed in one MOSFET in each mode, which can effectively improve efficiency;
2. The inverter operates with the principle of boost or buck, so that part of the energy can be directly transmitted to improve efficiency;
3. The proposed inverter is feasibility for PV grid-tied systems with wide-range voltage changes because of its step-up and step-down capabilities.

2. Circuit Configuration

The schematic of the investigated transformer-less buck-boost grid-tied inverter is illustrated in Figure 3. Two dual-switch buck-boost DC–DC converters with coupled inductors are connected in parallel and output unipolar half-waves respectively during positive and negative half-cycles. The dual-switch buck-boost converter for a positive half-cycle is mainly composed of the power switches S_{Bu1}, S_{Bo1}, the diodes D_1, D_3, and the coupled inductors L_1, L_3. The power switches S_{Bu2}, S_{Bo2}, the diodes D_2, D_4, and the coupled inductors L_2, L_4 form the dual-switch buck-boost converter for the negative half-cycle. The capacitors C_f, C_s and the inductor L_s are the output low-pass filter. Since this paper focuses on the steady-state characteristics and feasibility of the proposed circuit structure, the input source is represented by an ideal voltage source to simplify the circuit.

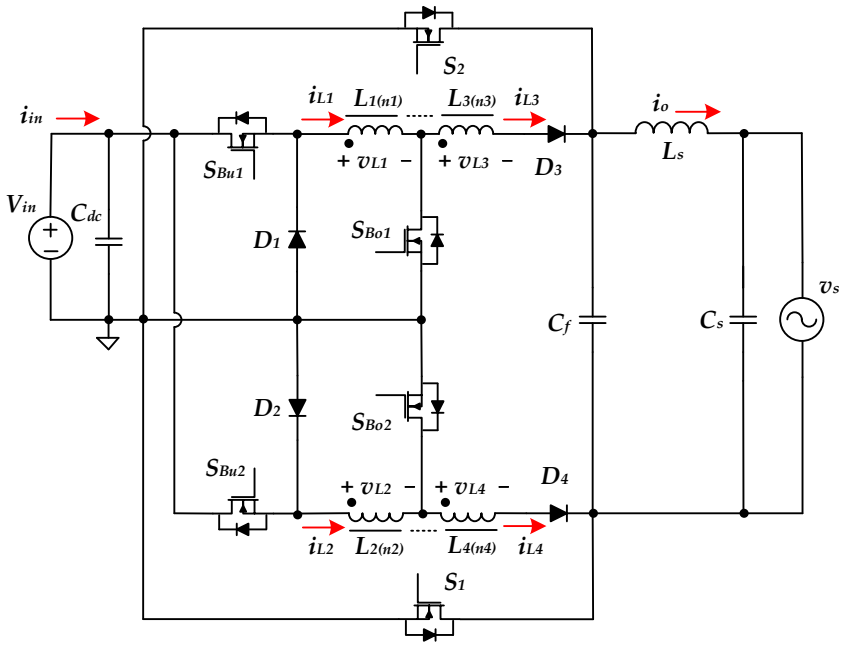


Figure 3. The schematic of the investigated transformer-less buck-boost grid-tied inverter.

During the positive (negative) half-cycle and in the step-down mode, the switch S_{Bu1} (S_{Bu2}) performs high-frequency switching, and the power switch S_{Bo1} (S_{Bo2}) is maintained in the off state. When S_{Bu1} (S_{Bu2}) is turned on, energy is able to be directly delivered to the

output terminal via the switch S_1 (S_2). Its working principle is similar to a buck converter, resulting in greatly improving conversion efficiency.

During the positive (negative) half-cycle and in the step-up mode, the switch S_{Bo1} (S_{Bo2}) performs high-frequency switching, and the power switch S_{Bu1} (S_{Bu2}) remains on. When S_{Bo1} (S_{Bo2}) is switched off, energy is able to be directly delivered to the output terminal via the diode D_3 (D_4) and the switch S_1 (S_2). Its working principle is similar to a boost converter, which can greatly improve conversion efficiency.

In addition, the switch S_1 (S_2) can provide a path for connecting the mains and the negative end of the input source, so that the leakage current of the PV array can be suppressed. The proposed transformer-less buck-boost inverter is appropriate for the PV grid-tied systems with wide-range voltage changes or high AC output-voltage because of its step-up and step-down capabilities. In addition, high-frequency switching is performed in only one MOSFET in each state, leading to low switching loss and high conversion efficiency.

3. Operation Principles

The investigated transformer-less buck-boost inverter is controlled by SPWM. Figure 4 is a conceptual diagram of the input voltage V_{in}, the mains voltage v_s(t), the operation modes, and the switch driving-signals in a line-cycle, where the peak value V_M of v_s(t) is higher than V_{in}. T_{ac} is the period of the mains voltage. As can be seen from Figure 4, based on the level of V_{in} and v_s(t), the investigated buck-boost inverter works in step-down or step-up mode, respectively. In the following, with regard to these two modes, their working principles in steady-state and the equivalent circuits of high-frequency switching will be provided in sequence.

3.1. Step-Down Mode

When the absolute value of the mains voltage $|v_s(t)|$ is lower than the input voltage V_{in}, the step-down mode is performed. During the positive half-cycle ($0 \leq \omega t \leq \pi$), the switch S_{Bu2} and the switches S_{Bo1}, S_{Bo2} remain in off state, and the switch S_1 remains in on state to provide a path for energy transfer. At this time, the power switch S_{Bu1} is controlled by high-frequency SPWM switching, and its duty ratio d_{Bu1}(t) is able to be presented as in Equation (1):

$$d_{Bu1}(t) = d_{Bu}(t) = \frac{V_P \sin \omega t}{V_{in}}, \ (V_P \sin \omega t \leq V_{in}). \tag{1}$$

when the switch S_{Bu1} is switched on, the diode D_1 turns off. Currently, the input voltage V_{in} charges the inductors L_1 and L_3 in series through the switches S_{Bu1} and S_1, and it transmits energy directly to the output. Figure 5a shows the corresponding circuit. When the switch S_{Bu1} is switched off and the diode D_1 is turned on, the inductors L_1 and L_3 in series release energy to the output. Figure 5b shows the corresponding circuit. The voltage gain of continuous conduction mode (CCM) is able to be presented as in Equation (2):

$$\frac{|v_s(t)|}{V_{in}} = d_{Bu}(t) \ . \tag{2}$$

It is worth mentioning that since the switch S_1 can connect the mains and the negative end of the input source, the leakage current of the PV array is able to be suppressed.

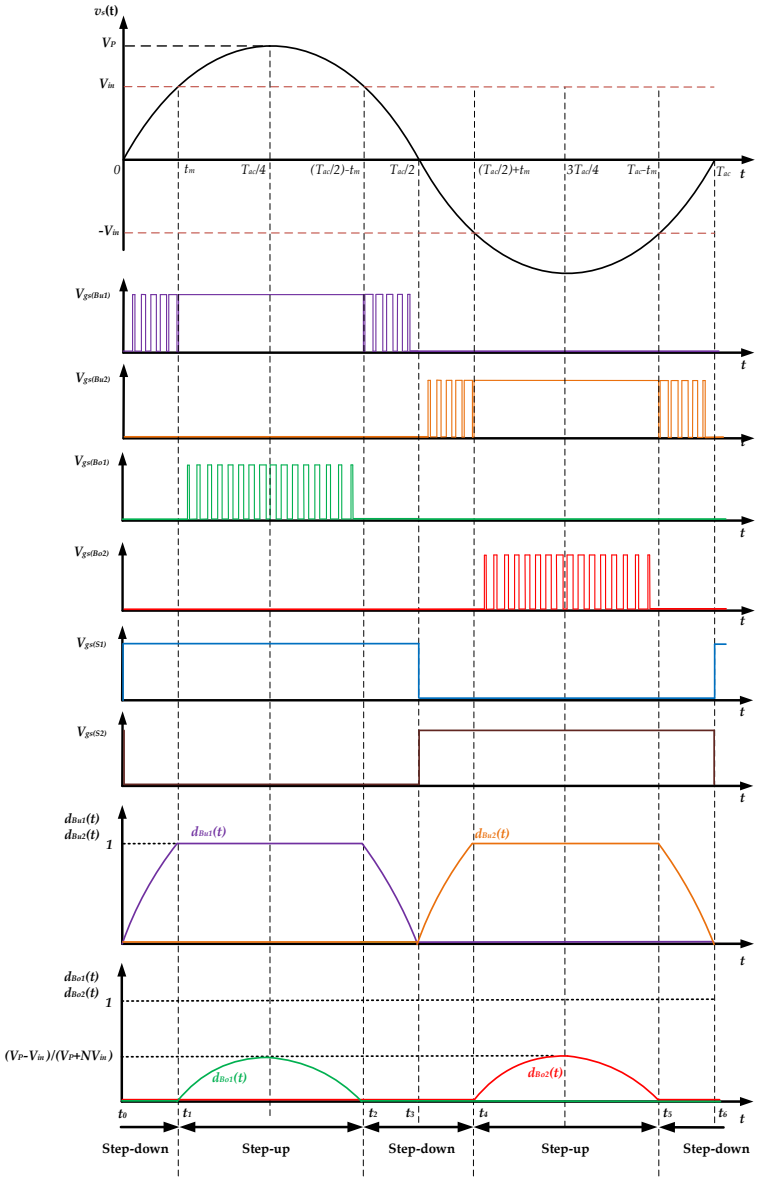
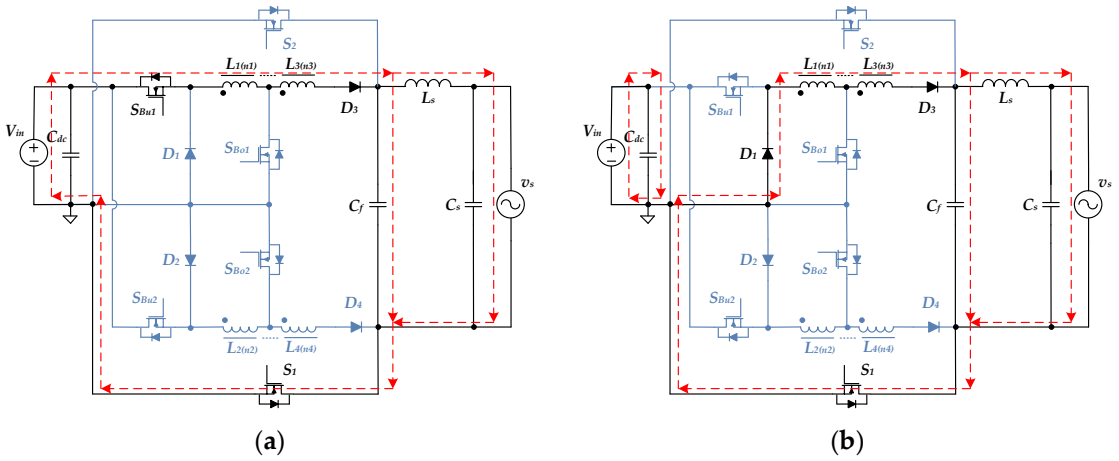


Figure 4. The timing diagram of working modes and switch driving signals.



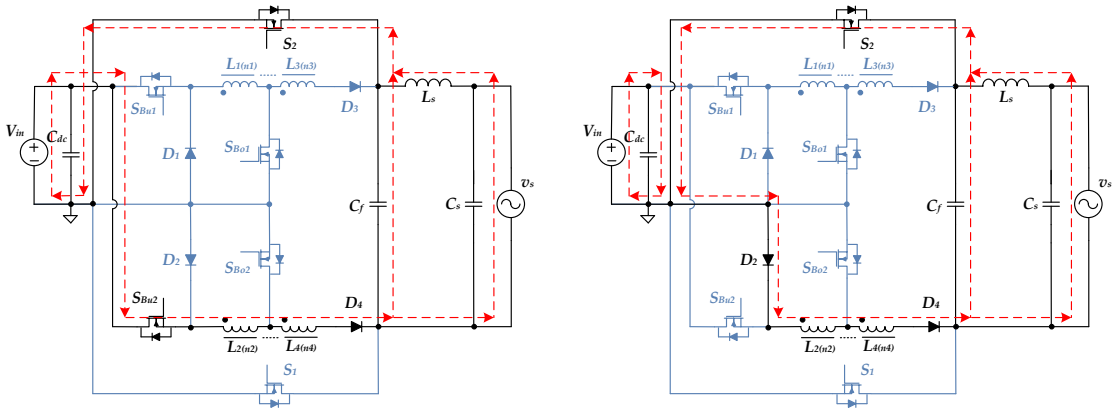
(**a**) (**b**)

Figure 5. During the positive half-cycle, the corresponding circuits of step-down mode: (**a**) S_{Bu1} ON, S_{Bu2} OFF, S_{Bo1} OFF, S_{Bo2} OFF, S_1 ON, and S_2 OFF; (**b**) S_{Bu1} OFF, S_{Bu2} OFF, S_{Bo1} OFF, S_{Bo2} OFF, S_1 ON, and S_2 OFF.

When the mains voltage v_s(t) becomes negative ($\pi \leq \omega t \leq 2\pi$), the switches S_{Bu1}, S_{Bo1}, and S_{Bo2} remain off, and the switch S_2 is turned on to provide a path for energy transmission. At this moment, the switch S_{Bu2} is controlled by high-frequency SPWM. Its duty ratio is the same as that of the switch S_{Bu1} in the positive half-cycle, which can be presented as in Equation (3):

$$d_{Bu2}(t) = d_{Bu}(t) = \frac{|V_P \sin \omega t|}{V_{in}}, \ (|V_P \sin \omega t| \leq V_{in}). \tag{3}$$

when the switch S_{Bu2} is switched on, the diode D_2 is switched off. At this moment, the input source V_{in} charges the inductors L_2, L_4 in series through the power switches S_{Bu2} and S_2, and it transfers energy directly to the output. Figure 6a shows the corresponding circuit. When the switch S_{Bu2} is switched off, the diode D_2 is switched on, and the inductors L_2, L_4 in series release energy to the output. Figure 6b shows the corresponding circuit, and the voltage gain of CCM is the same as Equation (2). In this state, the path of connecting the mains and the negative end of the input voltage is provided by the power switch S_2, which can also achieve the effect of suppressing the leakage current of the PV array.



(**a**) (**b**)

Figure 6. During the negative half-cycle, the corresponding circuits of step-down mode: (**a**) S_{Bu1} OFF, S_{Bu2} ON, S_{Bo1} OFF, S_{Bo2} OFF, S_1 OFF, and S_2 ON; (**b**) S_{Bu1} OFF, S_{Bu2} OFF, S_{Bo1} OFF, S_{Bo2} OFF, S_1 OFF, and S_2 ON.

3.2. Step-Up Mode

When the absolute value of the mains voltage $|v_s(t)|$ is higher than the input voltage V_{in}, the inverter works in step-up mode. The working principle of this mode is similar to that of a boost converter. The switch S_{Bo1} (S_{Bo2}) is controlled by high-frequency SPWM. When the mains voltage v_s(t) is positive ($0 \leq \omega t \leq \pi$), the switch S_{Bu1} stays on, and the switch S_{Bu2} stays off. When the switch S_{Bo1} is switched on, the diode D_3 is switched off, and switch S_1 remains on to provide a path for energy delivering. At this moment, the input voltage V_{in} delivers energy to the inductor L_1, and the capacitor C_f provides the energy required by the output. Figure 7a shows the corresponding circuit. The voltage across the inductor L_1 is able to be expressed as in Equation (4):

$$v_{L1} = V_{in}\,. \tag{4}$$

When the switch S_{Bo1} is switched off, the diode D_3 is switched on. At this moment, the input source V_{in} transfers energy to the output terminal and charges the capacitor C_f through the coupled inductors L_1, L_3 and the switch S_1. Figure 7b shows the corresponding circuit. Since the conduction of the switch S_1 can connect the mains and the negative end

of the input source, the leakage current of the PV array can be suppressed. The voltage across the inductor L_1 is able to be presented as in Equation (5):

$$v_{L1} = \frac{V_{in} - v_s(t)}{1+N}, \tag{5}$$

in which N is the turn ratio of the coupled inductor and is defined as (n_1:n_3 = 1:N). Using the volt-second balance theorem, Equation (6) is able to be found.

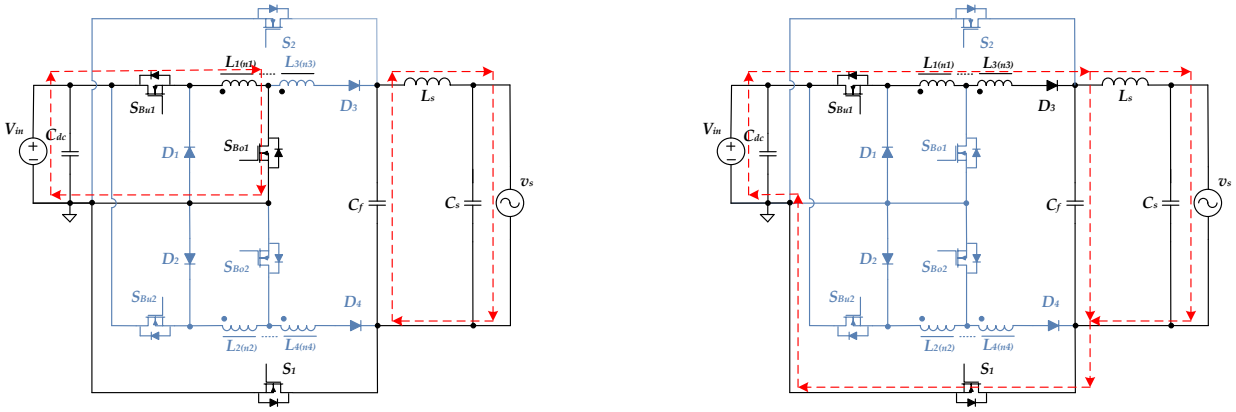
$$\int_0^{d_{Bo}T_S} V_{in}\, dt + \int_{d_{Bo}T_S}^{T_S} \left(\frac{V_{in} - v_s(t)}{1+N}\right) dt = 0, \tag{6}$$

where d_{Bo} is the duty ratio of the switch S_{Bo1}. By rearranging Equation (6), the voltage gain in CCM is shown in Equation (7):

$$\frac{v_s(t)}{V_{in}} = \frac{|V_P \sin \omega t|}{V_{in}} = \frac{1 + N d_{Bo}}{1 - d_{Bo}}. \tag{7}$$

The duty ratio d_{Bo} is able to be presented as in Equation (8):

$$d_{Bo1}(t) = d_{Bo}(t) = \frac{|V_P \sin \omega t| - V_{in}}{|V_P \sin \omega t| + N \cdot V_{in}}. \tag{8}$$



(**a**) (**b**)

Figure 7. During the positive half-cycle, the corresponding circuits of step-up mode: (**a**) S_{Bu1} ON, S_{Bu2} OFF, S_{Bo1} ON, S_{Bo2} OFF, S_1 ON, and S_2 OFF; (**b**) S_{Bu1} ON, S_{Bu2} OFF, S_{Bo1} OFF, S_{Bo2} OFF, S_1 ON, and S_2 OFF.

When the current of the inductor L_1 (L_2) drops to zero during S_{Bo1} switched off, the inverter works in discontinuous conduction mode (DCM), and the capacitor C_f provides the energy required by the load. Equation (9) defines the inductance constant τ_L:

$$\tau_L = \frac{L_p f_S}{R_L}, \tag{9}$$

where the inductor L_1 (L_2) is assumed to be the same inductance L_p, f_S is the frequency of MOSFET switching, and R_L is the resistance of equivalent output load. The voltage gain of DCM is presented as in Equation (10):

$$\frac{v_s(t)}{V_{in}} = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{d_{Bo}^2}{2\tau_L}}. \tag{10}$$

If the gain shown in Equation (7) is equal to Equation (10), the inverter will operate in the boundary conduction mode (BCM). Derived from this condition, the inductance constant τ_{LB} of BCM is able to be found and expressed as in Equation (11):

$$\tau_{LB} = \frac{d_{Bo}(1-d_{Bo})^2}{2(1+N)(1+Nd_{Bo})}. \tag{11}$$

If the inductance constant τ_L is smaller than its boundary value τ_{LB}, the inverter will work in DCM.

When the mains voltage v_s(t) becomes negative ($\pi \leq \omega t \leq 2\pi$) and working in the step-up mode, the roles of the switches S_{Bu1} and S_{Bu2} are exchanged. The switch S_{Bu1} stays off, and the switch S_{Bu2} stays on. When the switch S_{Bo2} is switched on, the diode D_4 is switched off, and the switch S_2 remains in the on state to provide a path for energy transmission. At this time, the input voltage V_{in} stores energy on the inductor L_2, and the capacitor C_f provides the energy required by the output. Figure 8a shows the corresponding circuit. When the switch S_{Bo2} is switched off, the diode D_4 is switched on. At this moment, the input voltage V_{in} transfers energy to the capacitor C_f and the output simultaneously through the path of the coupled inductors L_2, L_4 and the switch S_2. Figure 8b shows the corresponding circuit. The working principle of this state is similar to that of the positive half-cycle, and the voltage gain and boundary conditions are the same as those shown in Equations (7), (10), and (11). Since the continuous conduction of the switch S_2 can provide a path for connecting the mains and the negative end of the input source, the leakage current of the PV array can be suppressed.

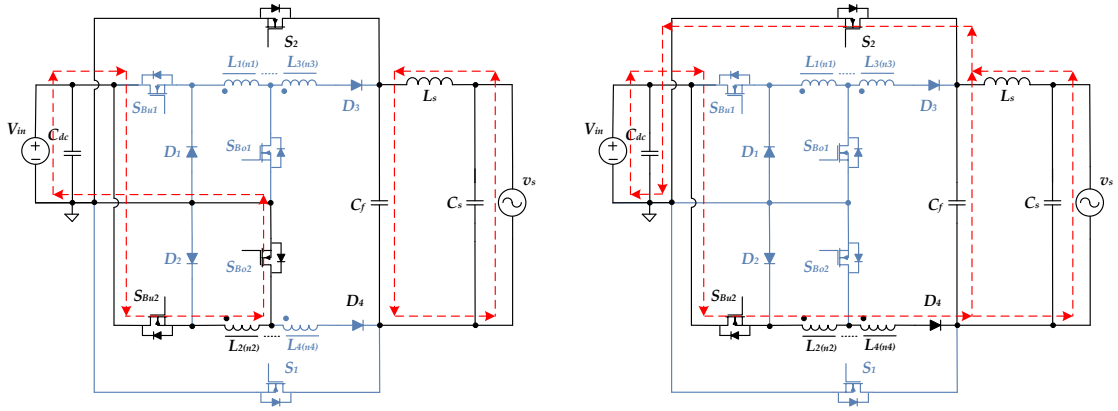


Figure 8. During the negative half-cycle, the corresponding circuits of step-up mode: (**a**) S_{Bu1} OFF, S_{Bu2} ON, S_{Bo1} OFF, S_{Bo2} ON, S_1 OFF, and S_2 ON; (**b**) S_{Bu1} OFF, S_{Bu2} ON, S_{Bo1} OFF, S_{Bo2} OFF, S_1 OFF, and S_2 ON.

As reported by the analyses mentioned above, Table 1 lists the voltage gain and the condition of each switching component within one AC cycle. As shown in this table, there are only one switch and one diode switching with high frequency (marked in green) in each state, resulting in lower switching losses. In addition, in each state, there is only one switch and one diode (or two switches) conducting continuously (marked in orange), which can reduce the conduction losses.

Table 1. The voltage gain and the condition of each switching component within one AC cycle.

Component	Positive Half-Cycle		Negative Half-Cycle	
	Step-Down Mode	**Step-Up Mode**	**Step-Down Mode**	**Step-Up Mode**
S_{Bu1}	switching with d_{Bu}	remaining on	remaining off	remaining off
D_1	switching	remaining off	always off	remaining off
S_{Bu2}	remaining off	remaining off	switching with d_{Bu}	remaining on
D_2	remaining off	remaining off	switching	remaining off
S_{Bo1}	remaining off	switching with d_{Bo}	remaining off	remaining off
D_3	remaining on	switching	remaining off	remaining off
S_{Bo2}	remaining off	remaining off	remaining off	switching with d_{Bo}
D_4	remaining off	remaining off	remaining on	switching
S_1	remaining on	remaining on	remaining off	remaining off
S_2	remaining off	remaining off	remaining on	remaining on
Gain	d_{Bu}	$(1 + Nd_{Bo})/(1 - d_{Bo})$	d_{Bu}	$(1 + Nd_{Bo})/(1 - d_{Bo})$

4. Loss Analysis

Loss analysis is performed to compare the efficiency of the investigated transformerless buck-boost inverter with the traditional grid-tied system. Since the working states are symmetrical, and the mains is a periodic sine wave, only the quarter of period needs to analyze and calculate. Assuming that the inverter always operates in CCM can simplify the analysis, and the mains voltage $v_s(t)$ is able to be presented as in Equation (12):

$$v_s(t) = V_P \sin \omega t. \tag{12}$$

If R_L is the equivalent resistance of the output load, the output load current $i_s(t)$ will be presented as in Equation (13):

$$i_s(t) = \frac{v_s(t)}{R_L} = \frac{V_P \sin \omega t}{R_L}. \tag{13}$$

Regarding the timing diagram shown in Figure 4, the inverter works in the step-down mode in the interval of time $t = 0 \sim t_m$. Within one high-frequency switching period, the average current of each inductor is able to be presented as in Equations (14)–(16):

$$i_{L1,Bu}(t) = i_{L2,Bu}(t) = i_s(t) = \frac{V_P \sin \omega t}{R_L}, \tag{14}$$

$$i_{L3,Bu}(t) = i_{L4,Bu}(t) = i_s(t) = \frac{V_P \sin \omega t}{R_L}, \text{ and} \tag{15}$$

$$i_{Ls,Bu}(t) = i_s(t) = \frac{V_P \sin \omega t}{R_L}. \tag{16}$$

The inverter works in the step-up mode in the interval of time $t = t_m \sim T_{ac}/4$. Within one high-frequency switching period, the average current of each inductor is able to be presented as in Equations (17)–(19):

$$i_{L1,Bo}(t) = i_{L2,Bo}(t) = \frac{1 + \mathrm{N} \cdot d_{Bo}(t)}{1 - d_{Bo}(t)} \times i_s(t) = \frac{(V_P \sin \omega t)^2}{V_{in} R_L}, \tag{17}$$

$$i_{L3,Bo}(t) = i_{L4,Bo}(t) = i_s(t) = \frac{V_P \sin \omega t}{R_L}, \text{ and} \tag{18}$$

$$i_{Ls,Bo}(t) = i_s(t) = \frac{V_P \sin \omega t}{R_L}. \tag{19}$$

When the peak voltage of $v_s(t)$ is higher than the input voltage, the conduction loss of each inductor is able to be obtained as in Equations (20)–(22):

$$P_{\mathrm{con},L1} = P_{\mathrm{con},L2} = \frac{2}{T_{ac}} \left[\sum_{n=1}^{N_{tm}} [i_{L1,Bu}(\frac{n}{N_s} \cdot T_{ac})]^2 \cdot R_{ESR,L1} \cdot T_{\mathrm{S}} + \sum_{n=N_{tm}}^{N_s/4} [i_{L1,Bo}(\frac{n}{N_s} \cdot T_{ac})]^2 \cdot R_{ESR,L1} \cdot T_{\mathrm{S}} \right], \tag{20}$$

$$P_{\text{con},L3} = P_{\text{con},L4} = \frac{2}{T_{ac}}\left[\sum_{n=1}^{N_{tm}}[i_{L3,Bu}(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{ESR,L1}\cdot T_{\text{S}} + \sum_{n=N_{tm}}^{N_s/4}[i_{L3,Bo}(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{ESR,L1}\cdot T_{\text{S}}\right], \tag{21}$$

$$P_{con,Ls} = \frac{4}{T_{ac}}\left[\sum_{n=1}^{N_{tm}}[i_{Ls,Bu}(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{ESR,Ls}\cdot T_{\text{S}} + \sum_{n=N_{tm}}^{N_s/4}[i_{Ls,Bo}(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{ESR,Ls}\cdot T_{\text{S}}\right], \tag{22}$$

where N_{tm} is the amount of high-frequency switching cycle within the time interval of $t = 0 \sim t_m$, and N_s is the amount of high-frequency switching cycle within one AC cycle T_{ac}. The equivalent series resistance (ESR) of each inductor is expressed as $R_{ESR,L1}$, $R_{ESR,L3}$, and $R_{ESR,Ls}$, respectively. Finally, the total inductor conduction loss of the inverter is able to be calculated from Equations (20)–(22) and presented as in Equation (23):

$$P_{con,L\_total} = P_{con,L1}\times 2 + P_{con,L3}\times 2 + P_{con,Ls}. \tag{23}$$

The conduction loss of each MOSFET is able to be calculated as in Equations (24)–(26):

$$P_{con,Bu1} = P_{con,Bu2} = \frac{2}{T_{ac}}\left[\sum_{n=1}^{N_{tm}}[i_s(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{DS,on}\cdot\left[d_{\text{Bu}}(\frac{n}{N_s}\cdot T_{ac})\right]^2\cdot T_S + \sum_{n=N_{tm}}^{N_s/4}[i_{\text{L1},Bo}(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{DS,on}\cdot T_{\text{S}}\right], \tag{24}$$

$$P_{con,Bo1} = P_{con,Bo2} = \frac{2}{T_{ac}}\left[\sum_{n=N_{tm}}^{N_s/4}[i_{L1,Bo}(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{DS,on}\cdot d_{Bo}(\frac{n}{N_s}\cdot T_{ac})\cdot T_{\text{S}} + \sum_{n=1}^{N_s/4}[i_s(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{DS,on}\cdot T_{\text{S}}\right], \tag{25}$$

$$P_{con,S1} = P_{con,S2} = \frac{2}{T_{ac}}\left[\sum_{n=1}^{N_s/4}[i_s(\frac{n}{N_s}\cdot T_{ac})]^2\cdot R_{DS,on}\cdot T_{\text{S}}\right], \tag{26}$$

where $R_{DS,on}$ is the conduction resistance of each MOSFET. The total switch conduction loss of the inverter is able to be calculated from Equations (24)–(26) and is presented as in Equation (27):

$$P_{con,S\_total} = P_{con,Bu1}\times 2 + P_{con,Bo1}\times 2 + P_{con,S1}\times 2. \tag{27}$$

The conduction losses of the power diodes D_1, D_2, D_3, and D_4 are able to be calculated as in Equations (28) and (29):

$$P_{con,D1} = P_{con,D2} = \frac{2}{T_{ac}}\left[\sum_{n=1}^{N_{tm}} i_{L1,Bu}(\frac{n}{N_s}\cdot T_{ac})\cdot \text{V}_{\text{F}}\cdot\left[1-d_{Bu}(\frac{n}{N_s}\cdot T_{ac})\right]\cdot T_{\text{S}}\right], \tag{28}$$

$$P_{con,D3} = P_{con,D4} = \frac{2}{T_{ac}}\left[\sum_{n=1}^{N_{tm}} i_{L3,Bu}(\frac{n}{N_s}\cdot T_{ac})\cdot \text{V}_{\text{F}}\cdot T_{\text{S}} + \sum_{n=N_{tm}}^{N_s/4} i_{L3,Bo}(\frac{n}{N_s}\cdot T_{ac})\cdot \text{V}_{\text{F}}\cdot\left[1-d_{Bo}(\frac{n}{N_s}\cdot T_{ac})\right]\cdot T_{\text{S}}\right], \tag{29}$$

where V_F is the diode voltage during forward biased. The total diode conduction loss of the inverter is able to be calculated from Equations (28) and (29) and presented as in Equation (30)

$$P_{con,D\_total} = P_{con,D1}\times 2 + P_{con,D3}\times 2. \tag{30}$$

In addition to conduction losses, switching losses also affect the conversion efficiency. The switching losses are mainly composed of switching on loss, switching off loss, and output capacitance loss [24]. The switching on losses of the MOSFETs S_{Bo1} and S_{Bo2} are able to be expressed as in Equation (31):

$$P_{on,Bo1} = P_{on,Bo2} = \frac{2}{T_{ac}}\left[\sum_{n=N_{tm}}^{N_s/4}\frac{\left[\left(\frac{N}{1+N}\right)\cdot V_{in}+\left(\frac{1}{1+N}\right)\cdot v_s(\frac{n}{N_s}\cdot T_{ac})\right]\cdot\left[i_{L1,Bo}(\frac{n}{N_s}\cdot T_{ac})\right]}{2}\cdot\left[\frac{Q_{GS}\cdot R_{Gon}}{(V_{mp,on}+V_{th})/2}+\frac{Q_{GD}\cdot R_{Gon}}{V_{mp,on}}\right]\right], \tag{31}$$

in which R_{Gon} is the resistance of gate-loop during the on state, Q_{GS} is the charge between gate and source, Q_{GD} is the charge between gate and drain, $V_{mp,on}$ is the Miller voltage of the on state, and V_{th} is the threshold voltage of gate. Additionally, the switching off losses of the MOSFETs S_{Bo1} and S_{Bo2} are able to be calculated as in Equation (32):

$$P_{off,Bo1} = P_{off,Bo2} = \frac{2}{T_{ac}} \left[\sum_{n=N_{tm}}^{N_s/4} \frac{\left[\left(\frac{N}{1+N}\right)\cdot V_{in} + \left(\frac{1}{1+N}\right)\cdot v_s\left(\frac{n}{N_s}\cdot T_{ac}\right)\right]\cdot\left[i_{L1,Bo}\left(\frac{n}{N_s}\cdot T_{ac}\right)\right]}{2} \cdot \left[\frac{Q_{GD}\cdot R_{Goff}}{V_{mp,off}} + \frac{Q_{GS}\cdot R_{Goff}}{(V_{mp,off}+V_{th})/2}\right] \right], \quad (32)$$

in which R_{Goff} is the resistance of the gate-loop during off state, and $V_{mp,off}$ is the Miller voltage of off state. Furthermore, using similar calculations, the losses of the switch S_{Bu1} (S_{Bu2}) during switching on and switching off are able to be calculated respectively as in Equations (33) and (34):

$$P_{on,Bu1} = P_{on,Bu2} = \frac{2}{T_{ac}} \left[\sum_{n=1}^{N_{tm}} \frac{V_{in} \cdot \left[i_{L1,Bu}\left(\frac{n}{N_s}\cdot T_{ac}\right)\right]}{2} \cdot \left[\frac{Q_{GS}\cdot R_{Gon}}{(V_{mp,on}+V_{th})/2} + \frac{Q_{GD}\cdot R_{Gon}}{V_{mp,on}}\right] \right]. \quad (33)$$

$$P_{off,Bu1} = P_{off,Bu2} = \frac{2}{T_{ac}} \left[\sum_{n=1}^{N_{tm}} \frac{V_{in} \cdot \left[i_{L1,Bu}\left(\frac{n}{N_s}\cdot T_{ac}\right)\right]}{2} \cdot \left[\frac{Q_{GD}\cdot R_{Goff}}{V_{mp,off}} + \frac{Q_{GS}\cdot R_{Goff}}{(V_{mp,off}+V_{th})/2}\right] \right] \quad (34)$$

The total switch switching loss is able to be calculated from Equations (31)–(34) and presented as in Equation (35):

$$P_{sw,S\_total} = \left(P_{on,Bo1} + P_{off,Bo1} + P_{Coss,Bo1}\right) \times 2 + \left(P_{on,Bu1} + P_{off,Bu1} + P_{Coss,Bu1}\right) \times 2, \quad (35)$$

in which $P_{Coss,Bo1}$ and $P_{Coss,Bu1}$ are the losses of output capacitance of MOSFETs S_{Bo1} and S_{Bu1}, respectively. In accordance with the voltage between drain and source, the characteristic curve illustrated in the datasheet of MOSFET is able to be used for the estimation of both $P_{Coss,Bo1}$ and $P_{Coss,Bu1}$.

Based on above loss analyses, an example with 220 V_{rms} output voltage and 500 W output power (V_M = 312 V, R = 96.8 Ω) is taken to draw the curves of power losses. The curves of inductor conduction loss, switch conduction loss, switch switching loss, and diode conduction loss are illustrated in Figure 9, in which input voltage is between 100 and 200 V. For evaluation, Figure 9 also shows the curves of a grid-tied system with two-stage energy processing (cascading a boost converter and an H-bridge SPWM inverter).

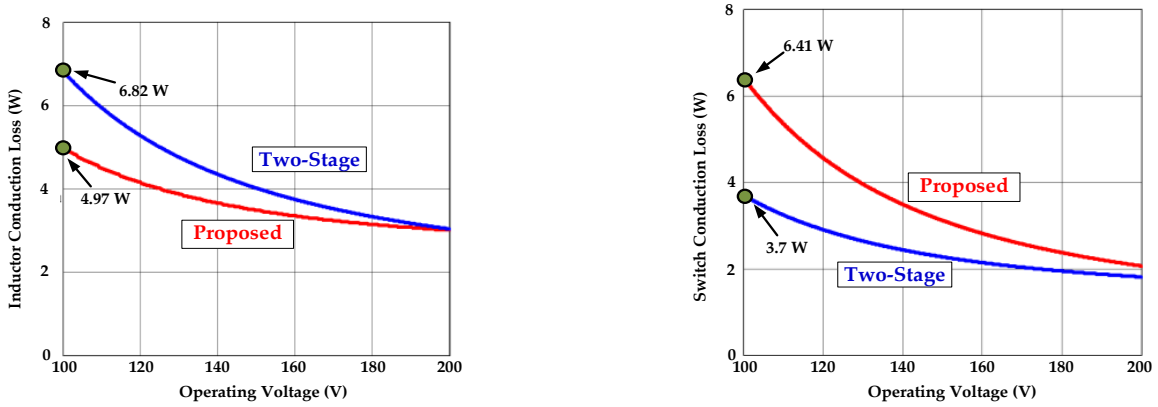


Figure 9. *Cont.*

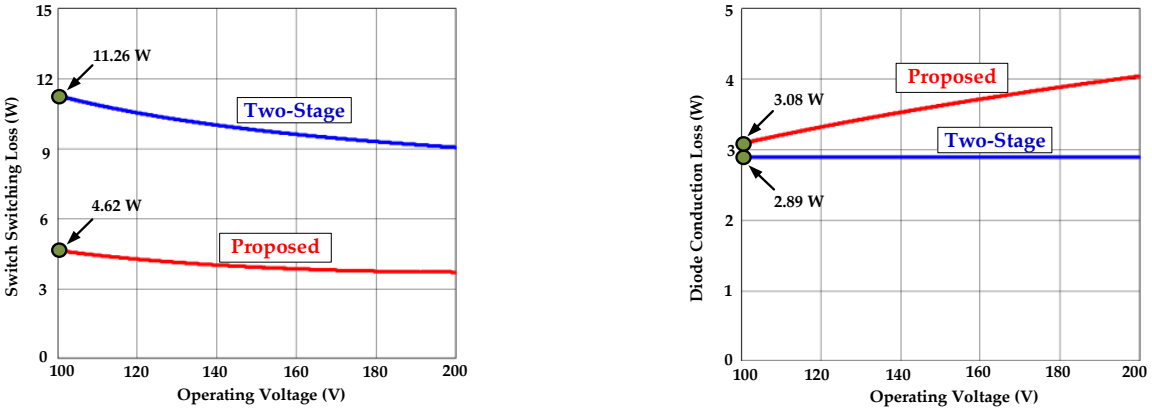


Figure 9. The power loss comparison curves of the proposed inverter and the traditional two-stage system: (**a**) conduction loss of all inductors; (**b**) conduction loss of all switches; (**c**) switching loss of all switches; (**d**) conduction loss of all diodes.

It is able to be understood from Figure 9a; since the investigated inverter does not need to boost the voltage to 400 V, it has lower total conduction loss of inductors. Figure 9b shows the curves of the total conduction loss of the switches based on Equations (24)–(27). When the input voltage is low, the high input current needs to go through the switch S_{Bu1} or S_{Bu2} in the step-up mode, resulting in slightly higher conduction loss of the switches. It is able to be seen from the switching loss curves shown in Figure 9c that since the proposed converter only requires a single stage of energy processing and only one switch performs high-frequency switching in each state, the switching losses are greatly improved. Figure 9d shows the curves of the total conduction loss of the diodes based on Equations (28)–(30). Since the diodes D_1 and D_2 only conduct in the step-down mode, the total diode conduction loss is lower at low input voltage. When the input voltage increases, the operation time of the step-down mode increases, and the total diode conduction loss increases accordingly. The traditional two-stage system only uses one diode in the boost converter, and the output voltage is a high voltage of 400 V, so it has lower diode conduction loss. Overall, under the condition of 100 V input, the total loss of the investigated inverter is 19.08 W, and the total loss of the traditional two-stage grid-tied system is 24.67 W. Therefore, it is able to be known that the total power loss of the investigated inverter can be reduced to improve conversion efficiency.

5. Experimental Results

To prove the correctness of the previous analysis, a prototype is built and measured according to the schematic illustrated in Figure 3 and the specifications shown in Table 2.

Table 2. Electrical specifications of the laboratory prototype.

Specifications	
Input voltage, V_{in}	100–200 V
Voltage of mains, v_s	220 V_{rms}
Frequency of mains, f_{ac}	60 Hz
Frequency of switching, f_s	20 kHz
Rated power, P_o	500 W

For avoiding the duty ratio being too large, its maximum value is set to 0.45. Since the maximum duty ratio occurs at the peak output voltage of 312 V and the minimum input voltage of 100 V, the turn ratio N can be calculated from Equation (7) as around 1.6. In the design example, the turn ratio N of 1.5 is chosen.

By combining Equations (9) and (11), the BCM inductance L_B is able to be obtained as in Equation (36):

$$L_B = \frac{R \times d_{Bo}(1 - d_{Bo})^2}{2(1 + N)(1 + Nd_{Bo}) \times f_S} \tag{36}$$

By selecting the inductor current to be BCM at the peak of sinusoidal voltage and 50% rated power, the BCM inductance L_B is able to be obtained from Equation (36) as 155 µH. In the implementation example, 200 µH is chosen for the inductance of L_1 and L_2. Table 3 shows the selected component parameters according to the analysis and design addressed before.

The investigated transformer-less buck-boost grid-tied inverter is controlled by SPWM. Figure 10 illustrates the experimental waveforms of the output voltage v_o and the driving signals of the switches S_{Bu1}, S_{Bo1}, and S_1. When the inverter operates in the step-down mode, the switch S_{Bu1} is switched at high frequency, and the switches S_{Bo1} remain off. Conversely, when the inverter operates in the step-up mode, the switch S_{Bo1} performs high-frequency switching. The switch S_1 continuously conducts during the positive half-cycle to provide an energy transmission path. During the negative half-cycle, the switch S_2 replace the switch S_1 to conduct continuously, and the switch S_1 remains off.

Table 3. Component parameters of the laboratory prototype.

Component Parameters	
Input capacitor, C_{dc}	3300 µF
MOSFETs	47N60C3
Pwer diodes	C3D10060A
Turn ratio, N	1.5
Inductors, L_1, L_2	200 µH
Inductors, L_3, L_4	450 µH
Capacitor of filter, C_f	5 µF
Inductor of output, L_s	1 mH
Capacitor of output, C_s	5 µF

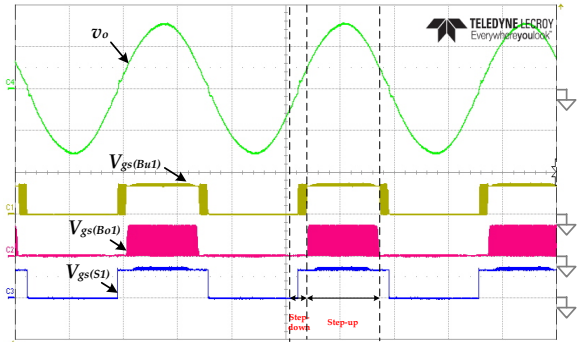


Figure 10. The experimental waveforms of the output voltage v_o and the gate-driving signals under the condition of 100 V input voltage and 500 W load. (v_o: 200 V/div; V_{gs}: 20 V/div; time: 5 ms/div).

Under the condition of 100 V input voltage and 500 W load, Figure 11 illustrates the experimental waveforms of the input voltage V_{in}, the output voltage v_o, and the output current i_o. It can be seen that v_o and i_o are low-distortion and close to an ideal sinusoidal wave. These results verify that the proposed buck-boost grid-tied inverter can achieve the function of DC to AC conversion. Figure 12 illustrates the experimental waveforms of the output voltage v_o, and the inductor currents i_{L1}, i_{L3}. As shown in Figure 12a, the step-down mode is performed when the instantaneous voltage of v_o is below 100 V; on the contrary, the step-up mode is performed. The inductor currents i_{L1}, i_{L3} are in CCM to reduce current peaks and ripple. Figure 12b shows zoom-in waveforms on the peak of output voltage. It can be seen that the inductor L_1 is charging alone and discharging in series with the

inductor L_3, which can effectively increase voltage gain. Figure 13 shows the simulation waveforms of the output voltage v_o and the leakage current under the condition of 100 V input voltage and 500 W load. These waveforms prove that the proposed inverter can effectively suppress the leakage current of the PV panel.

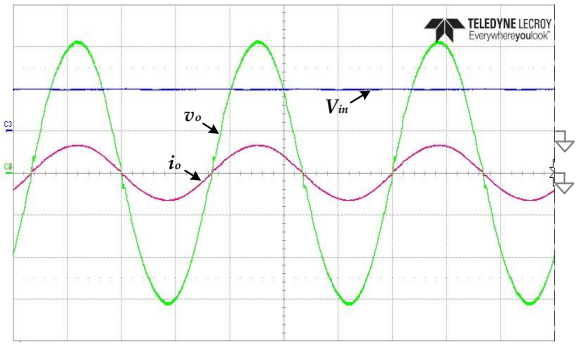


Figure 11. The experimental waveforms of the input voltage V_{in}, the output voltage v_o, and the output current i_o under the condition of 100 V input voltage and 500 W load (V_{in}, v_o: 100 V/div; i_o: 5 A/div; time: 5 ms/div).

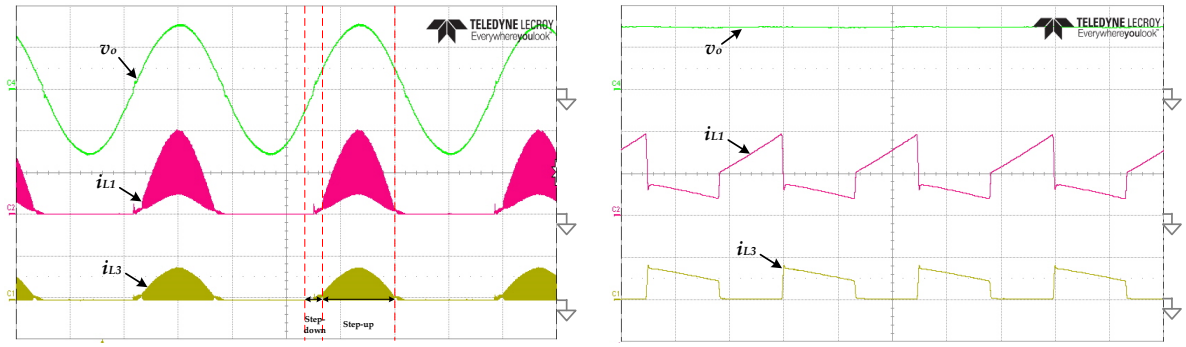


Figure 12. Under the condition of 100 V input voltage and 500 W load, the experimental waveforms of the output voltage v_o and the inductor currents i_{L1}, i_{L3}: (**a**) complete AC period (v_o: 200 V/div; i_{L1}, i_{L3}: 10 A/div; time: 5 ms/div); (**b**) zoom-in on the peak of the output voltage (v_o: 200 V/div; i_{L1}, i_{L3}: 10 A/div; time: 20 µs/div).

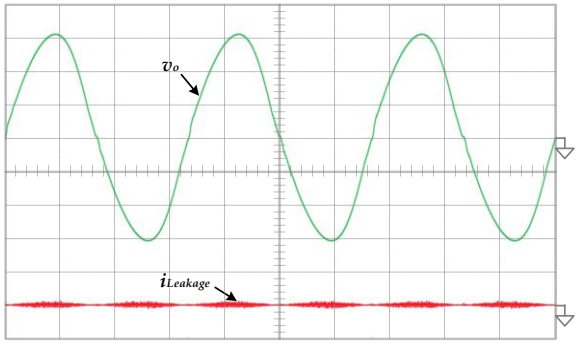


Figure 13. The simulation waveforms of the output voltage v_o and the leakage current $i_{Leakage}$ under the condition of 100 V input voltage and 500 W load (v_o: 100 V/div; $i_{Leakage}$: 100 mA/div; time: 5 ms/div).

Moreover, the laboratory prototype is further measured with 200 V input voltage to verify its suitability for a wide range of input voltage applications. Figure 14 illustrates the experimental waveforms of the output voltage v_o and the driving signals of the switches

S_{Bu1}, S_{Bo1}, and S_1. The modulation method is similar to that at 100 V input, but the operation time of the step-down mode becomes longer, and the operation time of the step-up mode becomes shorter.

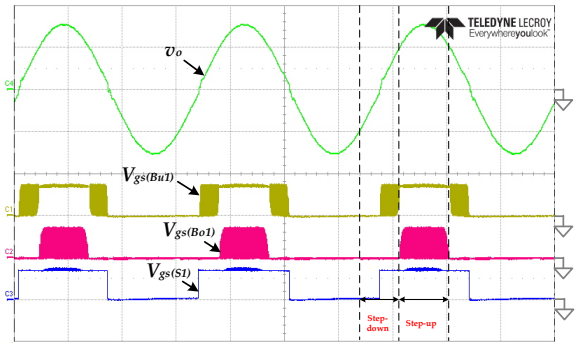


Figure 14. The experimental waveforms of the output voltage v_o and the gate-driving signals under the condition of 200 V input voltage and 500 W load (v_o: 200 V/div; V_{GS}: 20 V/div; time: 5 ms/div).

Figure 15 illustrates the experimental waveforms of the input voltage V_{in}, the output voltage v_o and the output current i_o under the condition of 200 V input voltage and 500 W load. As can be seen, v_o and i_o are also low-distortion and close to the ideal sinusoidal wave, which indeed verifies the feasibility for the applications with wide-range input voltage. Figure 16 illustrates the experimental waveforms of the output voltage v_o, and the inductor currents i_{L1}, i_{L3} under the same conditions. At Figure 16a, due to the higher input voltage, the peak of inductor currents is lower than those at 100 V input voltage. Figure 16b illustrates zoom-in waveforms of the inductor currents i_{L1}, i_{L3} on the peak of output voltage. It can be seen that the inductor L_1 is still charging alone and discharging in series with the inductor L_3. Figure 17 illustrates the simulation waveforms of the output voltage v_o and leakage current under the condition of 200 V input voltage and 500 W load. It can be seen that the leakage current can still be effectively suppressed under 200 V input voltage.

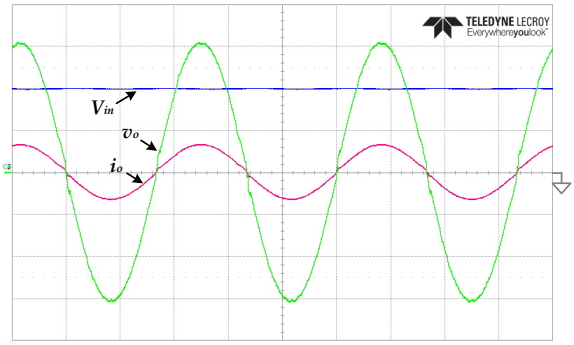


Figure 15. The experimental waveforms of the input voltage V_{in}, the output voltage v_o, and the output current i_o under the condition of 200 V input voltage and 500 W load (V_{in}, v_o: 100 V/div; i_o: 5 A/div; time: 5 ms/div).

The measured odd-order harmonics and total harmonic distortion (THD) of the inverter output under 100 V and 200 V input voltages are collected in Table 4. The data meet the requirements of international electrical standards; it is able to verify the feasibility of the investigated inverter. Figure 18 illustrates the experimental efficiency curves of the laboratory prototype, in which the efficiency is up to 95% at 100 V input and 96.7% at 200 V input, respectively. These results further confirm that high conversion efficiency can be achieved by the investigated inverter with a single stage of energy processing. Figure 19 shows the picture with the experimental test bench. The development board of

dsPIC33FJ16GS504 generates SPWM driving signals, and the wire-wound resistor is used as testing loads.

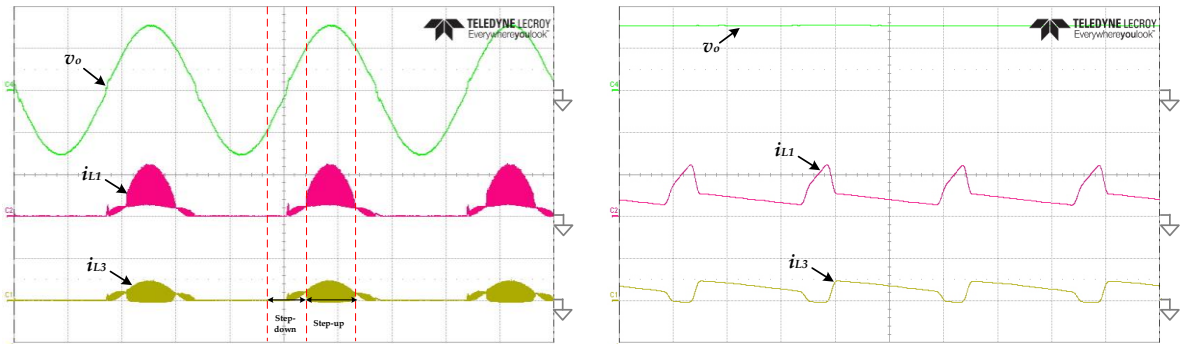


Figure 16. Under the condition of 200 V input voltage and 500 W load, the experimental waveforms of the output voltage v_o and the inductor currents i_{L1}, i_{L3}: (**a**) complete AC period (v_o: 200 V/div; i_{L1}, i_{L3}: 10 A/div; time: 5 ms/div); (**b**) zoom-in near the peak of the output voltage (v_o: 200 V/div; i_{L1}, i_{L3}: 10 A/div; time: 20 µs/div).

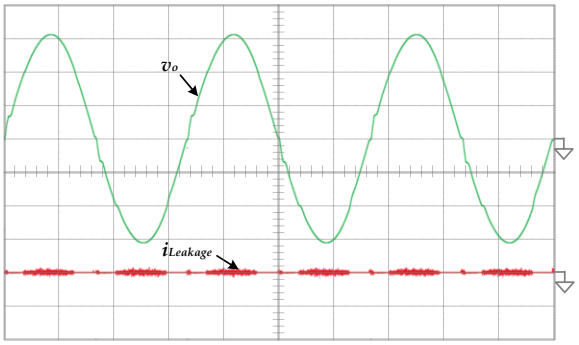


Figure 17. The simulation waveforms of the output voltage v_o and the leakage current $i_{Leakage}$ under the condition of 200 V input voltage and 500 W load (v_o: 100 V/div; $i_{Leakage}$: 100 mA/div; time: 5 ms/div)

Table 4. Measured harmonics and THD of the inverter output.

Harmonics	100 V	200 V
THD	1.34%	1.10%
Harmonic of 3rd	1.18%	0.79%
Harmonic of 5th	0.43%	0.53%
Harmonic of 7th	0.13%	0.22%
Harmonic of 9th	0.12%	0.18%
Harmonic of 11th	0.09%	0.15%

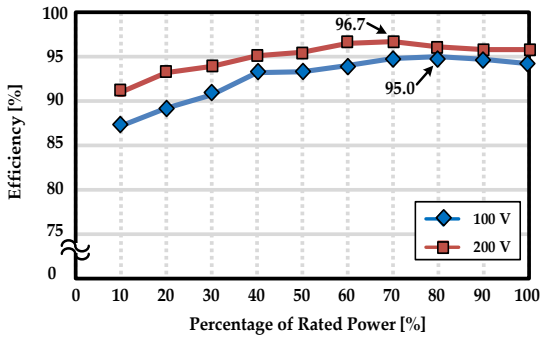


Figure 18. Measured efficiency curves of the laboratory prototype.

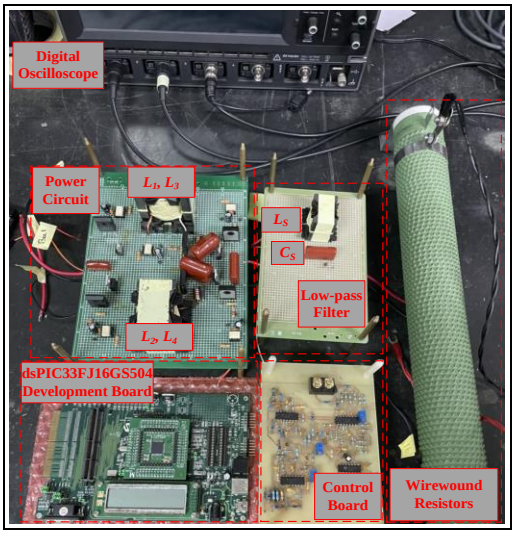


Figure 19. The picture with the experimental test bench.

6. Discussions

According to the experimental waveforms above, the feasibility of the proposed inverter has indeed been verified. In order to further summarize its main contributions and discuss the performance in terms of loss, efficiency, cost, and harmonic distortions, the following discussions are carried out.

The traditional PV grid-tied system is composed of a boost converter and a H-bridge inverter. Due to the two-stage energy processing, the system efficiency is reduced. The proposed inverter only needs single energy processing, and only one power switch performs high frequency switching, improving the conversion efficiency effectively. By adding coupled inductors, the voltage gain of the inverter can be increased, which is suitable for low input voltage applications. The inverter has both step-up and step-down functions so that it is suitable for PV systems with wide-range input-voltage fluctuation.

Based on the results of the previous loss analysis, the expected full load efficiency should be 96.3%. The measured full load efficiency of 100V input shown in Figure 18 is about 94.7%, which is slightly lower than the expected result. This is because only the power losses of the main power components at room temperature is considered in the loss analysis. Long-time operation increases the junction temperature and on-resistance of power semiconductor components, resulting in increase of power loss. In addition, the conduction loss of the copper wire in the circuit layout should be of considerable proportion, but it is not included in the loss analysis.

Table 5 shows comparisons between the proposed buck-boost inverter and the traditional two-stage grid-tied system. Since the proposed inverter requires only a single stage of energy processing, its measured full-load efficiency can be as high as 94.7%. In the two-stage system, even if the efficiencies of the boost converter and the inverter are both up to 97%, the overall efficiency is only about 94.1%, which is lower than the proposed inverter. The proposed inverter has the beneficial feature of reduced voltage stress of power switches, which is favorable for reducing the cost of power components. Although the proposed inverter requires a higher number of components, the overall cost is only slightly higher than the two-stage system. Since the proposed inverter has both step-up and step-down capabilities, and it has high voltage gain, its operable input voltage range is relatively wide. In addition, since the proposed inverter and the traditional two-stage system both have an output low-pass filter, their total harmonic distortions can be lower than 2% to meet electrical specifications.

Table 5. Comparisons between the proposed inverter and the traditional two-stage system.

Item	Proposed Inverter	Two-Stage System
Circuit Topology	A Buck-Boost Grid-Tied Inverter	A Boost Converter in series with an H-Bridge Inverter
Number of Energy Processing	Single	Twice
Full Load Efficiency (100 V Input)	94.7%	<94.1%
Number of Power Switches	6	5
Number of Power Diodes	4	1
Number of Magnetic Components	3	2
Voltage Stress of Power Components	Low	High
Cost	Slightly Higher	Moderate
Volatge Gain	High	Moderate
Input Voltage Range	Wide	Narrow
THD	<2%	<2%

7. Conclusions

In this article, the development and the implementation of the transformer-less buck-boost grid-tied inverter with low leakage-current and high voltage-gain have been successfully achieved. Two dual-switch buck-boost converters with coupled inductors are connected in parallel to generate unipolar half-waves, and two low-frequency switches are adopted to switch the output polarity. By adding coupled inductors, the voltage gain can be effectively increased, so the proposed inverter is suitable for a wide range of input-voltage applications. Since only single energy processing is required, and only one MOSFET performs high-frequency switching in each mode, switching losses and efficiency can be effectively improved. In addition, the two unfolding switches can also provide a path for connecting the mains to the negative end of the input voltage, so that the leakage current of the PV array can be effectively suppressed. Finally, an experimental prototype was constructed, and corresponding measurements were made to verify the validity of the circuit structure of the investigated inverter.

Author Contributions: Conceptualization, C.-H.C.; methodology, C.-H.C.; software, Y.-F.C.; validation, Y.-F.C.; formal analysis, C.-H.C.; investigation, C.-H.C.; resources, C.-H.C.; data curation, Y.-F.C.; writing—original draft preparation, C.-H.C.; writing—review and editing, C.-H.C.; visualization, C.-H.C.; supervision, C.-H.C.; project administration, C.-H.C.; funding acquisition, C.-H.C. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

BCM	boundary conduction mode
CCM	continuous conduction mode
CMV	common mode voltage
DCM	discontinuous conduction mode
ESR	equivalent series resistance
MOSFET	metal-oxide-semiconductor field-effect transistor
MOST	Ministry of Science and Technology

PV	photovoltaic
SPWM	sinusoidal pulse-width modulation
THD	total harmonic distortion

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