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A Fault Tolerant Voter for Approximate Triple Modular Redundancy

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Abstract: Approximate Triple Modular Redundancy has been proposed in the literature to overcome the area overhead issue of Triple Modular Redundancy (TMR). The outcome of TMR/Approximate TMR modules serves as the voter input to produce the final output of a system. Because the working principle of Approximate TMR conditionally allows one of the approximate modules to differ from the original circuit, it is critical for Approximate TMR that a voter not only be tolerant toward its internal faults but also toward faults that occur at the voter inputs. Herein, we present a novel compact voter for Approximate TMR using pass transistors and quadded transistor level redundancy to achieve a higher fault masking. The design also targets a better Quality of Circuit (QoC), a new metric which we have proposed for highlighting the ability of a circuit to fully mask all possible internal faults for an input vector. Comparing the fault masking features with those of existing works, the proposed voter delivered upto 45.1%, 62.5%, 26.6% improvement in Fault Masking Ratio (FMR), QoC, and reliability, respectively. With respect to the electrical characteristics, our proposed voter can achieve an improvement of up to 50% and 56% in terms of the transistor count and power delay product, respectively.

Keywords: fault tolerance; voter; triple modular redundancy (TMR); approximate TMR (ATMR)

1. Introduction

The Integrated Circuit (IC) industry is on the verge of one of its most crucial eras. Despite the pros of extra density and potential performance of ICs, the cons of increasing complexity and likelihood of higher number of faults are also inevitable [1,2]. The quest for reliability, the probability of not incurring a failure within the given operation period, has become a vital aspect for circuit designers and manufacturers [3,4]. The International Technology Roadmap for Semiconductors has reported that reliability is a challenge for nano-electronics owing to the technological issues posed by the ever-shrinking semiconductor devices [5]. Thus, the next generation of very deep sub-micron systems will be defined by their reliability and performance [1]. For a realistic analysis of the reliability, fault modeling must be conducted at the transistor level [6].

Primarily, fault prevention and fault tolerance are sought to yield reliable digital systems. Fault prevention aims at a priori elimination of all faults in which the system practically targets an acceptably low chance of failure [1]. Fault tolerance is the ability of a system to mitigate faults that arise during an operation. Fault tolerance is the assurance of a correct operation despite a fault occurrence, and thus signifies a higher reliability. When it is ensured that the occurrence of an internal or external fault does not affect the actual output of a function module, the fault is known to be masked or efficaciously hidden from observation by the outside world. A fault that does not cause an error is said to be masked. This phenomenon is referred to as fault masking. If a fault is not masked, it will lead to an erroneous output of the function module. In brief, the manifestation of a fault is construed

to be an error [7,8]. Fault tolerance is augmented into the system for the purpose of fault masking through the inclusion of redundancy techniques such as Triple Modular Redundancy (TMR) [9].

TMR guarantees an accurate output through a majority voter, even when a single module is faulty. TMR is one of the most general and effective hardening techniques. However, TMR suffers from a 200% area overhead problem [10,11]. Previous works on fault tolerance techniques have proposed the use of selective hardening methods such as Partial TMR [12], Selective TMR [13] and Approximate TMR (ATMR) [11,14,15] to overcome this area overhead issue of TMR without significantly compromising the fault masking. In the concept of selective hardening, the word 'Selective' implies that the protection method is providing full protection to selected part of the circuit/system. The simple idea behind selective hardening is that if hardening an entire circuit is too expensive, we can harden only those circuit parts that are particularly exposed to failure or that are critical for correct system functioning [13]. Selective hardening, Selective TMR, and ATMR have the same goal that is full protection of critical parts of the system. Selective TMR, partial TMR, and ATMR benefits from the insertion of TMR in the nodes that present a greater vulnerability to single event upsets (SEUs) [16]. In the case of ATMR, TMR uses approximated logic circuits to generate redundant modules that are optimized for the area, as compared to the original module. This idea consists of generating approximate logic circuits with reduced resource use while maintaining full protection against the most critical parts of the system and no approximations are made in that region. ATMR provides an additional level of selective hardening as depicted by Figure 1.

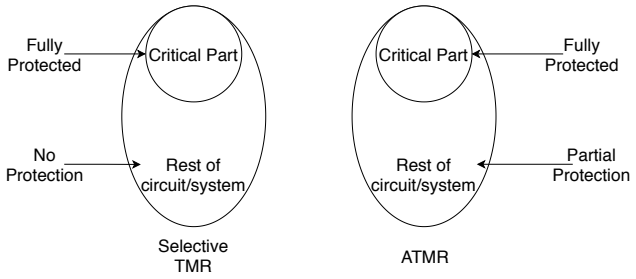

Figure 1. Selective Hardening: Selective TMR & ATMR.

For hardening purposes, the criticality of an application defines the choice of trade-off between a reliability enhancement and the cost allied with a fault tolerant design. Certainly, maintaining the balance between cost-budget and acceptable error rate constraint is imperative [17]. The experiments carried out in space also present a case of selective hardening. For instance, radiation hardened modules such as the LEON-FT microprocessor are used in spacecraft's mission-control computer whereas the scientific gadgets are mostly developed over commercial-off-the-shelf (COTS) parts with slight or no fault protection. This owes to the facts that radiation-hardened equivalents of the COTS parts, if accessible at all, tend to have a lower performance and consume more power, which is a limited resource in a spacecraft, than the COTS parts. The threat of an individual experiment failing might be tolerable, but a critical failure in an on-board mission control system could condense all experiments and complete mission useless [13].

Please note that a voter is integral to both TMR and ATMR. Because the final output is produced by a voter, a faulty voter poses a direct threat to the system reliability. Research on fault tolerant voters [1,2,8,18] have mainly focused on TMR. In [1,8,18] the fault tolerance ability of TMR voters was evaluated at the gate level, whereas [2] assessed fault-tolerant voters at the transistor level while assuming that each module of TMR produces an accurate output.

Since ATMR is a recent notion, voter design for ATMR has not been proposed in literature. In this work, we present a novel fault-tolerant voter for ATMR. Like conventional majority voters, the proposed voter produces an exact output. Hence, it can also be used in a TMR system. The contributions of our work are as follows:

- We highlight the reliability of ATMR, in contrast with TMR.

- A compact, low-power, high-speed, and fault-tolerant voter for ATMR is designed.
- A new metric, Quality of Circuit (QoC), is proposed. It holds immense significance to have prior insight of a circuit's intrinsic aptitude towards assurance of fault free output for certain input vectors. Hence, we present a metric that acknowledges the inherent capability of a digital circuit to mask all possible internal faults for a given input vector.
- We present a transistor-level analysis of fault-tolerant voters, considering all possible states of the voter inputs and evaluate them through a comparison with the proposed voter.

The rest of the paper is organized as follows. Section 2 provides the motivation of the present research based on the concepts of TMR, ATMR, voters, and reliability. Section 3 presents our design of a fault-tolerant voter for ATMR. Section 4 provides comparative analyses of fault tolerant voters and highlights the need for a QoC metric, followed by our conclusions in Section 5.

2. Motivation

2.1. TMR, Voter, and Reliability

In a TMR system, the original module is replicated three times, and the output of each module is fed into a voter. The voter produces the final output of the system based on the majority votes.

In case of a TMR system, if a single fault occurs that flips one of the voter inputs, the output of the voter will still be correct because the other inputs will agree with each other and produce the correct output. When two inputs of the voter are 0, a faulty input will be 1. However, since 0 holds the majority as input, the voter will output a 0 and mask the fault. Under such a scenario, the possible faulty input combinations are as follows: 001, 010, 100. Similarly, when two inputs of the voter are 1, a faulty input will be 0. In this case, the possible faulty input combinations are 011, 110, 101. Thus, the faults will be masked for faulty input conditions, i.e., 001, 010, 100, 011, 110, 101. Figure 2 illustrates the TMR phenomenon, where 000 and 111 are fault-free states. It would be safe to state that faults occurring within the voter circuit that propagates to the output are fatal to TMR.

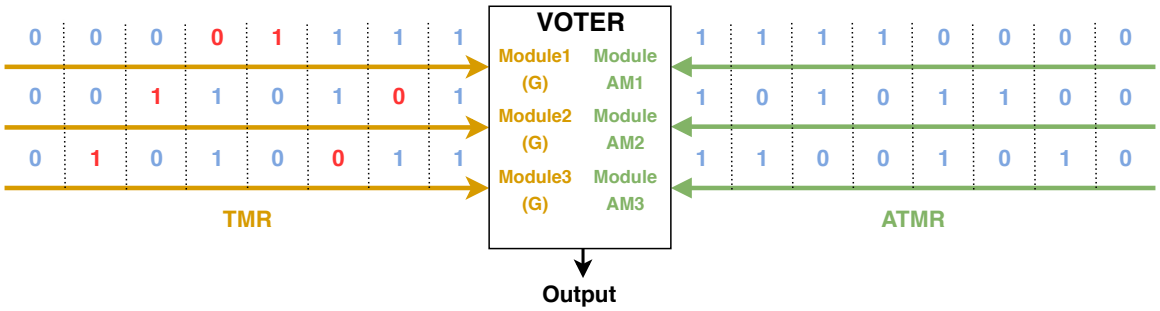

Figure 2. Input Vectors for Voter.

Reliability is the probability of no failure occurring within a given period of operation. The non-faulty state of a function module is represented as R_M, where R_M is the probability that a module will generate a correct output and is an exponential function of time with a constant failure rate λ [8,18]. Mathematically, R_M can be defined as $R_M = e^{-\lambda t}$. Consider the simplest system reliability model for a system with n modules. If the module reliability is R_M with a constant-failure rate λ, the system reliability, *Rsys*, is then given by [1]

$$Rsys(t) = [R_M(t)]^n = [e^{-\lambda t}]^n \quad (1)$$

As in case of TMR, all digital modules are independent and identical, and the reliability of TMR can be then determined as a function of the reliability R_M of a single module, assuming that the voting

circuitry does not fail. Furthermore, the systems will function properly if any two modules operate appropriately. The reliability of TMR can be given as follows:

$$\begin{aligned} R_T = {} & \text{Probability of all three modules functioning +} \\ & \text{Probability of any two modules functioning} \end{aligned} \tag{2}$$

$$R_T = B(3:3) + B(2:3) \tag{3}$$

$$= \binom{3}{3} R_M^3 (1-R_M)^0 + \binom{3}{2} R_M^2 (1-R_M)^1 \tag{4}$$

$$= 3R_M^2 - 2R_M^3 \tag{5}$$

$$= 3e^{-2\lambda t} - 2e^{-3\lambda t} \tag{6}$$

Considering the reliability of a voter R_v, then

$$R_{TMR} = R_{voter} R_T \tag{7}$$

$$= R_{voter}(3e^{-2\lambda t} - 2e^{-3\lambda t}) \tag{8}$$

This shows that the failure of a voter will simply mean the failure of TMR even if all modules are functioning correctly.

2.2. ATMR, Voter, and Reliability

ATMR can be developed using approximate modules for all three modules of TMR. The output of the approximate modules differs from the original module for some of the input vectors, which helps in complexity reduction. The working principle for ATMR is as follows [10]:

"*Only one of the approximate modules can differ from the original circuit at each input vector scenario, allowing the majority voter to still select two match outputs out of three for any input vectors*".

Consider an original module G with inputs I, J, and K. The truth table of G is given in Table 1. An approximate module (AM) of G, AM1, is produced by complementing the output of G for $\bar{I}J\bar{K}$. Another approximate module of G, AM2, is produced by complementing the output of G for $I\bar{J}K$ and IJK. The third approximate module of G, AM3, is produced by complementing the output of G for $\bar{I}\bar{J}\bar{K}$. It can be seen from Table 1 that AMA1 differs from G at $\bar{I}J\bar{K}$ and produces a value of 1. Similarly, AM2 differs from G at $I\bar{J}K$ and IJK, whereas AM3 differs from G at $\bar{I}\bar{J}\bar{K}$. An ATMR is formed by AM1, AM2, and AM3 where these approximate modules provide input to the voter that produces the final output. It can be seen from the example that the voter output is the same as that of G because the validity of the working principle of ATMR is maintained despite approximate modules being used to form the TMR. The vectors corresponding to $\bar{I}\bar{J}\bar{K}$, $\bar{I}J\bar{K}$, $I\bar{J}K$, and IJK, i.e., 000, 010, 101, and 111, are called unprotected vectors.

Table 1. Approximate TMR: An Example.

Input Vectors			Original Circuit	Approximate	Approximate TMR Approximate	Approximate	Voter Output
I	**J**	**K**	**Output (G)**	**Module 1 (AM1=A)**	**Module 2 (AM2=B)**	**Module 3 (AM3=C)**	**[ATMR Output]**
0	0	0	1	1	1	0	1
0	0	1	0	0	0	0	0
0	1	0	0	1	0	0	0
0	1	1	0	0	0	0	0
1	0	0	1	1	1	1	1
1	0	1	1	1	0	1	1
1	1	0	1	1	1	1	1
1	1	1	0	0	1	0	0

Now, assume that the three modules of ATMR are fault-free. Fault-free conditions for ATMR, as depicted in Figure 2, are 000, 001, 010, 100, 011, 101, 110, 111. This is because ATMR permits one of the approximate modules to differ from the original circuit at each input vector scenario. Thus, there will necessarily be cases in which two inputs of the voter will be the same, and one input will be different from them. Under such a scenario, if a fault occurs at the voter input it could be unfavorable for the ATMR system. Please note that the suitability of ATMR is application dependent as the application or design engineer can distinguish between critical and non-critical parts of a system and sensibly adapt ATMR. A TMR voter does not face this situation because this condition primarily exists owing to the working principle of the ATMR. Previously proposed fault tolerant voters [1,8,18] will still produce an erroneous output for unprotected vectors under such conditions because this is out of the scope for the TMR voter design. For example, in Table 1, when input vector $\bar{I}J\bar{K}$ is considered, the original circuit should produce a value of 1 at the output. For TMR, if one of the inputs fed to voter is flipped, the remaining two inputs will cover for it to produce a fault-free output of 1. For the ATMR in Table 1, $AM1$ and $AM2$ vote to propagate a value of 1 to the output despite $AM3$ producing a value of 0. If a fault occurs at the input of the voter fed from AM1, 1 is flipped to 0, and AM1 and AM3 will vote a faulty output of 0.

For ATMR, all digital modules are independent. Furthermore, the systems will only function properly if all modules work appropriately. The reliability of the ATMR (R_{AT}) and ATMR with voter (R_{ATMR}) can be respectively given as follows:

$$R_{AT} = \text{Probability of all three modules functioning} \tag{9}$$

$$R_{AT} = \binom{3}{3} R_M^3 (1 - R_M)^0 \tag{10}$$

$$= R_M^3 = e^{-3\lambda t} \tag{11}$$

$$R_{ATMR} = R_{voter} R_{AT} \tag{12}$$

$$= R_{voter}(e^{-3\lambda t}) \tag{13}$$

It is quite evident from (8) and (13) that the reliability of ATMR is much lower compared to that of TMR. It is of immense significance to have reliable voters and reliable ATMR modules. Hence, it is imperative to design a fault tolerant voter for ATMR which should not only be able to mask faults that occur inside the voter circuit but also, the voter input needs to be fault free.

3. Fault-Tolerant Voter for ATMR

ATMR is meant to overcome the area overhead issue of TMR. Hence, any application that opts to adopt ATMR must be sensitive to the area consumption. Thus, as a pre-requisite, a voter for ATMR should be designed such that it occupies the minimum area. This design aspect is one of our forte.

With respect to fault tolerance, as discussed earlier, a voter for ATMR should be tolerant toward (a) faults occurring within the voter circuit nodes (internal outputs) and (b) the faults flipping the inputs of the voter.

To limit faults occurring at the circuit nodes, a circuit with the minimum nodes is endorsed. According to [18], a voter with less transistors, and hence less nodes, has a lower probability of having an internal fault. The work concluded that a voter with less transistors has a higher probability that the TMR system will operate correctly. In a similar fashion, we propose a fault-tolerant voter for ATMR by using pass transistor logic (PTL) to keep the number of transistors to a minimum. In PTL, the primary inputs drive the gate and source/drain terminals, which leads to the use of a reduced number of transistors for logic implementation. The use of a pass transistor helps in decreasing the possible faulty nodes within the circuit. Please note that only single node faults are considered, which implies that only one internal node of the entire circuit is faulty at a given time.

Faults flipping the inputs of the voter behave such that an input stuck-at-1 (s-a-1) fault of the gate terminal of an NMOS transistor causes a closing of the path between the drain and its source of it.

An input stuck-at-1 (s-a-1) fault to the gate terminal of a PMOS transistor causes in opening of the path between the drain and its source. An input stuck-at-0 (s-a-0) fault to an NMOS transistor results in an opening of the path between the drain and source. An input stuck-at-0 (s-a-0) fault at a PMOS transistor results in a closed path between the drain and source. References [19,20] proposed the use of Quadded Transistor redundancy and Triple Transistor redundancy, respectively, for the provisioning of input fault tolerance. For the proposed voter faults, flipping of the inputs of the voter is handled using the redundancy technique of [19]. As the number of transistors is kept to a minimum using pass transistors, unlike in previous studies, this provides us with the freedom to introduce transistor-level redundancy for the voter inputs. However, the use of pass transistors brings about certain design constraints and not every transistor can be made redundant. This is because NMOS produces a weak 1 and PMOS produces a weak 0. Hence, the outputs do not have a full voltage swing (low noise margin), and additional drivers may be needed.

For design simplicity, redundancy for all transistors with inputs A and B is introduced. It is ensured that any single transistor fault will not change the logic behavior and the fault will be tolerated. The redundancy is provided though quadded transistors, which has higher reliability than triple redundancy [20]. In a quadded redundancy technique, a transistor with gate input A is replaced with a four-transistor structure, as shown in Figure 3. Two transistors are connected in parallel $(A + A)$ with gate input A. Two such structures are then connected in series $(A + A)(A + A)$. This configuration of quad transistor is opted because each quad structure has an effective resistance equal to that of a single transistor [19]. Hence, a quadded structure implements the logic function $(A + A)(A + A)$ and $(B + B)(B + B)$ for A and B inputs, respectively, in the proposed voter, as shown in Figure 4e. No single transistor fault will change the logic behavior, and the fault will be tolerated. Furthermore, double s-a-0 (NMOS)/s-a-1 (PMOS) are tolerated if they do not occur in any two parallel transistors. Double s-a-1 (NMOS)/s-a-0 (PMOS) are tolerated if they do not occur in any two series transistors. In addition, any triple fault that does not include two parallel s-a-0 (NMOS)/s-a-1 (PMOS) transistors or two series s-a-1 (NMOS)/s-a-0 (PMOS) transistors is tolerated [19].

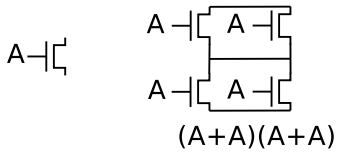

Figure 3. Quadded Redundancy: $(A + A)(A + A)$ [19].

The proposed voter design is presented in Figure 4e. The main design transistors are Tp1, Tp5, Tn3, Tn7, Tp9, and Tn9. Tp1, gated by A, is made redundant through Tp2, Tp3, and Tp4. Similarly, Tp5 with B as an input has a redundancy provision through Tp6, Tp7, and Tp8. Tn3 has a gate input of B and source input of A. This transistor is made redundant through Tn1, Tn2, and Tn4. Similarly, Tn7 has redundancy through Tn5, Tn6, and Tn8. The output is produced through a mux. Because the gate inputs of mux are driven by 0/1 produced through the pass transistors, owing to the design constraints, redundancy is not provided here. All transistors, except for two at the output stage, are made redundant. This input level redundancy facilitates an ATMR structure because the voter inputs of ATMR can differ from each other under a fault-free condition, and an input fault will simply lead to a faulty output. For instance, consider the case of ATMR in Table 1, where the input vector is $\bar{I}J\bar{K} = 010$. Now, the voter inputs are $A = AM1 = 1$ and $B = C = AM2 = AM3 = 0$. In this case, the fault-free voter should output a 0. Assuming that B at Tp5 is stuck at 1 and that the transistor behaves like an open switch, in this case Tp6, Tp7, and Tp8 will work as a closed switch to ensure a fault-free final output.

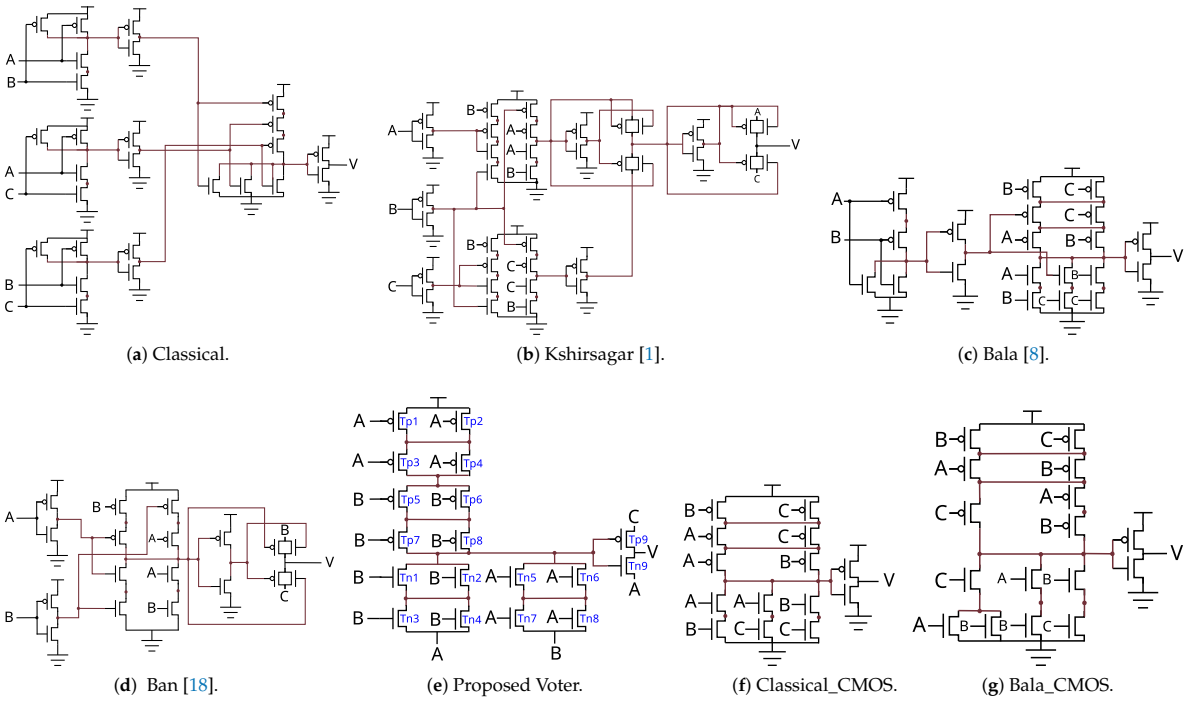

Figure 4. Voters Architectures.

4. Analysis of Fault-Tolerant Voters

4.1. Simulation Setup

The fault masking capability of proposed voter for ATMR is evaluated by testing the design for stuck at faults. The voter is simulated with single fault using ModelSim through Verilog. In Verilog, a Single Event Transient (SET) is emulated by forcing a change in the state of the node by means of the force/release command. This simulated SET pulse is only logical, and therefore the sizing the electrical and temporal masking is not evaluated [10]. Thus, to test the voter circuit, force/release is exhaustively used at each node. The simulation setup, as shown in Figure 5, is similar to that of ATALANTA [21], which enumerates those input vectors where a fault propagates to the output at the gate-level. In our case, as shown in Figure 5, the design is assessed at the transistor level. Each node, one at a time, is introduced with a fault and all possible input vectors are applied. Finally, those input vectors for which a fault propagates to the output are generated. The set of these input vectors is referred to as vulnerable input vectors (VIV). The set of input vectors for which a fault occurring inside the circuit nodes will not propagate to the output is referred to as invulnerable input vectors (IIV).

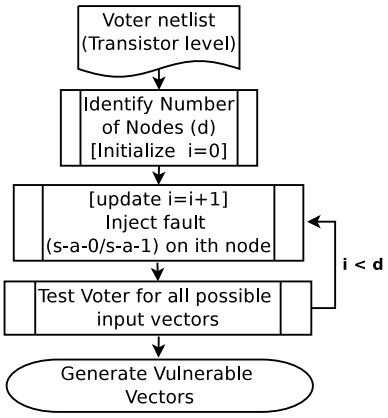

Figure 5. Flow Chart for acquiring vulnerable vectors.

For a comparative analysis, the following voters are considered: (a) Classical (b) Kshrisagar [1] (c) Bala [8] (d) Ban [18] (e) Proposed Voter (f) Classical_CMOS, and (g) Bala_CMOS. A Classical voter has a multistage architecture and is the most conventional voter design implementation using three two-input AND gates and one three-input OR gate , as shown in Figure 4a. The CMOS implementation of a classical voter using complex logic gates leads to a smaller number of transistors in the design, as presented in Figure 4f. The CMOS version of Classical voter is implemented and studied by references [2,22]. The Kshirsagar voter is a fault-tolerant design with 36 transistors based on a priority encoder and multiplexer, as illustrated in Figure 4b. The Kshirsagar voter uses transmission gates. The Ban voter shown in Figure 4d is a simplification of a Kshirsagar voter through the exclusion of a priority encoder and a reduction of the XOR logic gates to a single gate. It uses a total 18 transistors. The Bala voter, shown in Figure 4c, involves a 2-input OR gate and a complex gate to achieve a more robust design than the Classical, Ban, and Kshirsagar voters. Figure 4g shows the CMOS implementation of a Bala voter using single complex logic [2].

The voters are tested for stuck-at-faults and metrics such as Fault Masking Ratio (FMR) and Vulnerable Input Vectors (VIV). FMR quantifies the intrinsic fault tolerance of a logic circuit. As discussed earlier, some of the internal faults do not propagate to the output owing to the masking capability of the voter circuit. FMR is defined as the ratio of total number of correct voter output states in the presence of internal faults, which are masked, divided by the total number of potential internal fault occurrences [5,8].

$$FMR = \frac{k}{2^{n+m} - 2^n} \tag{14}$$

where n, m, and k are the primary inputs, internal nodes, and internal faulty combinations for which a fault is masked at the output, respectively. Here, 2^n represents the non-faulty combinations of nodes, whereas 2^{n+m} specifies the total number of faulty and non-faulty combinations [5].

To investigate the electrical properties of voter circuits, the designs were mapped using a 45 nm library [23] in Cadence Virtuoso. All the designs were simulated under the same conditions. The following parameters were used for the purpose of simulation: W = 90 nm, L = 50 nm, and Voltage = 1 V. The designs were examined in terms of the number of transistors, delay, power, and power-delay-product (PDP). Please note that all the designs were tested using all possible test vectors to determine the worst-case delay.

4.2. Analysis of Simulation Results

Table 2 shows the fault making ability of the voters on basis of the FMR and VIV. A high FMR and minimum length of VIV is desired. High FMR values of 0.720, 0.645, and 0.625 are reflected by the Kshirsagar [1], proposed, and Ban [18] voters. For s-a-0 and s-a-1, the proposed, Classical_CMOS, and Bala_CMOS voters are vulnerable under fewer input vectors. In the case of s-a-0, out of eight possible input vectors, the proposed, Classical_CMOS, and Bala_CMOS voters have 3, 4, and 5 vulnerable input vectors, respectively. In the case of s-a-1, out of eight possible input vectors, the proposed, Classical_CMOS, and Bala_CMOS voters have 3, 4, and 4 vulnerable input vectors, respectively. It can be observed that the proposed design has the maximum number of invulnerable vectors for both stuck-at-faults. This is a very important aspect because it ensures that a stuck-at-fault will not propagate to the output for five out of the eight vectors, making the proposed voter highly reliable. Here, it can be noticed that FMR fails to highlight a circuit's capability of fully masking an input vector from a fault. The capability of fully masking an input vector reflects the guarantee of a circuit that, for the given input vector, the output will always be fault free. Hence, we propose a new

metric, the QoC, based on the VIV. The QoC quantifies the aptitude of a circuit for fully masking an input vector, and can be given as follows:

$$QoC = 1 - \frac{VIV_T}{2^n} \tag{15}$$

where VIV_T is the total number of vectors in the VIV, and n is the number of circuit inputs.

Table 2. Internal Fault-Tolerance Capabilities of the Voters.

Design	Total Nodes	FMR	Vulnerable Input Vectors				QoC	
			Stuck-at-0		Stuck-at-1		Stuck-at-0	Stuck-at-1
Classical	12	0.427	$[0--, 1-0, 101]$	7/8	$[0---]$	8/8	0.125	0
Kshirsagar [1]	17	0.720	$[---]$	8/8	$[---]$	8/8	0	0
Bala [8]	9	0.472	$[00-, 10-, 010]$	5/8	$[11-, 0-1, 101]$	5/8	0.375	0.375
Ban [18]	8	0.625	$[-10, -01, 011, 100]$	6/8	$[-00, 11-, 011, 001]$	6/8	0.25	0.25
Proposed Voter	6	0.645	$[001, 110, 111]$	3/8	$[011, 100, 101]$	3/8	0.625	0.625
Classical_CMOS	6	0.354	$[-00, 001, 010]$	4/8	$[11-, 101, 011]$	4/8	0.5	0.5
Bala_CMOS	7	0.410	$[00-, 10-, 010]$	5/8	$[11-, 011, 101]$	4/8	0.375	0.5

A fault-tolerant circuit design should target a high FMR and high QoC. Please note that either s-a-0 or s-a-1 can occur for a circuit at any given time. Hence, the QoC can be given as the minimum QoC for s-a-0 and s-a-1. The QoC of the different voter circuits is presented in Table 2. The Kshirsagar voter architecture shows a good FMR. However, it is unable to establish a high QoC. The proposed voter produces the highest QoC of 0.625, followed by Classical_CMOS and Bala_CMOS, which present a good offset between the FMR and QoC.

Table 3 compares all voters in terms of the electrical features. The proposed design, with 18 transistors, outperforms all other designs in terms of the delay, power, and power-delay-product (PDP). There are four quad structures present in the design where each quad structure has an effective resistance equal to that of a single transistor [19]. The proposed design basically involves six effective resistances which is minimum among all existing works and enables the design to have the least delay compared to all the other voters. Since lesser number of transistors are used and pass transistors need lower switching energy to charge up a node because of the reduced voltage swing, the proposed design has the lowest power consumption. It should be noted that the Classical_CMOS, Bala_CMOS, Ban, and proposed voters have the least numbers of transistors, ranging from 14 to 18. However, 12 transistors exclusively serve for the provisioning of quadded redundancy for the proposed voter. The Classical voter shows the highest PDP, whereas the proposed voter has the lowest PDP.

Table 3. Design Metrics.

Design	Number of Transistors	Delay (ps)	Power (nW)	PDP (10^3)
Classical	24	30.92	3233	99.96
Kshirsagar [1]	36	3.20	4395	14.09
Bala [8]	20	15.90	1533	24.37
Ban [18]	18	3.16	1404	4.44
Proposed Voter	18	1.85	427	0.79
Classical_CMOS	14	13.80	1267	17.48
Bala_CMOS	16	13.05	1179	15.39

Figure 6 shows the product of the power, delay, and area (PDAP) of the evaluated circuits. It also shows the relation between the number of circuit nodes and invulnerable input vectors. Note that the IIV, here, of each design is an intersection of the IIV for stuck-at-0 and IIV for stuck-at-1. The Kshirsagar voter [1] has the highest number of nodes, invulnerable input vectors do not exist, and the PDAP is

extremely high. However, the proposed design has two invulnerable input vectors, minimum nodes, and a low PDAP.

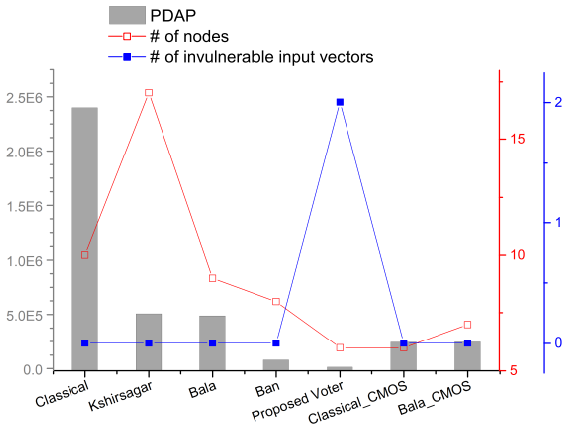

Figure 6. Relationship between nodes, invulnerable vectors, and PDAP.

4.3. Reliability Calculations

In this section the the reliability of the voters is analyzed, when a repair method is absent. Assume that the probability of the fault being masked is p. It relies on a ratio based on the number of simulations for which the fault propagates to the output and the total number of simulation iterations performed. It can be calculated using the simulation setup explained in Section 4.1. Please note that exhaustively generated input vectors corresponding to a diverse sequencing of primary input patterns were applied to the voters for estimation of p.

$(1-p)$ represents the probability that the voter is unsuccessful in masking the fault. Consider a failure rate λ_1, then the probability for successful fault masking of voter is given as $\lambda_1 p$. Hence, the probability that the voter is affected and does not mask the fault can be represented by $(1-p)\lambda_1$.

The state transition diagram illustrated in Figure 7 is used to derive reliability of the voting circuit. The operational states of voters are given as : State-1 and state-2. State-2 represents the state where the voter experiences a fault but masks it. State-3 presents for the system failure. The transition rate from state-2 to state-3 is represented by λ_2. The reliability of the voter in the state transition diagram is then computed assuming $(\lambda_1 = \lambda_2)$ and is given by [24]:

$$R_V(t) = (1 + p\lambda t)e^{-\lambda t} \tag{16}$$

λ represents the failure rate of single node of the voter. In order to cover for all the nodes present in the circuit, $d\lambda$ is considered for the calculation of (16) where d is the total number of nodes in the circuit.

$$R_V(t) = (1 + pd\lambda t)e^{-d\lambda t} \tag{17}$$

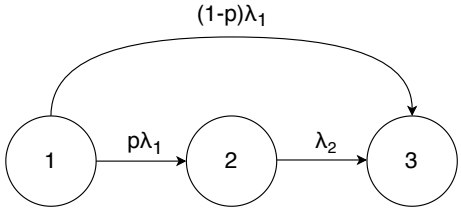

Figure 7. State transition diagram for reliability analysis.

The reliability curves for voters against normalized time (λt) are presented in Figure 8. In comparison with existing works [1,8,18], proposed voter is of most use for $\lambda t > 0.02$. It can be seen that the proposed voter is able to achieve upto 26.6% improvement in reliability for $\lambda t > 0.04$. The proposed voter shows improved reliability as compared with previous works, owing to its high FMR and better QoC.

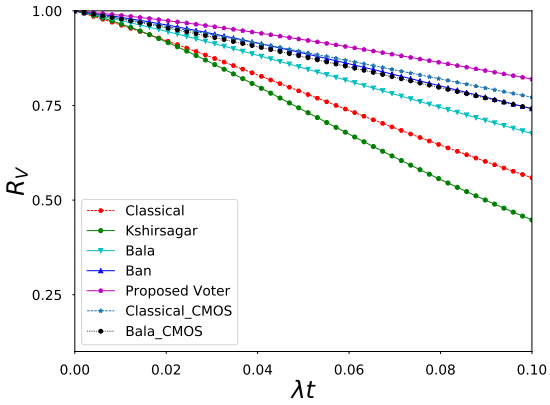

Figure 8. Reliability curves for voters.

5. Conclusions

ATMR is a promising candidate to overcome the area overhead issue of TMR. For TMR and ATMR, the final output is produced by the voter. In case of TMR, all three modules are a copy of the original circuit and their output act as the voter input, a faulty input to the voter is masked by remaining two inputs. However, in an ATMR system, a faulty input at the voter will not always be masked as the three modules are not the exact copy of original circuit and the inputs to the voters may intrinsically differ from each other due to the approximations. In this paper, we investigated the significance of a voter for ATMR. The work focused on fault tolerance at voter inputs and also, aimed for such voter design that minimum internal faults can propagate to output. We proposed a novel fault tolerant voter with superior electrical features designed using pass transistors and quadded transistor redundancy. The use of pass transistors aided in designing the voter with reduced number of transistors which led to minimum internal faults propagating to output. Since the number of transistors was less, we conveniently embedded quadded transistor redundancy to mask faults at voter inputs. These design criteria especially target ATMR and the proposed voter is specialized design which is meant for ATMR system. Hence, the work proposed a novel fault tolerant voter for ATMR with superior electrical and masking features. The merit of proposed design is illustrated through better QoC, a new proposed metric. A higher QoC ensure that greater number of input vectors are fully masked against internal faults. Finally, we show that the proposed voter has higher reliability than existing works. The proposed design can be effectively used for TMR too because of its better electrical and fault tolerant characteristics. Please note that a fault tolerant TMR voter is not effective for ATMR.

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