A 30–40 GHz CMOS Receiver Front-End with 5.9 dB NF and 16.5 dB Conversion Gain for Broadband Spectrum Sensing Applications

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Abstract: A broadband receiver front-end with low noise figure and flat conversion gain response is presented in this paper. The receiver front-end is a part of the broadband spectrum sensing receiver and processes 30–40 GHz of broad input spectrum followed by down-conversion to DC-10 GHz IF signal. The proposed work is comprised of a low noise amplifier (LNA), on-chip passive Balun, down conversion mixer, and output buffer. To achieve front-end target specification over 10 GHz input bandwidth, the stagger-tuned LNA is employed and the down conversion mixer is loaded with a 3rd-order LC ladder low pass filter. The prototype chip was implemented in 45 nm CMOS technology. The chip achieves 10.3–16.5 dB conversion gain, 5.9 dB integrated NF, and −11 dBm IIP3 from 30 to 40 GHz. The chip is realized within 0.42 mm² and consumes 96 mW from a 1.2 V supply.

Keywords: Chebyshev; current-reuse; Ka-band; ladder filter; push–pull; receiver; spectrum-sensing; stagger-tuned

1. Introduction

Modern wireless transceivers operate in a spectrum-crowded environment due to numerous communication standards introduced to meet the different needs of end-users. The opportunistic utilization of the available spectrum is proposed to maximize the bandwidth usage and achieve a high data rate [1,2]. Then, a broadband receiver solution for spectrum sensing applications is essential to achieve the opportunistic utilization of the valuable resource, also known as cognitive radio. The work in [3] proposed a frequency channelization receiver architecture as one of the attractive solutions to achieve an expeditious spectrum utilization. The channelization receiver system adopts both parallel and series channelization, which help relax the RF front-end requirements and achieve fast frequency spectrum analysis with high dynamic range. The channelization receiver requires a separate RF front-end solution. The broadband input signal branches into parallel RF front-ends with equal bandwidth. The receiver front-end presented in this paper is able to accommodate one of the parallel front-end signal paths, which translates a 30–40 GHz (Ka-band) RF input signal to DC-10 GHz IF signals while maintaining a good signal-to-noise ratio. The critical specification of the proposed receiver front-end is the 10 GHz bandwidth in both the RF and IF frequency range, which is hard to achieve at the same time. Thus, various techniques
to improve the operating bandwidth of each block are applied to the proposed receiver design. At the same time, the front-end has to provide low noise and high linearity requirements to have a wide dynamic range [3]. These requirements are satisfied with a newly proposed input matching network utilizing gate to drain feedback capacitance and a linear down-conversion mixer with current-reuse.

The wireless receiver operating at the Ka-band frequency can be utilized in many applications. First of all, to support the high data rate needed in fifth generation (5G) communication, unused millimeter-wave (mm-wave) frequency range including Ka-band has become a very attractive candidate. The 5G transceiver operating at Ka-band was studied in many previous works as a result [4–7]. Another application of the Ka-band frequency range is ultra wideband (UWB) automotive radar system. To achieve a resolution of a few centimeters, Ka-band is utilized in the receiver front-end of UWB short-range radar applications [8,9]. Satellite communication systems is another example of utilizing the Ka-band frequency range while providing a smaller form-factor at the system level [10,11].

This paper is an extended version of the work presented in [12]. The detailed optimization methods to achieve broadband operation are presented. Unpublished evidence of the validity of the proposed receiver front-end at Ka-band frequency is provided in this work. The low noise amplifier (LNA) input matching condition for stable operation is given. The mixer bandwidth extension due to the peaking inductor is analyzed based on the analog filter theory and compared with one without the peaking inductor.

The organization of the paper is as follows. The system architecture is explained in Section 2. Section 3 describes the structure and design considerations of major building blocks to meet the broadband and high performance requirements. Measurement results are presented in Section 4, and concluding remarks are provided in Section 5.

2. Overall RF Front-End System

Figure 1 shows the system architecture of the proposed receiver front-end. The proposed work is targeting a 30–40 GHz frequency range broadband input signal with single-ended configuration. The two-stage stagger-tuned low noise amplifier (LNA) provides signal amplification while providing broadband operation bandwidth. The second stage of LNA is loaded with an on-chip transformer, which performs single-to-differential signal conversion. Balun operation in this work is essential not only for its robustness to common-mode noise and interference but also for its good receiver stability. A 30–40 GHz RF signal is then down-converted to a DC-10 GHz IF frequency band by an active push–pull type mixer loaded by 3rd-order LC ladder filter. An IF signal is delivered to an off-chip 50 Ω load through the common-source configured output buffer.

![Figure 1. Receiver front-end architecture: stagger-tuned two-stage low noise amplifier (LNA), down-conversion mixer loaded with 3-stage LC ladder filter, LO buffer, and output buffer.](image-url)
3. Building Blocks Designs

3.1. Low Noise Amplifier (LNA)

Figure 2 shows the schematic of the two-stage LNA for the proposed receiver front-end. The first stage of the LNA is a common-source amplifier stage with inductive peaking load. In contrast to the conventional inductor degenerated LNA [13,14], the common-source amplifier with parasitic coupling capacitance ($C_{gd}$) is employed to achieve the input matching without sacrificing noise performance due to a degenerated inductor at the source.

![Figure 2. Schema of the LNA.](image)

The schema of the LNA’s first stage, calculating the input matching condition, is provided in Figure 3. $C_D$ denotes the combination of interconnected line parasitic, ac-coupling and second-stage gate-source capacitances. The real part of input impedance ($Re(Z_{in})$) seen at the gate of trans-conductance ($g_{m1}$) stage is derived here to show the input matching condition. The effect of $C_{gs}$ is neglected since they merely functions as a shunt components in parallel with the derived $Re(Z_{in})$ expressed as

$$Re(Z_{in}) = \frac{(C_D + C_{gd})(g_{m1}R_{D}^2 + R_D) - (R_D C_D + g_{m1}L_D)}{A},$$

where $A = (R_D C_D + g_{m1}L_D)^2\omega^2 + (g_{m1}R_D - L_D C_D \omega^2 + 1)^2$. As shown in Equation (1), with the help of the reactive load of the LNA ($L_{PD}, C_{PD}$) and $C_{gd}$, $Z_{in}$ exhibits the real impedance suitable for input matching. To achieve 50 $\Omega$ input matching and avoid potential instability, $Re(Z_{in})$ should have a positive value. $A$ always has a positive sign, so the numerator of $Re(Z_{in})$ determines the stability. The numerator of $Re(Z_{in})$ has a positive value, regardless of frequencies, when $D = (C_D + C_{gd})(g_{m1}R_{D}^2 + R_D) - (R_D C_D + g_{m1}L_D)$ is larger than 0. Through some calculations, it can be proven that the proposed LNA exhibits positive real impedance if $R_D > \sqrt{L_D/C_D}$.

Figure 4 shows the stable and unstable region in terms of the value of $R_D$. Table 1 provides the values of real design parameters. To achieve the stable condition, $R_D$ should be higher than around 33 $\Omega$. Based on these derivations of $Re(Z_{in})$, $R_D$ was selected to 44 $\Omega$ in our design. The input inductor, $L_M$, cancels the reactive part of $Z_{in}$ and thus achieves broadband input matching over 10 GHz of RF bandwidth. The second-stage provides additional gain of LNA with a 2:1 turn ratio passive Balun as a stagger-tuned load [15]. Note that the receiver front-end needs to cover a 30–40 GHz input bandwidth and the first-stage LNA load works as the low-Q band-pass filter centered at 25 GHz. Then, the stagger-tuned load in the second stage helps to compensate the gain at high-frequency regimes with a 40 GHz resonance.
frequency. The combinational effect due to two-stage stagger-tuned implementation gives the center frequency located at 38 GHz.

Table 1. LNA design parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{m1}$</td>
<td>76.2 mS</td>
<td>transconductance of $M_1$</td>
</tr>
<tr>
<td>$L_D$</td>
<td>230 pH</td>
<td>load inductor</td>
</tr>
<tr>
<td>$R_D$</td>
<td>44 Ω</td>
<td>load resistor</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>20 fF</td>
<td>parasitic capacitance between gate and drain</td>
</tr>
<tr>
<td>$C_D$</td>
<td>200 fF</td>
<td>parasitic gate capacitance of $M_2$</td>
</tr>
</tbody>
</table>

Figure 3. Schema of the LNA’s first stage.

Figure 4. The condition of $R_D$ for LNA input matching and stability.

The simulation result shows that the entire LNA exhibits a 28–45 GHz wide bandwidth, as depicted in Figure 5.
3.2. Down-Conversion Mixer

Figure 6 shows the down-conversion mixer in push–pull configuration. The conversion gain of the mixer can be expressed as
\[ A_V = \frac{2}{\pi} (g_{mp} + g_{mn}) R_L, \]
where \( g_{mp} \) and \( g_{mn} \) denote the trans-conductance due to NMOS and PMOS \( g_m \) stage of the mixer, and \( R_L \) is the load impedance. The complementary \( g_m \)-stage input doubles the conversion gain with the given bias current. It also improves the noise and linearity performances. The mixer in the proposed receiver front-end needs to down-convert a 30–40 GHz input signal to a DC-10 GHz IF signal, which gives a strict trade-off between conversion gain and the bandwidth. We employed the peaking inductor at the load as part of the C-L-C LC ladder filter, whose detailed analysis is given in the next section. The down-conversion mixer interfaced with differential outputs of Balun is the double-balanced structure. We employed the double-balanced structure here even though the push–pull configuration is immune to LO-feedthrough effects [16]. Instead, a double-balanced structure is chosen to avoid parasitic oscillation with the single-balanced mixer configuration.

Figure 6. Schema of the double-balanced mixer.

Figure 7 shows a schema of the single-balanced mixer with parasitic inductance at gate and the capacitance in the switching stages of the mixer due to the parasitic routing effects. As shown in Figure 7
(right), the impedance seen at the source of the switching stage can have a negative real part due to the parasitic inductance at gate and the parasitic capacitance, \( C_{gs} \), of the switching stage. This negative resistance causes the undesired oscillation in the single-balanced mixer. On the other hand, because LOP and LON nodes are virtual grounds in the double-balanced structure (Figure 6), the structure is robust to parasitic oscillation.

![Single-balanced mixer schema](image)

**Figure 7.** Schema of single-balanced mixer.

### 3.3. Third-Order LC Ladder Filter and LO Buffer

In mixer design, the trade-off between conversion gain and bandwidth is significant because the mixer operates in a broad bandwidth. To alleviate the gain drop at high frequency, an additional inductor is put between the mixer load and output buffer. With the introduced peaking inductor \((L_P)\), we can model the interface between the mixer load and the output buffer as a C-L-C ladder filter with single termination at the source. Figure 8 shows the single-ended representation of the interface network. \( R_L \) is the output resistance of the mixer, \( C_{INT} \) denotes the interconnection lines’ parasitic capacitance parallel with the parasitic capacitance of the mixer switching stage, and \( C_{BUF} \) denotes the input capacitance of the output buffer. The transfer functions of conversion gain without and with inductor, \( L_P \), are presented as follows

\[
A_v(s) = \frac{2/\pi(g_{mp} + g_{mn})R_L}{1 + sR_L(C_{INT} + C_{BUF})},
\]

\[
A_{v,3rd}(s) = \frac{2/\pi(g_{mp} + g_{mn})R_L}{1 + sR_L(C_{INT} + C_{BUF}) + s^2L_PC_{BUF} + s^3L_PC_{BUF}C_{INT}R_L}.
\]

By adding \( L_P \), the conversion gain has a third-order response, and we synthesized the pole location following the Chebyshev filter realization to maximize the bandwidth [17]. The condition for a third-order Chebyshev filter dictates the following design parameter. The third-order Chebyshev filter with a 2 dB ripple was chosen with normalized pole locations at \( S_{1,2}^N = -(0.185 \pm j0.923) \) and \( S_3^N = -0.369 \). With \( R_L = 86 \) \( \Omega \), \( C_{INT} = 136 \) fF and \( C_{BUF} = 234 \) fF for the given bias in the LC ladder network, \( L_P \) was chosen to the value of 1 nH, which gives the desired filter transfer function.
The effect of the bandwidth extension with third-order LC ladder filter is clearly seen in Figure 9. At the band-edge (10 GHz IF frequency), the conversion gain is improved by 5.26 dB by employing the inductor peaking load as part of the ladder filter. The required LO signal of 30 GHz in the proposed receiver front-end is injected from the off-chip source. To ensure maximum signal reception at such a high frequency, we employed the reactive matching network to match 50 Ω reference impedance. The matching network is implemented with a parallel capacitor and series inductor.

Figure 9. Simulated conversion gain of the down-conversion mixer with and without series peaking inductor $L_p$.

Figure 10 shows the value of the matching components as well as the trajectory from the gate of the LO buffer to the 50 Ω. The series inductor is realized with serpentine line inductance from the pad to the active circuit. This line inductance is clearly noticeable from the chip photograph shown in Figure 11. The LO buffer is realized with two-stage inverter-type amplifiers, where the first stage is AC coupled to the off-chip source, and the second stage is DC coupled to maximize the $f_t$. 
Figure 10. Schema of the two-stage LO buffer with reactive matching and a Smith chart with the trajectory from Z\textsubscript{BUF} to the 50 Ω.

Figure 11. Chip photograph of the proposed receiver front-end.
4. Measurement Results

The proposed receiver front-end was designed in TSMC 45 nm CMOS technology. The proposed receiver front-end was simulated with SpectreRF from Cadence and the electromagnetic effects of critical interconnect lines were considered by Advanced Design System (ADS). The fabricated chip was encapsulated in a quad flat no leads (QFN) package for connecting dc pads and IF output. The RF and LO signals were applied using on-wafer probing to reduce the losses and mismatches. Keysight N5234A as used for S-parameter measurement and Keysight N9010A-544 was used for spectrum analysis and noise figure measurement. The chip photograph of the implemented receiver front-end is shown in Figure 11. The total area of the chip is 0.42 mm$^2$, and the core circuits occupies 0.21 mm$^2$. The entire circuit consumes 96 mW with 1.2 V power supply. Figure 12a shows the input reflection coefficient (S$_{11}$). The target level was chosen as $-10$ dB for stable power transfer. There was a little frequency shift in S$_{11}$ due to the un-accounted parasitics in the interconnect line, but the broad impedance matching performance with S$_{11} < -9$ dB was achieved within the 30–40 GHz frequency range. Figure 12b shows the conversion gain and double-sideband NF over the 10 GHz IF frequency range of the implemented receiver front-end. The measured conversion gain was 10.3–16.5 dB. We measured a maximum conversion gain of 16.5 dB at 50 MHz IF frequency. Measured NF integrated over a 10 GHz IF bandwidth was 5.9 dB, whereas the simulated NF over the same integration bandwidth was 5 dB. Linearity performance is shown in Figure 12c. The measured IIP3 was around $-11$ dBm, based on the two tone input injection tones at 35 GHz and 35.1 GHz. A large signal linearity performance was measured with a 1 dB compression point as shown in Figure 12d. The implemented receiver front-end showed $-19$ dBm of 1 dB compression point (P$_{1dB}$). Measured P$_{1dB}$ and IIP3 showed an 8 dB difference, close to the theoretical discrepancy between the two [18]. Table 2 summarizes the performances and compares the performances with other recent works. It is clear that the proposed front-end exhibits the largest RF and IF bandwidth while having a small die area, moderate power consumption, and comparable performance to previous studies. Therefore, it is proven that the proposed front-end is suitable for the various Ka-band applications as well as channelization receiver systems.

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<tbody>
<tr>
<td>RF Frequency [GHz]</td>
<td>30–40</td>
<td>20–30</td>
<td>18.2–21.4</td>
<td>28–32</td>
<td>33.6–36.3</td>
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<tr>
<td>IF Bandwidth [GHz]</td>
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<td>0.3</td>
<td>1.35</td>
<td>4</td>
<td>2.3</td>
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<tr>
<td>Gain$_{\text{max}}$ [dB]</td>
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<td>18.7</td>
<td>49</td>
<td>10.5</td>
<td>30.9</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>5.9$^1$</td>
<td>7.1–14.2</td>
<td>5.25–6.25</td>
<td>5.6–8.6</td>
<td>5.9–7.5</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>$-11$</td>
<td>$&gt;-7.6$</td>
<td>$&gt;-33.5^2$</td>
<td>$&gt;-10.6$</td>
<td>N/A</td>
</tr>
<tr>
<td>P$_{1dB}$ [dBm]</td>
<td>$-19$</td>
<td>$&gt;-17.9$</td>
<td>$&gt;-43.3^3$</td>
<td>$&gt;-16.8$</td>
<td>$-23$</td>
</tr>
<tr>
<td>P$_{\text{consumption}}$ [mW]</td>
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<td>5.2</td>
<td>80</td>
<td>136.5</td>
<td>135/27.6$^4$</td>
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<tr>
<td>Technology</td>
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<td>CMOS 180 nm</td>
<td>SiGe 180 nm</td>
<td>SiGe 130 nm</td>
<td>CMOS 65 nm</td>
</tr>
<tr>
<td>Area [mm$^2$]</td>
<td>0.42/0.21 $^5$</td>
<td>0.18</td>
<td>0.4/0.24 $^5$</td>
<td>1.08</td>
<td>2.16 $^6$</td>
</tr>
</tbody>
</table>

$^1$ Integrated NF (DC–10 GHz), $^2$ Calculated from OIP3, $^3$ Calculated from OP$_{1dB}$, $^4$ Receiver only, $^5$ Active area, $^6$ Including transmitter.
Figure 12. Measured (a) input reflection coefficient ($S_{11}$), (b) conversion gain and NF over a 10 GHz IF frequency range; (c) IIP3 with $f_{rf1}=35$ GHz and $f_{rf2}=35.1$ GHz; and (d) 1 dB compression point with $f_{rf}=35$ GHz.

5. Conclusions

The 30–40 GHz receiver front-end for broadband sensing receivers is implemented. The two-stage stagger-tuned LNA and push–pull type mixer loaded with third-order LC ladder filter are employed to achieve the broadband operation with low current consumption. To ensure unconditional stability of the receiver front-end with single-ended input signal, a double-balanced mixer operation is employed with on-chip Balun. This chip achieves a maximum conversion gain of 16.5 dB, 5.9 dB integrated NF, and $-11$ dBm IIP3 from 30 GHz to 40 GHz. The power consumption is 96 mW from a 1.2 V supply. The active area is only $0.21$ mm$^2$. The proposed receiver front-end shows the widest RF and IF operating bandwidth with good performance and moderate power consumption compared to previous works.


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References
