A 6-Bit Ku Band Digital Step Attenuator with Low Phase Variation in 0.13-µm SiGe BiCMOS

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Abstract: A 6-bit Ku band digital step attenuator with low phase variation is presented in this paper. The attenuator is designed with 0.13-µm SiGe BiCMOS process technology using triple well isolation N-Metal-Oxide-Semiconductor (TWNMOS) and through-silicon-via (TSV). TWNMOS is mainly used to improve the performance of switches and reduce the insertion loss (IL). TSV is utilized to provide approximately ideal global current ground plane with low impedance for the attenuator. In addition, substrate floating technique and new capacitance compensation technique are adopted in the attenuator to improve the linearity and decrease the phase variation. The measured results show that the attenuator IL is 6.99–9.33 dB; the maximum relative attenuation is 31.87–30.31 dB with 0.5-dB step (64 states), the root mean square (RMS) for the amplitude error is 0.58–0.36 dB and the phase error RMS is 2.06–3.46° in the 12–17 GHz frequency range. The total chip area is 1 × 0.9 mm².

Keywords: digital step attenuator; low phase variation; triple well isolation NMOS; wideband; CMOS integrated circuits

1. Introduction

The attenuator is one of the key components of modern communications. It is widely used in the transmitter/receiver (T/R) module of phased array radar system [1,2], and its main function is to achieve amplitude control. Compared with the X-type attenuator [3] and variable gain amplifier (VGA) [4,5], the passive digital step attenuator has the advantages of low power consumption, high linearity, wide frequency band and low temperature drift. Therefore, the design of attenuator with high resolution, large attenuation, low IL and low phase variation has great value, and very broad application prospects.

A variety of passive attenuator circuits have been designed in [6–24]. There are three most-used topologies in the passive attenuators: Switched path attenuators [6–9], distributed attenuators [10,11] and switched T/Pi attenuators [12–24]. Switched path attenuators topology use single-pole-double-throw (SPDT) switches to control the signal between reference thru line path and the resistive attenuation network path. This topology exhibits low phase variation, but has high insertion loss and large chip area, so it is not suitable for multi-bit CMOS digital step attenuator. Transistors as varistors and the half/quarter-wavelength of the transmission lines (TLs) together constitute the distributed attenuators topology. Due to the relative attenuation signal paths across the transmission lines have no series switches, this topology has the advantage of low IL. Meanwhile, the use of the TLs greatly increases the chip area. Switched T/Pi attenuators topology is composed by the resistor attenuation network and series shunt single-pole-single-throw (SPST) switches. Its chip area is very compact and suitable for multi-bit integration.
In order to meet the design requirements of phased array system for attenuators with high resolution, large attenuation, low IL and low phase change, this paper proposed a 6-bit CMOS digital step attenuator using switched T/Pi topology. The switches are designed and optimized by TWNMOS and through-silicon-via (TSV), in order to improve the performance and reduce the IL of the switches. Moreover, the attenuator adopted substrate floating and new capacitance compensation technology, which improved linearity and reduced the phase variation.

2. Proposed Circuit Design and Analysis

The switch is one of the key building blocks in the digital step attenuator [25,26]. In this paper, the triple well isolation NMOS is adopted in the switch shown in Figure 1a. Figure 1b,c illustrate the simplified equivalent circuits for on-state and off-state of the switch. As shown in Figure 1, the on-resistance $R_{on}$ and parasitic resistance at source and drain terminals of NMOS switch will contribute to the insertion loss in the signal path. The parasitic capacitors $C_{GS}$, $C_{GD}$, $C_{SB}$ and $C_{DB}$ will contribute to the off-capacitance $C_{off}$ of NMOS switch and act as a leak path from input to output at the off-state. A large resistor $R_{G}$ ($10 \ \text{k}\Omega$) is used to prevent the RF signal from leaking through the bias line. Body floating technique is used to improve power handling of the switch by reducing the signal loss through source/drain-to-body junctions. To implement this technique, a large resistor $R_{B}$ ($10 \ \text{k}\Omega$) is added to the body terminal of the switch to enhance the linearity and insertion loss performance. Meanwhile, TSV is utilized to provide approximately ideal global current ground plane with low impedance for the attenuator.

![Figure 1](image)

(a) NMOS switch  (b) on-state  (c) off-state

Figure 1. (a) The NMOS switch in the proposed attenuator; (b) The on-state simplified equivalent circuits of the switch; (c) The off-state simplified equivalent circuits of the switch.

Inductive and capacitive correction structure digital step attenuator is adopted in [18] to achieve low phase variations. Although the inductance correction structure can achieve low IL, it occupies a large chip area. Capacitance correction structure has the advantages of lower phase variation and better agreement with simulation results in the broadband frequency range, but it has larger IL than inductance correction structure. In order to solve the contradiction between large IL and low phase variation of capacitance correction structure, especially large attenuation units, such as 8 dB and 16 dB attenuation cells. A new capacitance compensation technique is proposed in this paper. The topology of the proposed capacitance compensation correction network attenuation cell circuits in the digital step attenuator is shown in Figure 2.
The signal passes through the series path, as shown in Figure 2b. When the switch $M_1$ is on, and $M_2$ is off, the attenuator works in the reference state. Therefore, the correction network will affect the performance of the attenuation state; the equation of transmission phase error can be deduced as follows (see Appendix A for detailed derivation):

$$\theta = \tan^{-1} \left( \frac{-C_P R_p^2 (Z_0 + R_s)}{(R_p + R_{on})(2R_p + 2R_{on} + Z_0 + R_s)/\omega + 2R_p^3 C_P^2 \omega + R_p^2 C_P (Z_0 + R_s)} \right),$$  

(1) 

where $\omega$ is the operating angular frequency, $Z_0$ is the characteristic impedance. For simplicity, all parameters in the equation are treated as the constant except the operating angular frequency $\omega$.

The theoretical mathematical analysis image of function $\theta$ can be drawn using MATLAB in Figure 3a. The slope of $\theta$ changes from negative to positive value at the broadband angular frequency range. When the slope is zero, there exists a critical frequency $f$ ($f = \omega/2\pi$), which can be used to correct the transmission phase error.

Figure 3b shows the practical simulation results in 0.13 $\mu$m SiGe BiCMOS process of the transmission phase of the phase correction branch in Figure 2d. The transmission phase varies with parallel $C_P$ value (swept from 60 fF to 180 fF) at the broadband frequency range. Figure 3a,b possess a similar variation tendency, which verifies the theoretical analysis results in Equation (1).

Figure 4a shows the proposed T-type attenuator topology transmission phases of reference and attenuation states are simulated with various parallel capacitor $C_P$ values. The phases of attenuation states have the same variation trend as those of the phase correction branch in Figure 3b.
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circuit structure, Flatness of the phase
topology in 4 dB attenuation cell. The simulation phase
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T-type topology in 4 dB attenuation cell. The simu-
oration phase difference results with traditional
T-type topology in 4 dB attenuation cell. The simu-
T-type and proposed Cp T-type topology in 4 dB attenuation cell is illustrated in Figure 5b. With Cp compensation circuit structure, Flatness of the phase difference is better in a wide bandwidth range.

Figure 5. (a) The simulation attenuation results with traditional T-type and proposed Cp T-type topology in 4 dB attenuation cell; (b) the simulation phase difference results with traditional T-type and proposed Cp T-type topology in 4 dB attenuation cell.

Meanwhile, in order to study the influence of TSV on phase difference, parasitic parameters of TSV with different sizes can be obtained by the electromagnetic field (EM) simulation. Table 1 shows parasitic inductance and resistance of TSV with different sizes.

Table 1. Parasitic inductance and resistance of TSV with different sizes.

<table>
<thead>
<tr>
<th>Number of Row Vias</th>
<th>Number of Column Vias</th>
<th>Parasitic Inductance (pH)</th>
<th>Parasitic Resistance (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>33</td>
<td>37</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>28</td>
<td>26</td>
</tr>
<tr>
<td>1</td>
<td>7</td>
<td>23</td>
<td>17</td>
</tr>
<tr>
<td>1</td>
<td>12</td>
<td>17</td>
<td>9</td>
</tr>
<tr>
<td>2</td>
<td>7</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>11</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>12</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>22</td>
<td>6</td>
<td>3</td>
</tr>
</tbody>
</table>

TSV is utilized to provide approximately ideal global current ground plane with low impedance for the attenuator. Take the proposed Cp T-type topology in 4 dB attenuation cell as an example, the TSV connected to the switch body terminal mainly provides on-chip grounding of the substrate, and its effect on the phase variation of the attenuator can be neglected. The TSV connected to capacitance compensation correction branch of the attenuation cell also provides on-chip grounding. The parallel capacitor Cp grounding terminal of the capacitance compensation correction branch in attenuation cell is not ideal, which results in an additional phase variation of the attenuator circuit. Although the effect of TSV on attenuator performance is small, it cannot be ignored. The simulation phase difference results with TSV size variation in proposed Cp T-type topology in 4 dB attenuation cell is illustrated in Figure 6. In microwave and millimeter wave bands, TSV will inevitably introduce parasitic inductance and resistance. The parasitic parameters are related to their size (i.e., the number of rows and columns vias). The larger the size, the smaller the parasitic inductance and resistance, but the bigger size will occupy a large area of the layout, so a compromise should be considered. After careful consideration, the TSV size of 2 × 5 was selected in this design.
The proposed capacitance compensation correction network and switch are also applicable to the Pi and bridge-T type attenuation cells. They have the same operation principle to realize low phase difference as the proposed T-type attenuator topology.

Traditional capacitance $C_c$ and $C_p$ compensation correction networks are widely used in the digital control step attenuator circuit [18,20,21], but there are large insertion losses, especially in large 8 and 16 dB attenuation units. In order to solve this problem, a parallel capacitor $C_p$ is added to the attenuation shunt branch in 8 and 16 dB attenuation cells. Take 16 dB attenuation unit as an example: Figure 7a shows the simulation IL results with traditional $C_c$ and proposed $C_c + C_p$ compensation in 16 dB attenuation cell. The IL decreases obviously with the increase of frequency in the proposed $C_c + C_p$ compensation structure. The simulated attenuation, phase difference results with traditional $C_c$ and proposed $C_c + C_p$ compensation in 16 dB attenuation cell is illustrated in Figure 7b. With $C_c + C_p$ compensation circuit structure, the attenuation and phase difference change more smoothly in a wide frequency band.

![Figure 6](image_url)

**Figure 6.** The simulation phase difference results with TSV size variation in proposed $C_p$ T-type topology in 4 dB attenuation cell.
Through the above theoretical and simulation analysis, in the proposed 6-bit digital control step attenuator circuit, 0.5 dB, 1 dB, 2 dB and 4 dB attenuation units adopt the proposed parallel capacitor \( C_p \) compensation method, which reduces the additional phase shift of attenuation. In the large attenuation unit (8 dB, 16 dB), we combine the traditional capacitance compensation method with the proposed parallel capacitance \( C_p \) compensation method, which reduces the problems of excessive insertion loss and large phase shift fluctuation range in the traditional capacitance compensation method.

The utilized attenuation cell topology in 6-bit CMOS digital control step attenuator is shown in Figure 8. 0.5 dB, 1 dB and 2 dB attenuation cells are configured with switched bridge-T type in Figure 8a. 4 dB attenuation cell is configured with switched T-type in Figure 8b. The switched Pi-type topology in Figure 8c is suitable for large attenuation cells, such as 8 and 16 dB cells. The block diagram of the proposed 6-bit digital control step attenuator is shown in Figure 9.
The component values of each attenuator unit are summarized in Table 2. The 6-bit CMOS digital control step attenuator circuit is optimized in terms of linearity, loading effect and power processing ability. Finally, the bit ordering 0.5-4-8-2-1-16 dB sequence is adopted in this paper. The proposed attenuator is controlled by the 6-bit digital signal control circuit array, \( V_{c1}, V_{c2}, V_{c3}, V_{c4}, V_{c5}, V_{c6} \) which are used to control 0.5 dB, 1 dB, 2 dB, 4 dB, 8 dB, 16 dB attenuation modules, respectively. The layout of series/parallel resistors are the key components in the attenuator design; and the resistance values need to be carefully selected. In particular, small resistance values are realized by parallel connection of large resistance to reduce the influence of process variation effects. The power consumption of the attenuator is extremely low, which is contributed by the dynamic power consumption of inverters in each attenuation module.

![Figure 9](image-url) The block diagram of the proposed 6-bit digital control step attenuator.

The full chip electromagnetic (EM) simulation of the proposed 6-bit digital control step attenuator except resistors, capacitors and NMOS switch transistors components is realized in ADS Momentum in order to further ensure the performance. The transmission RF lines between the circuits of each attenuation cell are used to connect each module, which improves the matching performance and adjusts the transmission phase characteristics. Both input and output impedances of the proposed attenuator are matched to 50 \( \Omega \).

### Table 2. Component values of each proposed attenuator unit.

<table>
<thead>
<tr>
<th>Attenu. (dB)</th>
<th>Topology</th>
<th>( R_s (\Omega) )</th>
<th>( R_o (\Omega) )</th>
<th>( R_p (\Omega) )</th>
<th>( R_c (\Omega) )</th>
<th>( W_{1,3,5} (\mu m) )</th>
<th>( W_{2,4,6,7} (\mu m) )</th>
<th>( C_s (fF) )</th>
<th>( C_p (fF) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>Bridge-T</td>
<td>5.92</td>
<td>40.9</td>
<td>368</td>
<td>0</td>
<td>40</td>
<td>15</td>
<td>0</td>
<td>17</td>
</tr>
<tr>
<td>1</td>
<td>Bridge-T</td>
<td>15.7</td>
<td>74.1</td>
<td>1293</td>
<td>0</td>
<td>90</td>
<td>20</td>
<td>0</td>
<td>17</td>
</tr>
<tr>
<td>2</td>
<td>Bridge-T</td>
<td>20.7</td>
<td>164.6</td>
<td>873</td>
<td>0</td>
<td>80</td>
<td>20</td>
<td>0</td>
<td>83</td>
</tr>
<tr>
<td>4</td>
<td>T-type</td>
<td>15.3</td>
<td>0</td>
<td>90.5</td>
<td>0</td>
<td>80</td>
<td>15</td>
<td>0</td>
<td>50.7</td>
</tr>
<tr>
<td>8</td>
<td>Pi-type</td>
<td>0</td>
<td>0</td>
<td>91.1</td>
<td>53.7</td>
<td>60</td>
<td>15</td>
<td>84.2</td>
<td>58.1</td>
</tr>
<tr>
<td>16</td>
<td>Pi-type</td>
<td>0</td>
<td>0</td>
<td>50.1</td>
<td>70.6</td>
<td>20</td>
<td>15</td>
<td>102.5</td>
<td>152.2</td>
</tr>
</tbody>
</table>

The full chip electromagnetic (EM) simulation of the proposed 6-bit digital control step attenuator except resistors, capacitors and NMOS switch transistors components is realized in ADS Momentum in order to further ensure the performance. The transmission RF lines between the circuits of each attenuation cell are used to connect each module, which improves the matching performance and adjusts the transmission phase characteristics. Both input and output impedances of the proposed attenuator are matched to 50 \( \Omega \).

### 3. Measurement Results

The proposed 6-bit digital control step attenuator has been designed and fabricated in 0.13-\( \mu m \) SiGe BiCMOS technology. The die photograph of the proposed 6-bit digital control step attenuator is depicted in Figure 10. The total chip size is 1 \( \times \) 0.9 mm\(^2\). All the DC Pads are bond wired to a PCB for chip testing, and the chip is probed with Cascade’s 100 \( \mu m \) ground-signal-ground (GSG) probes at the input and output ports. The power consumption of the proposed attenuator is extremely low and negligible.
Figure 10. The die photograph of the proposed 6-bit digital control step attenuator.

The input return loss (RL) is >13 dB in Figure 11a and the output return loss is >14.1 dB in Figure 11b at 10–18 GHz for the 64 states. Figure 12 shows the measured insertion loss (of the reference state) is 6.99–9.33 dB and IP_{-1dB} (of the reference state) is 13.6–16.2 dBm at 12–17 GHz. The maximum attenuation relative to that of the reference state is 31.87–30.31 dB with 0.5-dB step (64 states) at 12–17 GHz in Figure 13. The measured results show that the root mean square (RMS) for the amplitude error is 0.58–0.36 dB and the RMS phase error is 2.06–3.46° in the 12–17 GHz frequency range for the 64 states in Figure 14. The RMS for the amplitude error can be defined as:

$$A_{RMS} = \sqrt{\frac{1}{N} \sum_{i=1}^{N} (A_{m,i} - A_{theo,i})^2 (dB)},$$

(2)

where $A_{RMS}$ is the attenuation RMS amplitude error, $i$ is the attenuation state index, $N$ is 64, $A_{m,i}$ is the measured attenuation relative to the reference in a given state, and $A_{theo,i}$ is the theoretical attenuation in a given state. The RMS phase error for the attenuation is calculated using the equation defined as follows:

$$\theta_{RMS} = \sqrt{\frac{1}{M} \sum_{i=1}^{M} (\theta_{m,i} - \theta_{ref,m})^2 (deg)},$$

(3)

where $\theta_{RMS}$ is the attenuation RMS phase error, $i$ is the attenuation state index, $M$ is 64, $\theta_{m,i}$ is the measured attenuation relative phase in a given state, and $\theta_{ref,m}$ is the measured attenuation relative phase in the reference state.
Figure 11. (a) The measured input return loss of the proposed attenuator; (b) the measured output return loss of the proposed attenuator.

Figure 12. The measured insertion loss and IP-1dB of the proposed attenuator.

Figure 13. (a) The measured 64-state relative attenuation of the proposed attenuator; (b) the measured 64-state relative insertion phase of the proposed attenuator.
with IP–1dB than [13,16,21]. Compared with [12,13,17], this design has wide frequency coverage. Even compared with all references in Table 3, the RMS phase error of this design has considerable competitive advantage. In this paper, the design of a 6-bit digital attenuator with low insertion loss and small RMS phase error in Ku-band (12–17 GHz) is realized by using substrate floating technology and the proposed capacitance compensation technology.

Table 3. Performance comparison of relevant digital control step attenuators.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Frequency (GHz)</th>
<th>Technology</th>
<th>Number of Bits</th>
<th>Attenuation Rang (dB)</th>
<th>Attenuation Step (dB)</th>
<th>RL (dB)</th>
<th>RMS Amplitude Error (dB)</th>
<th>RMS Phase Error (°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>19–21</td>
<td>CMOS</td>
<td>6</td>
<td>32</td>
<td>0.5</td>
<td>&gt;12</td>
<td>&gt;12</td>
<td>&gt;12</td>
</tr>
<tr>
<td>[13]</td>
<td>14–18</td>
<td>BiCMOS</td>
<td>6</td>
<td>31.5</td>
<td>0.5</td>
<td>&gt;13</td>
<td>&lt;0.26</td>
<td>1.7–7.2</td>
</tr>
<tr>
<td>[16]</td>
<td>6–12.5</td>
<td>BiCMOS</td>
<td>7</td>
<td>16.51</td>
<td>0.26</td>
<td>&lt;13</td>
<td>&lt;0.26</td>
<td>1.6–4.2</td>
</tr>
<tr>
<td>[17]</td>
<td>20–24</td>
<td>BiCMOS</td>
<td>6</td>
<td>31.5</td>
<td>0.5</td>
<td>&lt;10</td>
<td>&lt;0.43</td>
<td>&lt;4</td>
</tr>
<tr>
<td>[18]</td>
<td>DC–14</td>
<td>BiCMOS</td>
<td>6</td>
<td>31.5</td>
<td>0.5</td>
<td>&gt;10</td>
<td>&lt;0.5</td>
<td>&lt;4</td>
</tr>
<tr>
<td>[19]</td>
<td>DC–20</td>
<td>BiCMOS</td>
<td>6</td>
<td>31.5</td>
<td>0.5</td>
<td>&gt;12</td>
<td>&lt;0.37</td>
<td>&lt;4</td>
</tr>
<tr>
<td>[20]</td>
<td>12–17</td>
<td>BiCMOS</td>
<td>6</td>
<td>31.5</td>
<td>0.5</td>
<td>&gt;12</td>
<td>0.58–0.36</td>
<td>2.06–3.46</td>
</tr>
<tr>
<td>This Work</td>
<td></td>
<td>BiCMOS</td>
<td>6</td>
<td>31.5</td>
<td>0.5</td>
<td>&gt;12</td>
<td>0.37–0.36</td>
<td>2.06–3.46</td>
</tr>
</tbody>
</table>

1. excluding pads 2. including pads.

5. Conclusions

This paper has presented a 12–17 GHz 6-bit digital control step attenuator with low phase imbalance in 0.13-μm SiGe BiCMOS technology. In this design, a parallel capacitor \( C_p \) is added to the attenuation shunt branch of the traditional \( P_1 \), T, and bridge-T type attenuation cells to form a phase correction network with the parallel resistor. Furthermore, in order to study the influence of TSV on phase difference, parasitic parameters of TSV with different sizes can be obtained by an electromagnetic field (EM) simulation. After careful consideration, the TSV size of \( 2 \times 5 \) was selected in this design. As far as the author knows, this is the first 6-bit digital attenuator designed with TSV. The influence of TSV on attenuator performance is also analyzed and verified. With the help of these techniques, the transmission phase error of the attenuation state can be corrected, thus, leading to a low phase imbalance. Meanwhile, substrate floating technology is adopted to reduce switches insertion loss and
improve linearity. The proposed attenuator achieves the RMS phase error less than 3.46° and amplitude error less than 0.58 dB over 12–17 GHz. It has a maximum attenuation range of 31.87 dB with the approximate 0.5-dB step. In addition, good input/output return loss, high IP–1dB, moderate chip area and wide bandwidth are obtained, which makes it suitable to use in Ku-band phased array systems.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

For T-network configuration, ABCD-parameters relate the voltages to current in the following form for a two-port network:

\[
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} = \begin{bmatrix}
A & B \\
C & D
\end{bmatrix} \begin{bmatrix}
V_2 \\
I_2
\end{bmatrix}
\]

Which can be put in matrix form as

\[
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} = \begin{bmatrix}
A & B \\
C & D
\end{bmatrix} \begin{bmatrix}
V_2 \\
I_2
\end{bmatrix}
\]

The ABCD parameters in Equation (A3) are defined as

\[
A = \frac{V_1}{V_2} \bigg|_{I_2=0} \quad A = \frac{V_2}{I_2} \bigg|_{V_2=0}
\]

The ABCD network is useful in finding the voltage or current gain of a component or the overall gain of a network. One of the great advantages of ABCD parameters is their use in cascaded network or components. When this condition exists, the overall ABCD parameter of the network becomes the matrix product of an individual network and a component.

For T-network configuration, Parameters A and C are determined when Port2 is open circuited as

\[
A = \frac{V_1}{V_2} \bigg|_{I_2=0} \rightarrow V_2 = \frac{Z_C}{Z_C + Z_A} V_1 \rightarrow A = \left(\frac{Z_C + Z_A}{Z_C}\right),
\]

and

\[
C = \frac{I_1}{V_2} \bigg|_{I_2=0} \rightarrow I_1 = V_2 \left(\frac{1}{Z_C}\right) \rightarrow C = \left(\frac{1}{Z_C}\right).
\]
According to Equation (A9), we can get the Figure 2d ABCD parameters of the network as follows:

\[ B = \frac{V_1}{I_2} \bigg|_{v_{20}} \rightarrow I_2 = \frac{-V_1}{Z_A + (Z_B / Z_C)} \frac{Z_C}{Z_B + Z_C} \rightarrow B = \left( \frac{Z_A Z_B + Z_A Z_C + Z_B Z_C}{Z_C} \right) \]  
\[ (A7) \]

and

\[ D = \frac{-I_1}{I_2} \bigg|_{v_{20}} \rightarrow I_2 = -I_1 \left( \frac{Z_C}{Z_B + Z_C} \right) \rightarrow D = \left( \frac{Z_B + Z_C}{Z_C} \right) \]  
\[ (A8) \]

Therefore, the T-network ABCD matrix is

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix} = \begin{bmatrix}
\frac{Z_C + Z_A}{Z_C} & \frac{Z_A Z_B + Z_A Z_C + Z_B Z_C}{Z_C} \\
\frac{Z_C}{Z_C} & \frac{Z_B + Z_C}{Z_C}
\end{bmatrix} 
\]  
\[ (A9) \]

Simplified the equivalent circuit of phase correction branch, as shown in Figure 2d, the transmission phase of the network is derived from the transmission (ABCD) matrix for the attenuation state. According to Equation (A9), we can get the Figure 2d ABCD parameters of the network as follows:

\[ A = \frac{1 + j \rho \omega C_p (R_{on} + R_s) + R_p}{R_{on} (1 + j \rho \omega C_p) + R_p} \]  
\[ (A10) \]

\[ B = \frac{2R_c R_{on} + R_s^2 (1 + j \rho \omega C_p) + 2R_c R_p}{R_{on} (1 + j \rho \omega C_p) + R_p} \]  
\[ (A11) \]

\[ C = \frac{1 + j \rho \omega C_p}{R_{on} (1 + j \rho \omega C_p) + R_p} \]  
\[ (A12) \]

\[ D = \frac{(R_s + R_{on}) (1 + j \rho \omega C_p) + R_p}{R_{on} (1 + j \rho \omega C_p) + R_p} \]  
\[ (A13) \]

Assume that the matching impedance of Port 1 and Port 2 is \( Z_0 \), according to the theory of microwave network, the insertion phase \( \theta \) of the T-network can be calculated by the following equation:

\[ \theta = \tan^{-1} \frac{\text{Im}(AZ_0 + B + CZ_0^2 + DZ_0)}{\text{Re}(AZ_0 + B + CZ_0^2 + DZ_0)} \]  
\[ (A14) \]

Im and Re represent the imaginary part and the real part of the formula, respectively.

\[ \text{Im}(AZ_0 + B + CZ_0^2 + DZ_0) = \left[ 2R_c (1 + R_p^2 \omega^2 C_p^2) R_p \omega C_p Z_0 + R_s (1 + R_p^2 \omega^2 C_p^2) R_p^2 \omega C_p \right] + Z_0^2 \left( 1 + R_p^2 \omega^2 C_p^2 \right) R_p^2 \omega C_p \]  
\[ (A15) \]

Due to \( R_p^2 \omega^2 C_p^2 \ll 1 \), the formula can be simplified to (A16)

\[ \text{Im}(AZ_0 + B + CZ_0^2 + DZ_0) = - \left( 2R_c R_p \omega C_p Z_0 + R_s^2 R_p \omega C_p + Z_0^2 R_p^2 \omega C_p \right). \]  
\[ (A16) \]

\[ \text{Re}(AZ_0 + B + CZ_0^2 + DZ_0) = Z_0^2 (R_p + R_{on}) + 2Z_0 R_c (R_p + R_{on}) + R_s^2 (R_p + R_{on}) + 2Z_0 (R_p + R_{on})^2 + 2 \left( R_p \omega C_p \right)^2 (Z_0 + R_s), \]  
\[ (A17) \]
\[
\begin{align*}
\theta &= \tan^{-1} \left( \frac{-R_p^2 \omega C_p (Z_0 + R_s)}{(R_p + R_m) (Z_0 + R_s) + 2(R_p + R_m)^2 + 2(R_p^2 \omega C_p)^2 + R_p^2 \omega C_p (Z_0 + R_s)} \right), \\
\theta &= \tan^{-1} \left( \frac{-C_p R_p^2 (Z_0 + R_s)}{(R_p + R_m) (2R_p + 2R_m + Z_0 + R_s)/\omega + 2R_p^4 C_p^2 \omega + R_p^2 C_p (Z_0 + R_s)} \right).
\end{align*}
\]

The appendix gives a detailed derivation of Formula (1) in this paper.

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