

Article

A Phasor Measurement Unit Algorithm Using IIR Filters for FPGA Implementation

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Abstract: Phasor measurement units (PMU) are increasingly used in electrical power transmission networks, to maintain stability and protect the network. PMUs accurately measure voltage, phase, frequency, and rate of change of frequency (ROCOF). For reliability, it is desirable to implement a PMU using an FPGA. This paper describes a novel algorithm, suited to implementation in an FPGA and based on a simple PMU block diagram. A description of its realization using low hardware complexity infinite impulse response (IIR) filters is given. The IEC/IEEE standard 60255-118-1:2018 Part 118-1: Synchrophasor measurements for power systems, describes “reference” Finite Impulse Response (FIR) filters for implementing PMU hardware. At the 10 kHz sampling frequency used for our implementation, each “reference” FIR filter requires 100 multipliers, while an 8th order IIR filter only requires 12 multipliers. This paper compares the performance of different order IIR filter-based PMUs with the performance of the same PMU algorithm using the IEC/IEEE FIR reference filter. The IIR-based PMU easily satisfies all the requirements of IEC/IEEE standard and has a much better out of band signal rejection performance than a FIR-based PMU. Steady state errors for a rated voltage $\pm 10\%$ and a rated frequency ± 5 Hz are $< 0.000001\%$ for total vector error (TVE) and < 1 μ Hz for frequency, with a latency of two mains cycles.

Keywords: phasor measurement unit; PMU; synchrophasor; synchrophasor measurement; IIR filter; IIR step response; IIR group delay; measuring relay; power protection relay; P class; M class

1. Introduction

This paper deals with the algorithm development of a PMU using infinite impulse response (IIR) filters and the resulting simulated performance.

The electrical power supply network is undergoing a rapid transition from a concentrated predominantly fossil fuel based generation system, to a distributed and predominantly renewable based system. The renewable generation has more short term variability and less inertia and that may cause more network stability problems. Synchrophasor measurement devices can be used to monitor the voltage and phase at different parts of a power network and thus maintain stability. These devices are also known as phasor measurement units (PMU). By measuring currents as well, an accurate measurement of power flows in the network can be obtained. The main waveforms are converted into phasors with a magnitude and phase. The phase is differentiated to produce frequency and the frequency is differentiated to produce the rate of change of frequency (ROCOF). The PMU output data contains an accurate time stamp, so that network control centers can rapidly detect power flows, faults, load-generator unbalances, and oscillations. Figure 1, from GE grid solutions PMU brochure [1] illustrates this. There are two classes of PMUs; P (Protection) class, and M (Measurement) class. P class PMUs can be used to operate protection relays to connect or disconnect transmission lines, generators, or loads as needed to maintain network stability. Those P class PMUs need to be able to

detect voltage, phase, or frequency changes in less than two mains cycles. M class PMUs are used for general measurements or after the event fault analysis and their speed of response is less critical.

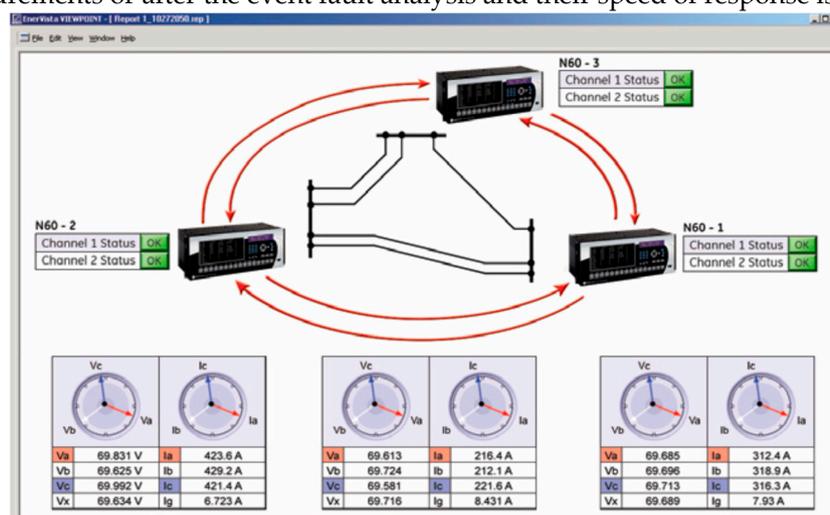


Figure 1. Using PMUs to monitor power network stability [1].

Monti, Roscoe, and Sadu [2] give a good background of PMU requirements and their performance measurement processes. Phadke [3], Usman [4], and Pigati [5] show how PMUs can be used to detect power system faults and operate protection relays thus maintaining the stability and reliability of the power network. The book “Phasor Measurement Units and Wide Area Monitoring Systems” [6] gives a good background on the use of PMUs in power systems. The Hornsdale Power reserve 100 MW/129 MWh battery uses the fast and accurate frequency detection provided by PMUs to quickly dispatch or absorb power to keep the generator-load balance of the network [7]. This frequency control ancillary services (FCAS) capability keeps the network stable and makes the battery very profitable.

1.1. IEC/IEEE PMU Standard

The IEC/IEEE standard 60255-118-1:2018 Part 118-1: Synchrophasor measurements for power systems [8], describes the requirements of PMUs. That standard is an update of the IEEE standard C37.118.1TM-2011 for synchrophasor measurements for power systems [9] and its addendum IEEE standard C37.118.1aTM-2014 [10]. Since the IEC/IEEE standard 60255-118-1 standard is used frequently in this paper, a simple abbreviation “IEC/IEEE Std” is used to refer to it. The IEC/IEEE Std specifies that the total vector error (TVE) under steady state conditions should be less than 1%. Table E.1 of the IEC/IEEE Std foreshadows a change of required accuracy for the PMU algorithm, under steady state conditions, for TVE to 0.01%. The corresponding frequency error (FE) should be less than 5 mHz and the rate of change of frequency error (RFE) should be less than 10 mHz/s. In addition performance requirements are specified under transient and modulation conditions, representing the typical behavior of the power grid. Some of the accuracy requirements of the 2011 standard [9] were too difficult to obtain and in 2014 the accuracy requirements were amended [10]. For instance, the ± 10 mHz/s steady state accuracy for the rate of change of frequency (ROCOF) was relaxed to ± 400 mHz/s for P class PMUs and to ± 100 mHz/s for M class PMUs.

The frequency is calculated by differentiating the measured phase with time. The ROCOF is determined by differentiating the frequency with time. This differentiation increases any high frequency noise, and accentuates the quantization noise. In addition, harmonic frequency components are present in the PMU measurements, so that filtering of the measured PMU data is essential. The IEC/IEEE Std suggests the use of a two main cycle long triangular weighted finite impulse response (FIR) reference filter [8] (pp. 54, D 3).

1.2. Commercial PMU Performance

PMUs are normally built into the protection and control systems produced by major power equipment manufacturers. As such, some do not provide details of their PMU performance. The GE N60 network stability and synchrophasor measurement system instruction manual [11] in Figure 2.4 indicates that the mains waveforms are digitally bandpass filtered using an FIR filter. A half cycle or one cycle Fourier transform is then used to provide the phasor estimation. The frequency is obtained by measuring the time between two negative to positive zero crossings of the waveforms. The waveform sampling frequency is adjusted dynamically to the mains frequency by a fast frequency tracking system. The voltage accuracy is specified as $\pm 0.5\%$ and the frequency accuracy as ± 1 mHz. The ROCOF accuracy is 80 mH/s. The ABB phasor measurement unit product guide [12] has a voltage accuracy of 0.5%, a frequency accuracy of ± 2 mHz, and a ROCOF accuracy of ± 10 mHz/s. No details of the principles of operation are provided. In addition, both [11] and [12] indicate that the equipment satisfies the requirement of IEEE C37.118 [10]. The OpenPMU project [13] uses Python code on low cost Raspberry Pi / Beaglebone Black modules, to realize a PMU. The waveform to phasor conversion is done by least squares curve fitting the mains waveform with a sinewave. As part of that project, Brogan et al. developed a pre-compliance test [14], which allows PMUs to be tested according to the IEC/IEEE Std. Brogan analyzed some commercial PMUs and shows that they fail some of the transient compliance tests of IEEE C37.118 [10]. Goldstein at NIST [15] also evaluated the performance of commercially available PMUs and showed that three out of eleven commercial devices failed some of the accuracy requirements of IEEE C37.118 [10].

1.3. FPGA Advantages

Microprocessors use a clock to execute different programmed steps in a sequential manner, it is possible that an error in reading memory can cause the processor to hang. For critical real time measurements, such as a PMU, this is normally overcome by including a dead-man timer, to reboot the processor if this were to occur. In FPGAs, semi-permanent programmable connections are made in the digital logic hardware. The hardware is event driven, a change in input causes an immediate change in the output. All the required functions are operated in parallel. Clocks can be used to perform some sequential events or to synchronize and buffer data as needed. Modern FPGAs are instantly ON and do not require any programming at startup. Not requiring a dead-man timer, ensures that an FPGA implementation of a PMU has a better reliability than a PMU implemented with microprocessors. The proposed FPGAs includes sufficient hardware multipliers for all the IIR filter stages, so that the digital signal processing (DSP) calculations shown in Figure 2 can be completed in much less than the 0.1 ms sampling period. In comparison, it takes 0.5 ms to perform the multiplications for one new input to an IEC/IEEE Std FIR reference filter with 400 taps using an Intel i7-9700 based PC. The PMUs latency includes both the DSP calculation time and the group delay of the filters used in a PMU algorithm. Minimizing the calculation time allows for a higher group delay of the filters and thus a higher attenuation for out-of-band signals and harmonics.

In an FPGA the word length for different parts of the system block diagram can be tailored to ensure that each part has a similar accuracy, thus optimizing the FPGA real estate. For the system described here, the IIR filters require a much larger word length than the mains waveform IQ down conversion. In this PMU realization, the three phase waveforms are digitized using a 10 kHz sampling rate. The output data rate or “reporting rate” is the same as the sampling rate. The 10 kHz sampling rate requires the DSP of the PMU algorithm, to produce the PMU outputs in less than 0.1 ms. This can be easily achieved in an FPGA. The OpenPMU system and the commercial PMUs described above use clock-based processors and FIR filtering with reporting rates up to 120 times per second. A much higher reporting rate, such as 10 kHz, has an advantage for accurately measuring transients.

1.4. Related Work

Three different techniques exist to provide a static estimation of the magnitude and phase of a mains voltage or current waveform. Firstly, the classic windowed discrete Fourier transform (DFT). Macii [16] describes the optimum window function for obtaining the best phasor accuracy when the

mains frequency does not exactly coincide with a DFT frequency component. He does not describe any proposed hardware implementation. A DFT uses a window function, such as the rectangular window of the rectangular filter in Figure 2 to filter the mains waveform prior to applying a DFT to calculate the amplitude and phase of many frequency components.

The second technique uses an interpolated DFT (IpDFT), where interpolation between frequency components adjacent to the mains frequency are used to obtain a better accuracy of the magnitude and phase of the mains voltage or current. AdhiKari [17] used the national instruments (NI) RIO-based platform and its PMU implementation to investigate different FPGA realizations of PMUs. The algorithm included in the NI advanced PMU development system, uses an iterative interpolated DFT described by Paolone [18]. Romano [19] describes an FPGA-based PMU that uses the iterative interpolated DFT to obtain a TVE from the algorithm of about 0.02%. An iterative technique is used to remove spectral leakage from negative mains frequency components. AdhiKari also indicates that several other FPGA-based PMU implementations use this same technique. Tosato [20] uses a windowed IpDFT to implement a PMU. To minimize out of band frequency components, an elliptic response bandpass IIR filter is used to filter the mains waveforms prior to applying the windowed IpDFT. In the above two techniques, the filtering is applied to the mains frequency (50 Hz) waveforms.

The third technique uses IQ down-conversion followed by low pass filtering as shown in figure D.1 of the IEC/IEEE Std. That technique is used in this paper. Using IQ down-conversion cancels any image frequency components, which are troublesome in the above two techniques.

It appears [20] that most instrument manufacturers use this technique, however manufacturer's brochures [11,12] do not provide these details. The low pass filter recommended by the IEC/IEEE Std is a one cycle long FIR filter with triangular filter coefficients as shown in Figures D.3 and D.4 of the IEC/IEEE Std. As discussed in this paper, those FIR filters are difficult to implement in an FPGA when a high sampling frequency is used. Usman [4] shows a version of IEC/IEEE Std Figure D.1 but does not discuss the filters. Messina [21] uses a phase locked loop (PLL) to change the local oscillator (LO) frequency to track the mains frequency and thus remove any accuracy degradation caused by the mains frequency and the LO frequency being different.

This paper shows that IIR filters have a significant advantage over FIR filters in FPGA real estate requirements and out of band attenuation. Bessel IIR low pass filters have a step response with very low overshoot and a maximally flat group delay. The algorithm presented in this paper is based on IQ down-conversion and using low pass Bessel IIR filters. This results in accurate voltage, phase, frequency, and ROCOF measurements even if the mains frequency deviates from its nominal value.

Toscani [22] developed a PMU algorithm, using space vector transformation instead of IQ down-conversion, followed by filtering the real and imaginary parts of the resulting vectors using Bessel IIR filters. Toscani does not discuss the group delay requirement of the IIR filter. The simulation results are generally significantly worse. As an example, the P class 2nd harmonic distortion TVE of 0.0082% and FE of 4.8 mHz is worse than the 0.001759% and 0.844 mHz for the 6th order IIR filter presented in the 2nd harmonic distortion table in this paper. Toscani does not present any RFE simulation results.

The algorithm presented in this paper produces much lower errors than those published in any of the references.

2. Algorithm Design

2.1. System Block Diagram

Figure 2 shows the block diagram of the PMU algorithm described in this paper. The algorithm is based on the IEC/IEEE Std Figure D.1, with a rectangular filter being used instead of the IEC/IEEE Std FIR filter for the low pass filter. In addition, further low pass Bessel IIR filtering is applied after the phasor conversion.

The 50 Hz mains waveforms are applied to the analogue front end hardware. The waveforms are attenuated and then filtered using a third order anti-aliasing filter with a Bessel response and a

1 ms group delay. The anti-aliasing filter provides 60 dB attenuation at 4 kHz. Those waveforms are then digitized using a 16 bit, six channel, AD7656 ADC. A GPS disciplined oscillator will provide the 10 kHz sampling frequency for the ADC and the PMU timestamp data. The principles described can easily be adapted to other mains frequencies and sampling frequencies. The digitized three phase mains voltage waveforms are shifted to a zero IF signal by IQ down-conversion using digitally synthesized 50 Hz quadrature waveforms. This synthesizer produces Sin(Fr) and Cos(Fr) for down-conversion of phase A, Sin(Fr + 120°) and Cos(Fr + 120°) for phase B and Sin(Fr-120°) and Cos(Fr-120°) for phase C. The resulting I and Q signals can then be filtered using low pass filters. The suggested IEC/IEEE Std implementation in Figure D.1 uses a two cycle long triangular tap FIR filter instead of the rectangular filter. For a 10 kHz sampling frequency, two cycles corresponds to 400 samples, so that allowing for symmetry, 200 different weighted taps are required. The one cycle rectangular filter simply requires 200 additions and some scaling to average the samples over one mains cycle. The frequency response of the rectangular filter has notches of attenuation at 50 Hz and multiples thereof. This provides a high attenuation for image frequency signals and harmonics of 50 Hz after IQ down-conversion.

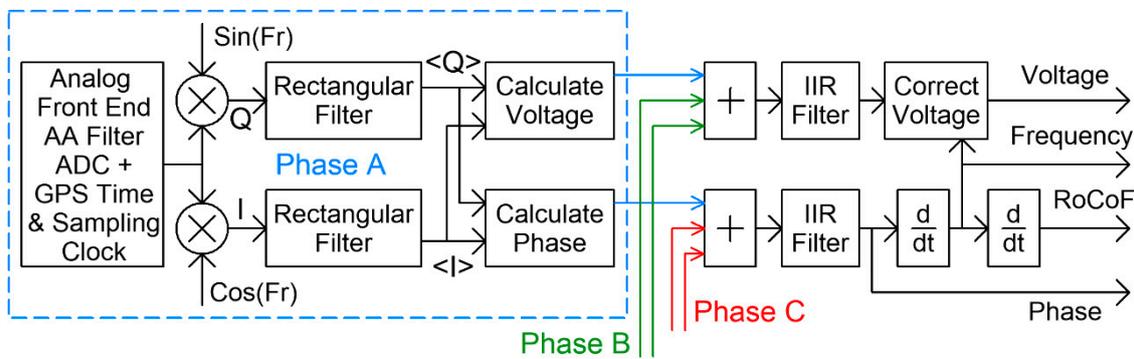


Figure 2. Block diagram of the PMU for FPGA realization.

The IQ signals for each phase are filtered using rectangular filters. The voltage magnitude of the phasor is calculated from the filtered I and Q signals using Equation (1):

$$|V| = \sqrt{\langle I \rangle^2 + \langle Q \rangle^2} \tag{1}$$

The phase of the phasor is calculated using Equation (2):

$$Phase = Atan2\left(\frac{\langle I \rangle}{\langle Q \rangle}\right) \tag{2}$$

The IQ down-conversion, rectangular filtering and Equations (1) and (2) is equivalent to obtaining the magnitude and phase for a single (mains) frequency using a DFT. Calculating a single frequency obviously requires less calculation than doing a whole DFT. For a three phase supply, the voltage magnitude and phase from phases A, B, and C are averaged and used as inputs to the IIR filters in Figure 2.

This combined voltage magnitude and phase has an error, whose amplitude is related to the difference between the LO frequency (Fr) and the actual mains frequency, as shown in Figure 3. A phase error results in frequency and ROCOF errors. The frequency of these unwanted signals is at the 6th harmonic of the mains frequency. In this paper, these unwanted signals are removed from the voltage magnitude and phase waveforms signals of Figure 2, using IIR filters. Alternately a rectangular filter with a notch at the 6th harmonic of the mains frequency can be used. As a result, the extra complexity of a PLL to minimize the difference between the LO and mains frequency is not required.

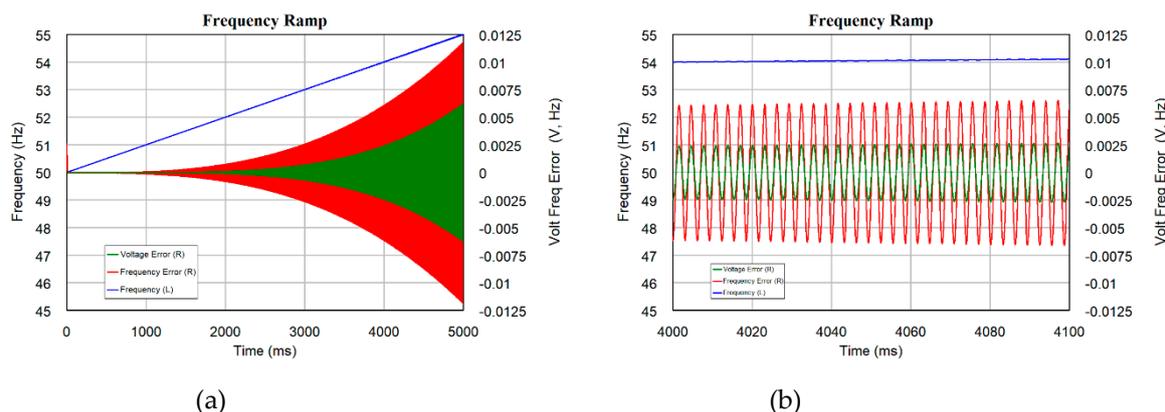


Figure 3. (a) Frequency, frequency error, and voltage error compared to a frequency ramp. (b) Close-up showing the 6th harmonic error signals.

The frequency response of the rectangular filter is a Sinc function and the resulting attenuation versus frequency difference between the LO and mains frequencies for the voltage measurement is corrected for in the “Correct Voltage” block. In the FPGA realization, a lookup table containing correction factors is used for this. The phase measurement is accurate and no correction needs to be made. Having a 10 kHz sampling frequency ensures that the frequency is sufficiently stationary over the three samples used to ensure accurate frequency and ROCOF values. The reporting latency is the time between an event occurring on a power system and the time that it is reported in the data. For a P class PMU this should be < 2 mains cycles. (40 ms for 50 Hz). The total group delay for the PMU’s digital filtering is chosen to be 37 ms, allowing 1 ms group delay for the filtering in the analogue input conditioning hardware of the analog front end block in Figure 1, < 1 ms for the signal processing and < 1 ms for sending the output data to a logging computer, to give a total delay less than 40 ms. The differentiation to produce frequency and ROCOF signals can also be done prior to the IIR filtering. Then, separate IIR filters need to be used for the phase, frequency, and ROCOF signals. That provides additional filtering to the quantization noise produced by the differentiation at the expense of hardware complexity. Whether this reduction in quantization noise is worth using four IIR filters instead of two, is still to be determined after the hardware realization of the PMU.

3. IIR Filter Design

This paper compares the TVE, FE, and RFE performance for PMUs with 4th order to 8th order IIR filters, with those using the reference FIR.

The IEC/IEEE Std requires the PMUs response to a voltage or phase step to have a step response with less than 5% overshoot. The output should be at 50% of the final value at the “reporting time”. The allowable timing error should be less than the “delay time” and be less than 10 ms for a PMU with an output data rate of 50 measurements/s. The PMU presented here has a delay time less than 0.1 ms for all the step response tests 1 to 4 in Table 1. The response time of the PMU is determined as the time after which the PMU satisfies the accuracy requirements for TVE, FE, and RFE. These times are primarily determined by the step response and group delay of the IIR filter. IIR filters are normally realised using the bilinear Z transform, together with cut-off frequency pre-distortion. A Bessel filter has a maximally flat group delay and no overshoot of the step response. When the Bessel pole positions are used together with the bilinear Z transform to calculate the IIR filter coefficients, a slight distortion to the group delay and transient response occurs. This results in a slight overshoot, but that is much smaller than allowed by the IEC/IEEE Std. The results presented here use the bilinear Z transform design procedure [23] with frequency warping.

In this paper, the IIR filters are designed as cascaded second order filters. That results in stable filters with a low limit cycle noise. Figure 4 shows that a second order IIR filter stage requires three multiplications, A, B1, and B2, plus a multiplication by two and additions. A multiplication by two for a floating-point binary number representation is simply adding one to the integer exponent. An

8th order filter operating at the 10 kHz sampling frequency, will thus use 12 multiplications plus additions.

To maximize the dynamic range. The cascaded second order filter sections of IIR filter should be arranged with progressively reducing damping ratios. The first section should have the highest damping ratio and the last section should have the lowest damping ratio. That will minimise the overshoot due to transients in individual filter sections.

To investigate transients on a power system, it is desirable to use a high sampling frequency. The PMU described here, uses a sampling frequency of 10 kHz, resulting in 200 samples per 50 Hz mains cycle. The IEC/IEEE Std Figure D.3 suggests that for a P class PMU a two-cycle long FIR filter with a triangular window function is used instead of the rectangular filter in Figure 2. For a 10 kHz sampling frequency, the FIR filter shown in Figure 5, requires 400 taps with 400 multiplications. Relying on the filter symmetry, the number of multiplications required can be halved. When implemented in an FPGA, each multiplication requires a separate hardware multiplier, unless the multiplications are done successively under the control of a clock. The Alterra Max 10 FPGA [24,25] proposed for the hardware realisation, has 144 hardware 18 bit by 18 bit multipliers plus 50 K programmable logic elements on the FPGA. It is thus not possible to include the total 1200 multipliers required for the six FIR filters, without significant pipelining to reuse multipliers.

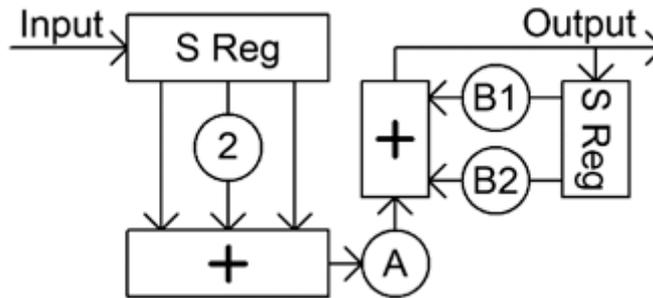


Figure 4. IIR 2nd order filter block diagram.

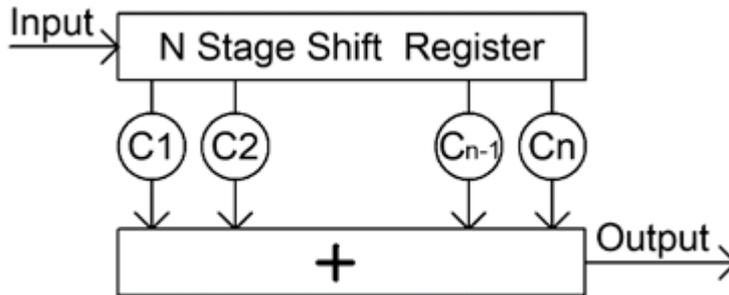


Figure 5. FIR filter block diagram.

The proposed PMU hardware only requires two IIR filters and using an 8th order IIR filter will thus only require six multipliers for the rectangular filters, plus 24 multipliers for the IIR filters. A PMU realisation using IIR filters can thus easily be implemented in the FPGA hardware.

As mentioned above, the total group delay for the digital filters is 37 ms. The rectangular filter of Figure 2 has a 10 ms group delay, so that a 27 ms group delay is available for the IIR filters. Figure 6 shows the step responses of IIR filters realized using the bilinear Z transform. The fourth order IIR filter (IIR4) has a much slower step response and a higher overshoot than the higher order IIR filters. The markers show a 0.8% overshoot for a 4th order filter, 0.6% for a 6th order filter, 0.3% for an 8th order filter, and 0.1% for a 10th order filter. Figure 7 shows the corresponding group delay of these IIR filters. The higher the order of the filter, the flatter the group delay.

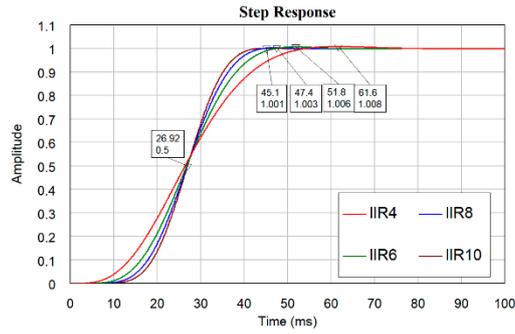


Figure 6. Step response of Bessel IIR filters.

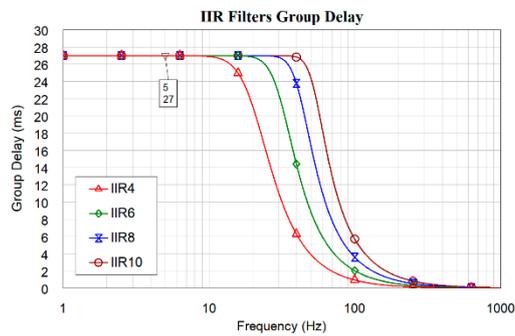


Figure 7. Group delay of Bessel IIR filters.

Figure 8 shows the frequency response of both these IIR filters and the rectangular filter of Figure 2. It can be seen that at 50 Hz, corresponding to the 2nd harmonic mains frequency component after IQ down-conversion, the 4th order filter has the most attenuation and will thus give the best 2nd harmonic rejection in the PMU. That is verified in Table 2. At 100 Hz baseband, corresponding to the 3rd harmonic mains frequency component after IQ down-conversion, the 8th and 10th order IIR filters give the most attenuation. Since below 70 Hz, the 8th and 10th order filters have less attenuation than the 6th order filter, it is not immediately obvious, what order IIR filter will give the best performance in the resulting PMU.

As shown in Figure 2, the ROCOF is produced by double differentiation of the phase signal. The 4th order IIR filter has no high frequency noise attenuation for ROCOF signals, resulting in a poorer noise performance. In addition, the 6th harmonic of mains frequency artifacts, shown in Figure 3 are not attenuated sufficiently by this filter and are present in the PMU output. Figure 9 shows the frequency response of the 8th order IIR filters together with the rectangular filter of Figure 2, as well as the two cycle long FIR filter recommended in Figure D.3 of the IEC/IEEE Std. The red curve of the rectangular filter plus the 8th order IIR filter with a total 1.85 cycle (37 ms) PMU delay, has a much higher high frequency attenuation than the two cycle long FIR filter recommended by the IEC/IEEE Std.

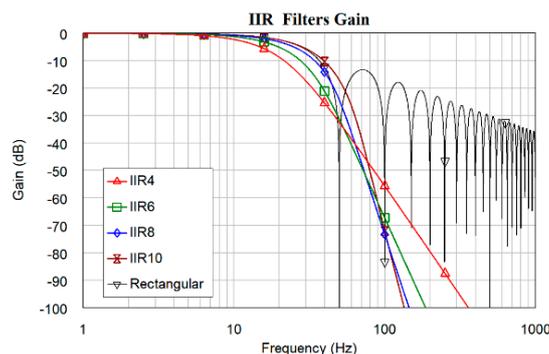


Figure 8. Frequency response of IIR filters.

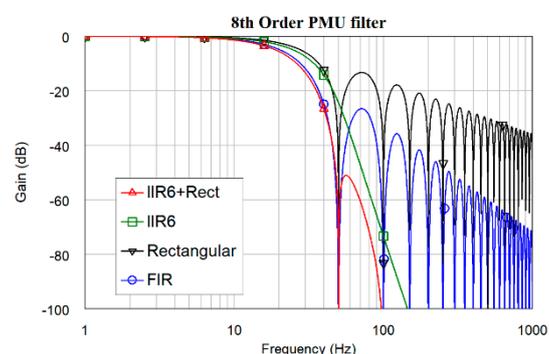


Figure 9. PMU transfer function using IIR and FIR.

4. PMU Simulation Results

4.1. P Class Performance

The IEC/IEEE Std defines a P class PMU as one which is used for power system protection applications “requiring fast response and mandates no explicit filtering”. This paper shows that IIR filtering is very beneficial. The algorithm corresponding to Figure 2, together with Equations 1 and 2 and using different order IIR filters are simulated in MATLAB. The MATLAB implementation of the PMU algorithm has been developed, optimized, and improved over a two year period to ensure an excellent performance and compatibility with FPGA implementation. The IEC/IEEE Std specify the PMU performance requirements, for steady state, transient and voltage, and phase modulation performance. In addition, immunity from mains harmonics is specified. These requirements are implemented as different tests:

Test 1: Apply a $\pm 10\%$ voltage step.

Test 2: Apply a ± 10 degree phase step.

Test 3: Apply a ± 5 Hz frequency step. (Not required in the IEC/IEEE Std)

Test 4: Apply a ± 1 Hz/s frequency ramp for 5 s. Start 50 Hz. End 55 Hz or 45 Hz.

Test 5: Apply a ± 1 Hz/s/s ROCOF ramp for 2 s. Start 50 Hz. End 52 Hz or 48 Hz.

Test 6: Apply $\pm 10\%$ voltage variation at up to 2 Hz sinewave modulation P class, 5 Hz M class.

Test 7: Apply 0.1 rad phase variation at up to 2 Hz sinewave modulation P class, 5 Hz M class.

In the tables presented in this paper, the IIRx-37 rows use filters with a 37 ms total PMU filtering delay, resulting in a 40 ms latency. The 8th order IIR8-39 and IIR8-57 have a total filter delay of 39 and 57 ms, respectively. The FIR filter has a total PMU filtering delay of 21.6 ms. Test 3, being a frequency step is not required as a test for the IEC/IEEE Std. However, it is very useful and test 3 is used to fine-tune the cut off frequency of the IIR filter, to minimize the difference between the generated phase delayed by the desired group delay and the measured phase from the simulation. That ensures that the group delay of all the measurements match the desired group delay, thus

minimizing the TVE, FE, and RFE errors. Table 1 shows the simulated steady-state errors of the final PMU algorithm with the different order IIR filters. To illustrate the advantages of IIR filters, the performance of the same PMU using the IEC/IEEE Std reference FIR filter plus a 6th harmonic filter is included. It can be seen that the PMU algorithm performance using both the IIR and FIR filters is much better than the IEC/IEEE Std requirements. In addition, the PMU response time requirements are satisfied for both the IIR and FIR filters. The TVE response times is < 38.1 ms for a PMU with a 4th order IIR filter, < 31.8 ms for a 6th order IIR filter, < 28.7 ms for a 8th order IIR filter, < 26.7 ms for a 10th order IIR filter, and 26.6 ms for a PMU with the IEC/IEEE Std FIR filter.

Table 1. Simulated P class PMU performance.

Test Number	1	2	3	4	5	6	7
Maximum TVE							
IIR4-37	0.000000%	0.000000%	0.000000%	0.052583%	0.086227%	0.119786%	0.733185%
IIR6-37	0.000000%	0.000000%	0.000000%	0.031215%	0.062484%	0.086877%	0.078188%
IIR8-37	0.000000%	0.000000%	0.000000%	0.025683%	0.050892%	0.071519%	0.064366%
IIR8-39	0.000000%	0.000000%	0.000000%	0.028025%	0.055479%	0.078018%	0.070215%
IIR10-37	0.000000%	0.000000%	0.000000%	0.022481%	0.044988%	0.062624%	0.056360%
FIR	0.000000%	0.000000%	0.000001%	0.021226%	0.042526%	0.059153%	0.053238%
Std Limit	1.0% / (0.01% DSP)		1.0% / (0.5% DSP)			3.0%	
Max Frequency Error mHz							
IIR4-37	0.000	0.000	0.000	0.000	0.069	0.000	2.156
IIR6-37	0.000	0.000	0.000	0.000	0.050	0.000	1.564
IIR8-37	0.000	0.000	0.000	0.000	0.041	0.000	1.287
IIR8-39	0.000	0.000	0.000	0.000	0.045	0.000	1.404
IIR10-37	0.000	0.000	0.000	0.000	0.036	0.000	1.127
FIR	0.000	0.000	0.000	0.001	0.034	0.000	1.065
Std Limit	5 mHz		10 mHz			60 mHz	
Max ROCOF mHz/s							
IIR4-37	0.000	0.000	0.273	0.351	0.022	0.000	27.095
IIR6-37	0.002	0.000	0.008	0.008	-0.001	0.000	19.651
IIR8-37	0.000	0.000	0.000	0.001	0.000	0.000	16.177
IIR8-39	0.000	0.000	0.000	0.001	0.000	0.000	17.647
IIR10-37	0.000	0.000	0.000	0.000	0.000	0.000	14.165
FIR	0.000	0.000	0.214	0.219	0.003	0.000	13.382
Std Limit	100 mHz/s		200 mHz/s			2300 mHz/s	

The IEC/IEEE Std in Annex E describes proposed changes to the accuracy requirements by setting separate requirements for the algorithm. These proposed requirements are shown in Table 1 by appending the word DSP, such as the steady state normal frequency requirement of (0.01% DSP). The algorithm described in this paper easily satisfies these requirements for all the PMUs in Table 1.

4.2. Harmonic Performance

As shown in Figures 8 and 9, the attenuation of the IIR + rectangular or the FIR filter around 50 Hz, corresponding to the mains second harmonic frequency after IQ down-conversion, is much less than the attenuation around 100 Hz. As a result, the performance for the second harmonic of the mains frequency, is the most critical. Table 2 shows the mains harmonic performance of the first seven harmonics for a 48 Hz mains frequency, when a 1% single harmonic of appropriate sequence is added to the three-phase waveform. If the mains frequency is 50 Hz then all the harmonics cause no error in the measured voltage, phase, frequency, or ROCOF. The magnitude of TVE, FE, and RFE errors increase with the deviation from the desired mains frequency, so the results in Table 2 are the critical

ones. The IEC/IEEE Std specifications are for ± 2 Hz deviation from the desired mains frequency. A 48 Hz mains waveform has a second harmonic at 96 Hz, which is down-converted to 46 Hz. The second harmonic of a 52 Hz mains waveform is down-converted to 54 Hz. The IIR + rectangular filter attenuation at 46 Hz is far less than that at 54 Hz, so the PMU harmonic rejection for a 48 Hz mains frequency is worse than for a 52 Hz mains frequency. As a result, only the performance for a 48 Hz mains frequency is shown in Table 2. For the IIR-PMU, the errors decrease monotonically with harmonic number. The 6th order IIR-PMU satisfies all the IEC/IEEE Std limits. Tables 1 and 2 show that the 8th order IIR-PMU overall has a better performance than the 6th order IIR-PMU, but as figure 8 shows, it has less attenuation at 50 Hz and thus a worse performance for the second harmonic errors.

The bold numbers in Tables 2 and 3 are results that are outside the IEC/IEEE Std limits.

Table 2. Simulated P class PMU harmonic performance.

48 Hz, Each harmonic 1% amplitude						
Harmonic	2	3	4	5	6	7
Maximum TVE						
IIR4-37	0.001346%	0.000066%	0.000013%	0.000006%	0.000004%	0.000004%
IIR6-37	0.001759%	0.000026%	0.000006%	0.000005%	0.000004%	0.000004%
IIR8-37	0.003742%	0.000019%	0.000005%	0.000004%	0.000004%	0.000004%
IIR8-39	0.002380%	0.000013%	0.000005%	0.000004%	0.000004%	0.000004%
IIR10-37	0.008025%	0.000022%	0.000005%	0.000004%	0.000004%	0.000004%
FIR	0.005049%	0.00224%	0.001234%	0.000612%	0.000185%	0.000081%
Std Limit	1.0%					
Max Frequency Error mHz						
IIR4-37	0.646	0.062	0.016	0.006	0.004	0.002
IIR6-37	0.844	0.023	0.003	0.001	0.000	0.000
IIR8-37	1.796	0.016	0.001	0.000	0.000	0.000
IIR8-39	1.142	0.009	0.000	0.000	0.000	0.000
IIR10-37	3.852	0.019	0.000	0.000	0.000	0.000
FIR	2.423	2.235	1.994	1.520	0.875	0.196
Std Limit	5 mHz					
Max ROCOF mHz/s						
IIR4-37	194.827	37.680	14.659	7.545	4.494	2.872
IIR6-37	254.565	13.781	2.412	0.700	0.268	0.119
IIR8-37	541.644	9.808	0.779	0.128	0.034	0.010
IIR8-39	344.484	5.598	0.441	0.072	0.019	0.005
IIR10-37	1161.631	11.357	0.415	0.039	0.011	0.001
FIR	730.824	1348.038	1803.770	1.832225	1312.880	354.483
Std Limit	400 mHz/s					

The third harmonic distortion performance for the 8th order IIR filter is much better than that of the 6th order IIR filter. Typical mains waveforms have much higher third harmonic distortion than second harmonic distortion, so an 8th order IIR filter should be preferable in a commercial instrument. The IEC/IEEE Std in Annex E indicates a proposed increase in the latency by 2 ms. Table 2 shows that by increasing the delay from 37 to 39, the 8th order IIR filter (IIR8-39) has a second harmonic RFE of 0.344484 Hz/s, which is inside the IEC/IEEE Std specifications.

4.3. Performance with Noisy Waveforms

To further compare the performance of the IIR-based PMU systems, a three-phase waveform with filtered voltage and frequency noise being added to the waveforms was generated, a 1% 3rd harmonic was included in this waveform to represent saturation caused by transformers. A 10 kHz sampling rate was used as before. To allow others to compare their PMU systems with the one presented in this paper, the PMU data and their resulting waveforms can be obtained from the link in the supplementary materials heading at the end of this paper. This same waveform 20 s long was then used as input to the PMU algorithm implementations for the different order IIR filters and the IEC/IEEE Std FIR + 6th harmonic notch filter. Table 3 shows the error performance obtained for this waveform with the different PMUs. The errors for all IIR-PMU systems are much less than the IEC/IEEE Std requirements. The FIR-PMU ROCOF errors, shown in bold, do not satisfy the IEC/IEEE Std requirements. Table 3 shows a decreasing error with an increase in IIR filter order. Since the generated waveform is very noisy, the RMS errors are a better indication of the overall performance than the maximum errors. For comparison, an M class 8th order IIR-PMU with a group delay of 57 ms, described in Section 4 below is included. The M class PMU has slightly higher errors, since it filters out more of the band noise that is included in the generated voltage, frequency, and ROCOF waveforms.

Table 3. Simulated P class and M class PMU noisy waveform performance.

	Max TVE (%)	Max FE (mHz)	Max RFE (mHz/s)	RMS TVE (%)	RMS FE (mHz)	RMS RFE (mHz/s)
IIR4-37	0.5608%	24.400	1470.9	0.1720%	7.443	379.707
IIR6-37	0.4084%	17.974	1083.6	0.1250%	5.450	282.173
IIR8-37	0.3372%	14.951	903.8	0.1031%	4.523	236.760
IIR8-39	0.3672%	16.219	978.9	0.1124%	4.913	255.652
IIR8-57	0.7277%	30.659	1828.4	0.2236%	9.448	464.575
IIR10-37	0.2958%	13.196	795.0	0.0904%	3.984	210.155
FIR	0.29631%	12.985	2450.7	0.0845%	3.851	491.722
Std Limit	3.0%	60 mHz	2300 mHz/s			

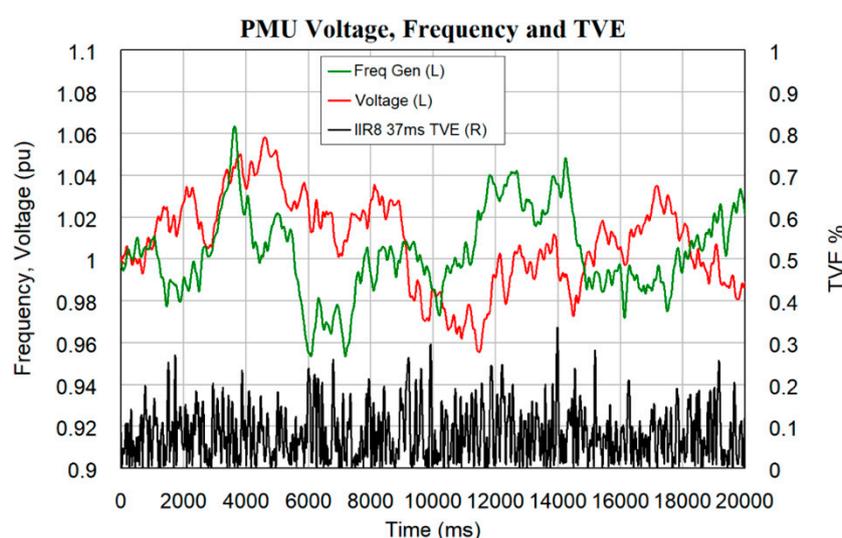


Figure 10. Voltage, frequency, and TVE of generated waveform.

Figure 10 shows the generated voltage, frequency, and TVE of the three-phase waveform used to produce the results shown in Table 3. Figure 11 shows a close-up of the frequency errors of the 8th order IIR-PMU filter and the FIR-PMU when the mains frequency deviated from the nominal frequency by about 5%. It shows the absence of 3rd mains harmonic errors from the IIR-PMU, but

the presence of significant 3rd harmonic errors in the FIR-PMU output. Figure 12 shows a close-up of the corresponding ROCOF errors and again shows the large difference in the 3rd mains harmonic errors between the IIR-PMU and the FIR-PMU. Figures 11 and 12 show that the IIR based PMU has a much better out of band signal rejection performance than the FIR-PMU.

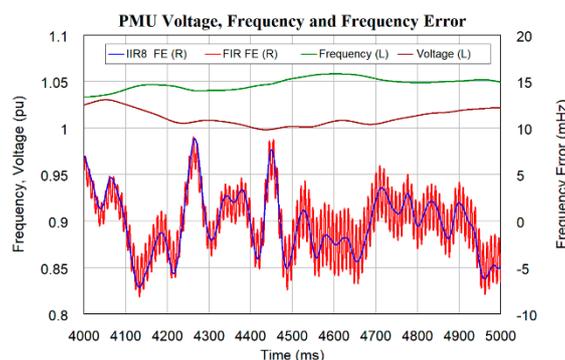


Figure 11. Close-up of frequency errors.

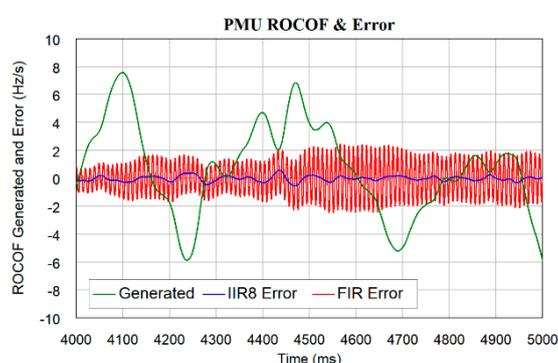


Figure 12. Close-up of ROCOF errors.

4.4. IIR Filter Selection

From the performance shown in Tables 1 to 3, the following observations can be made. Increasing the IIR filter order reduces the errors for tests 1 to 7. In addition, increasing the IIR filter order reduces the response time of the PMU incorporating those filters. However, as Figure 8 shows, increasing the IIR filter order reduces the attenuation at 50 Hz and as Table 2 shows then reduces the second harmonic rejection of the PMU. The 4th order IIR-PMU satisfies all the IEC/IEEE Std requirements, however, it has the worst performance of the IIR-PMUs in Table 1. When the phase output is differentiated to produce the ROCOF signal, a flat spectral density quantization noise results. The 10th order IIR-PMU has too high a second harmonic ROCOF error performance and also requires more hardware to implement. The 4th and 10th order filters can thus be ruled out for the realization of a P class PMU. The 6th order IIR-PMU satisfies all the IEC/IEEE Std requirements. Tables 1 and 3 show that the 8th order IIR-PMU has a better performance than the 6th order IIR-PMU, it produces less high frequency noise, and it has a better attenuation for 3rd and higher harmonics. However, with the 37 ms delay it does not quite satisfy the 2nd harmonic RFE requirements in Table 2. Increasing the delay by 2 ms as is proposed by the IEC/IEEE Std in Annex E results in an 8th order IIR-PMU that satisfies all the requirements. It is thus worthwhile to realize the PMU using 8th order IIR filters.

4.5. Comparison with FIR Filters

To compare the performance of IIR-PMUs with FIR-PMUs, the rectangular filter in Figure 2 is replaced with the IEC/IEEE Std recommended FIR filter. Figure 3 shows that a frequency deviation

from the nominal mains frequency causes errors at the 6th harmonic of the mains frequency. The IIR filters attenuate those error signals sufficiently, however the IEC/IEEE Std FIR filter does not have sufficient attenuation at the 6th harmonic of the mains frequency. To provide sufficient 6th harmonic attenuation for the FIR-PMU simulation, the IIR filter in Figure 2 is replaced with a 6th harmonic filter consisting of a rectangular filter with one sixth of a cycle length. This rectangular filter is included in all the FIR results presented in this paper. Table 1 shows that the resulting FIR-PMU performance is very similar to that of a PMU using IIR filters. However, Table 1 shows that the ROCOF performance for the frequency step in tests 3 and the frequency ramp in test 4 is far worse, due to these 6th harmonic signals not being sufficiently attenuated, even with this extra filter.

Table 2 shows that the performance of the FIR-PMU with harmonics being present, is far worse than the performance of the IIR-PMU. Without the 6th harmonic rectangular filter, the harmonic ROCOF errors for the FIR-PMU rise proportional to the harmonic. Table 2 shows that, even with the 6th harmonic filter, the FIR-PMU does not satisfy the harmonic requirements of IEC/IEEE Std. For up to the 18th harmonic, only the 14th harmonic for a 48 Hz mains waveform and the 7th, and 13th harmonic for a 52 Hz mains waveform gave RFE errors that satisfied the IEC/IEEE Std. All the TVE and FE measurements satisfied the IEC/IEEE Std.

The FIR and 6th harmonic filter have a group delay of 21.6 ms, so that an IIR filter with a group delay of 15.4 ms could be included to give a total group delay of 37 ms to the FIR-PMU. Using a 6th order IIR for this result in an FIR+IIR-PMU with a similar performance to the 6th order IIR-PMU. This FIR+IIR-PMU satisfies all the IEC/IEEE Std performance requirements. Such a PMU requires all the multipliers needed for a FIR filter, as well as the multipliers for IIR filters. Such a PMU is much more complex in hardware for a similar performance to that of a 6th order IIR-PMU.

When comparing the FIR-PMU and the IIR-PMU, tables 1 and 3 show that overall there is little difference in performance between the 8th order IIR-PMU and a PMU with an FIR filter followed by a 6th harmonic filter. Table 2 shows that the second harmonic performance of the FIR-PMU does not satisfy the requirements of the IEC/IEEE Std. Table 3 and Figures 10 to 12 show that the FIR-PMU has a poorer performance for frequency and ROCOF accuracy than the IIR-PMU. Using IIR filters will thus have both hardware and performance advantages.

4.6. M Class PMU Performance

An M class PMU is one used in “analytic measurements often require greater precision but do not require minimal reporting delay.” IEC/IEEE Std indicates that “The user must choose a performance class that matches the requirements of each application”. The IEEE limit in Table 1, shows the highest accuracy requirement of IEC/IEEE Std for either P class or M class. The modulation frequency used in tests 6 and 7 is increased from the 2 Hz for P class, shown in Table 1, to 5 Hz for M class. Simulations for tests 6 and 7 with 5 Hz modulation result in a TVE < 0.74% for all the IIR and FIR filters, with 3% allowed in the standard. The largest frequency error is < 40 mHz, with 300 mHz allowed and the largest RFE is 1040 mHz/s, with 14,000 mHz/s allowed. The PMU algorithms described in this paper will thus satisfy the tests in Table 1 for either class of operation with a significant performance margin.

Table 2 shows the harmonic performance with the 1% harmonic amplitude specified for P class PMUs. Increasing the harmonic amplitude to 10% as required for M class PMUs will increase the errors by close to 10 times since the algorithm performance is very linear. It may be desirable for a network operator to allow for a slight increase in latency from the two mains cycles to say three mains cycles in order to increase the immunity to mains harmonics. To investigate this the cut off frequency of the IIR filters were changed to increase the PMUs total group delay from 37 (1.85 mains cycle) to 57 ms (2.85 mains cycle). The performance of the resulting IIR-PMUs was then investigated and compared with the IEC/IEEE Std requirements.

For an M class PMU, more filtering is required than for a P class PMU, so 4th order IIR filters are not considered, and the PMU performance is evaluated using 6th order to 10th order IIR filters. The resulting 2.85 cycle delay IIR-PMUs satisfies all the TVE, FE, and RFE error requirements for both P class and M class PMUs, for all the tests in Table 1, with a significant margin. By increasing the group

delay, the response times are increased in proportion. For 6th order to 10th order IIR-PMUs the TVE response times are less than 2.85 mains cycles. Applying a 3/2 times scaling to the response times for FE and RFE, shows that all response time requirements are easily satisfied.

For calculating the harmonic performance for the M class PMU, a maximum harmonic amplitude of 10% of the mains voltage is added to the mains waveform. For 57 ms delay IIR-PMUs with 6th order to 10th order IIR filters, the following performance was obtained for second harmonic errors with a 48 Hz mains frequency: The maximum TVE = 0.002%, the maximum FE = 0.54 mHz, and the maximum RFE = 160 mHz/s. That is much less than either the P class or M class IEC/IEEE Std limits. Using higher harmonics or the 52 Hz mains frequency result have smaller errors still. Plotting the TVE, FE, and RFE for the waveforms used for Table 3, shows increased low frequency errors compared with the results in Figures 10 to 12. This is to be expected since the 8th order IIR filter for a 37 ms delay PMU has a 3 dB cut off frequency of 19.0 Hz and the same filter for a 57 ms delay PMU has a cut off frequency of 10.9 Hz. The TVE, FE, and RFE are the errors between the generated voltage, frequency, and ROCOF, and their corresponding measured values. The generated voltage, frequency, and ROCOF contain out of band noise that is filtered out by the PMU and is flagged as errors, even though the noise is part of the generated waveforms.

The performance of an M class FIR-PMU including a 6th harmonic rectangular filter and a 6th order IIR filter to give a 57 ms delay is evaluated. The IIR group delay is 35.2 ms and is thus the dominant delay. The simulated performance of this FIR+IIR-PMU is very similar to that of a 6th order IIR-PMU. The extra hardware complexity in using the IEC/IEEE Std reference FIR filter in a PMU is thus not justified as it does not increase the performance.

The only difference between an 8th order IIR-PMU with a 37 ms delay and a 57 ms delay is the value of the filter coefficients. It is thus very easy to convert from a P class PMU to an M class PMU by simply reprogramming the FPGA with different IIR filter coefficients.

5. IIR Filter Realization

To make best use of the available dynamic range, the IIR filters need to be arranged so that the first 2nd order section has the highest damping ratio and the last 2nd order section has the lowest damping ratio. The 6th order IIR filter has a 3 dB cut off frequency of 15.94 Hz and the 8th order IIR filter has a 3 dB cut off frequency of 18.74 Hz for a 27 ms IIR filter group delay. With a 10 kHz sampling frequency, the fractional bandwidth is thus less than 0.2%. As a result, the IIR filter operation involves subtracting large numbers with very small differences. To determine how many bits are required for the floating point arithmetic, the difference between the step response, gain, phase, and group delay for a double precision and a floating point integer MATLAB implementation is performed.

The IEC/IEEE Std in Table E1 indicates a proposed 0.01% TVE accuracy requirement for the algorithm under steady state conditions. A 0.00573° phase error corresponds to a 0.01% TVE, if the magnitude is accurate. Similarly, a 0.01% magnitude error corresponds to a 0.01% TVE, if the phase is accurate. The 16 bit ADC proposed for the hardware has an accuracy of 0.004% if a 40% overload is allowed. If the phase accuracy or gain accuracy of the whole algorithm is 0.001% or 0.000573° then the accuracy will primarily be determined by the ADC and analogue hardware. The IIR filter accuracy should contribute less than 10% of that desired error. For the IIR filters, the accuracy requirements are thus 0.0001% (1E-6) for gain and 0.0000573° (5.7E-5) for phase.

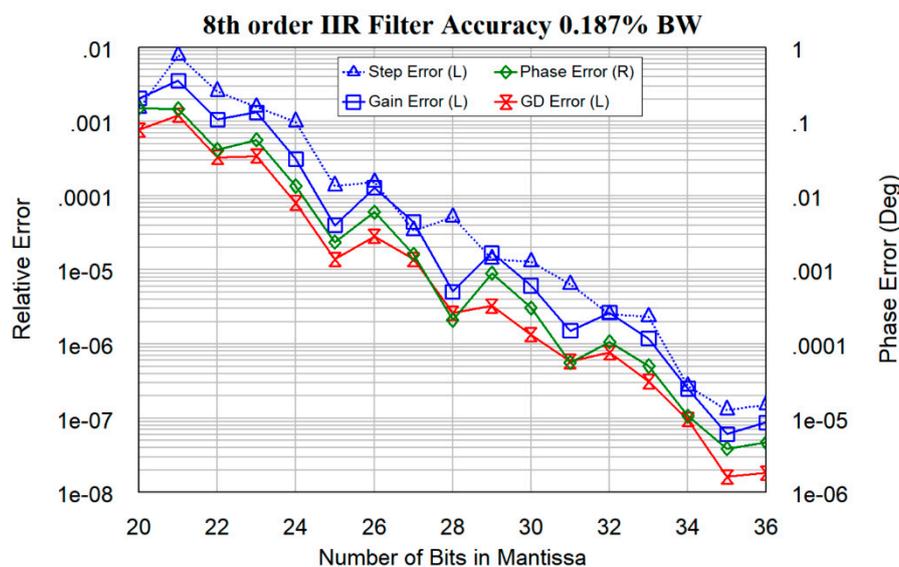


Figure 13. 8th order IIR filter bit length versus accuracy.

Figure 13 shows the errors resulting in realizing the 8th order IIR filters using different bit lengths for the floating-point integer arithmetic. Eight bits are used for the exponent. Figure 13 shows that 34 or more bits are required for the mantissa to meet the above accuracy requirements. The hardware multipliers in the FPGA have 18 bit inputs and 36 bit outputs. Four of these can be connected to form a 36 bit by 36 bit input multiplier. The 72 bit output is normally converted to a 34 or more bit mantissa floating point integer. From Figure 4, an 8th order IIR filter will thus require $4 \times 4 \times 3 = 48$ multipliers. By using some sequential or pipelined operation, it is possible to reduce that number if the FPGA capacity is exceeded. The 6th order IIR filter requires a 0.159% bandwidth and its number of bits versus accuracy plot is similar to Figure 13. The 6th order IIR filter also requires 34 or more bits for the mantissa to meet the above accuracy requirements. The IIR filters can thus easily be realized with sufficient accuracy in the FPGA.

6. Current and Future Work

Work is currently underway to implement the FPGA algorithm and IIR filters described in this paper in a DE10-Lite FPGA development board [24], containing an Alterra Max 10 FPGA [25]. The “Calculate Voltage” and “Correct Voltage” blocks in Figure 2 can all be implemented as lookup tables, with either quadratic or fourth order interpolation. The atan2 function in Equation 2, required for the “Calculate Phase” block in Figure 2 can either be implemented using a Cordic algorithm or using lookup tables. The hardware real estate requirements and calculation times for that are currently being investigated.

The first version of the analogue hardware to buffer, filter, and digitise the three-phase mains waveforms is complete, but requires minor modifications to the PCB. That hardware includes a six channel, 200 kSPS, 16 bit ADC, so that the PMU can be extended to include measurements of currents in the future. A 16 bit ADC has sufficient accuracy to satisfy the accuracy requirements for the PMU. The GPS disciplined VCXO hardware, to control the sampling clock and the GPS time stamp, is complete and the VHDL coding for its control is being implemented in the FPGA. The Labview software to display the measured data has been developed, but still needs to be tested using the final FPGA implementation. The resulting PMU will then undergo testing using real three-phase waveforms.

7. Conclusions

PMUs need to be very reliable and produce trustworthy measurement data. In an FPGA semi-permanent hardware, connections are made to perform the required PMU algorithm functions.

Having a high sampling and data output rate of about 10 kSPS, allows an accurate power system transient performance to be obtained. At these sampling rates, the number of hardware multipliers available on FPGAs is insufficient to allow FIR filters to be implemented without making compromises. IIR filters have the advantage of requiring only three multipliers per 2nd order stage.

The same PMU algorithm was used to compare IIR-based PMUs and FIR-based PMUs. It was shown that for most IEC/IEEE Std tests, P class IIR-PMUs have a similar performance to an FIR-PMU, using the recommended P class FIR. However, IIR-based PMUs have a much better ROCOF performance and a better out of band signal immunity performance as shown in the mains harmonic tests. The 4th, 6th, and 8th order IIR filter-based PMUs pass all the IEC/IEEE Std harmonic tests, but the FIR-based PMUs fail those. IIR-based PMUs require significantly less FPGA real estate and are thus the obvious choice for realizing the signal processing for an accurate PMU using a low cost instant ON FPGA.

Supplementary Materials: The following are available online at www.mdpi.com/xxx/s1, The PMUData.txt and WaveData.txt files, used to produce Table 3 and Figures 10 to 12, and the instructions on how to use them. These files are provided so that others can use them to test their PMU algorithms.

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