Analysis of the Voltage-Dependent Plasticity in
Organic Neuromorphic Devices

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Abstract: The bias-dependent signal transmission of flexible synaptic transistors is investigated. The novel neuromorphic devices are fabricated on a thin and transparent plastic sheet, incorporating a high-performance organic semiconductor, dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene, into the active channel. Upon spike emulation at different synaptic voltages, the short-term plasticity feature of the devices is substantially modulated. By adopting an iterative model for the synaptic output currents, key physical parameters associated with the charge carrier dynamics are estimated. The correlative extraction approach is found to yield the close fits to the experimental results, and the systematic evolution of the timing constants is rationalized.

Keywords: flexible electronics; neuromorphic engineering; organic field-effect transistors; synaptic devices; short-term plasticity

1. Introduction

Neuromorphic engineering is an emerging technological area, which aims at mimicking the biological functionalities of neurons, synapses, or a whole brain by various electronic materials and devices [1–6]. Recently, the use of organic electronics in neuromorphic systems has gained tremendous attention, thanks to its capacity to expand the technological scope of such systems by creating unconventional interfaces such as direct neuroprotheses and robotic sensory bridges [7–10]. There are many possible routes to organic-based neuromorphic architecture, including electrochemical [11,12], memristive [13], and field-effect approaches [14–16]. Among them, organic field-effect transistor (OFET)-based synaptic devices are a particularly promising element, considering the possibility of a fully solid-state, flexible neuromorphic chip that leverages the versatility of OFETs in constructing various circuit building blocks [17–20]. Despite the rapidly growing technological viability of OFET synapses, there is still a lack of understanding on fundamental phenomena prevailing at the single-device level, which acts as a current bottleneck for the development of organic-based complex neuromorphic hardware systems. We recognize this issue, and present here a detailed analysis of one specific neuromorphic functionality, namely the short-term plasticity (STP) in flexible OFET synaptic devices. By combining experimental measurements and numerical modeling, systematic understanding of the voltage-dependent transmission behavior at the synaptic junction is obtained. By increasing the input-spike voltage magnitude, slowing down of both charging and discharging is observed, as the floating carrier reservoir turns electrostatically populated. The detailed analysis from this study builds a solid foundation for advanced models and the realization of flexible organic neuromorphic circuitries.

2. Experimental Methods

The organic synaptic transistors based on a floating-gate OFET architecture were fabricated with dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) semiconductor (Figure 1a), according to the
bottom-gate, top-contact structure depicted in Figure 1b. A key to this device is the utilization of the ultra-thin, flat Al nanolayer, which is surface-oxidized to form an Al/AlOx stack [16]. The device fabrication processes are summarized as follows. The gate substrate is prepared as a flexible and transparent polyethylene terephthalate (PET) sheet, which has a predeposited conducting indium tin oxide (ITO) film (130 nm) (surface resistivity 60 Ω/sq, Sigma-Aldrich). The ITO surface was planarized by a 40-nm thick poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS, Clevios™, Heraeus) buffer layer to reduce the gate leakage. Then, insulating poly(methyl methacrylate) (PMMA, M.W. = 120,000, Sigma-Aldrich) was spin-coated from a toluene solution to serve as a blocking dielectric (410 nm). The Al functional layer with a nominal thickness of 3 nm was thermally evaporated and exposed to ambient air for oxidation. DNTT (sublimed grade, 99%, Sigma-Aldrich) was vacuum-evaporated for a hole-transporting molecular channel (50 nm). Finally, the Au source/drain electrodes (30 nm) were evaporated through a shadow mask.

![Figure 1](image-url)

**Figure 1.** (a) Chemical structure of dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT), used as an active molecular material in organic synaptic transistors. (b) Cross-sectional illustration of the device structure. (c) Circuit diagram employed for the measurement of voltage-dependent synaptic plasticity. (d) Model illustration: Biological processes relevant to the neuronal signal transmission through release and re-uptake of neurotransmitters and the electronic processes that mimic such properties through trapping-mediated hole transport at the semiconductor channel.

For emulating the STP behavior, we used the quasi-two-terminal electrical configuration shown in Figure 1c. Here, the gate and drain electrodes were externally wired and connected to a common computer controlled source-measure unit (Keithely 2400). The synaptic voltage ($V_{syn}$) pulses were generated by using a LabVIEW code, for them to have a specific number of sharp spike-like electrical stimulation stages with varying frequencies. The synaptic current ($I_{syn}$) was measured as a function of time as the output signal.

3. Results and Discussion

Materials characterization including atomic force microscopy (AFM) and transmission electron microscopy (TEM) as well as the basic transistor characterization such as transfer, output, mobility measurements has been reported in our previous paper [16]. Here, we introduce a numerical model that is applied to analyze the experimental STP. It is based on the functional model initially developed for nanoparticle organic memory field-effect transistors (NOMFET), by Bichler and co-workers [21]. In this study, we modify the notations and introduce the correlative parametrization approach, so that
it can better describe our synaptic devices. Let’s first recapitulate the physical meaning of such a model, by drawing a parallel between a biological synapse and a synaptic transistor channel. As shown in Figure 1d, the communication through a biological synapse is signaled by the action potential of the presynaptic neuron, which in turn activates the release of neurotransmitters toward the postsynaptic neuron. Part of these chemical messengers are eventually pulled back into the presynaptic neuron through re-uptake. Therefore, a specific time-domain pattern of neural signals conditions the dynamic variation of synaptic strength. Similarly, in our OFETs, holes accumulated at the DNTT channel serve as electronic signal carriers. Since the $V_{syn}$ is bound to drain and gate, part of the transporting holes are trapped into the Al floating gate when a spike arrives. These trapped carriers can be easily detrapped into the channel, which is a key feature of our transistors with an ultra-thin tunnel oxide. Therefore, the STP behavior can be emulated by adjusting the input $V_{syn}$ pulses.

For the square-type input $V_{syn}$ waveform consisting of varying frequency and duty cycles, the direct relationship between the $n$th synaptic current $I_n$ and the $(n+1)$th one $I_{n+1}$ can be iteratively established. As an intermediate, the current $I_{n+}$ is the value at the falling edge of each synaptic spike and is dictated by how much the floating gate is charged during that pulse, which is written as

$$I_{n+} = I_0 \exp \left( -\frac{W}{\tau_1} \right) + I_0 \left[ 1 - \exp \left( -\frac{W}{\tau_1} \right) \right]$$

(1)

where $W$ is the activation pulse width, $\tau_1$ is the trapping time constant, $I_0$ is the initial current, $\Delta E_F$ is the semiconductor Fermi-level shift at the fully charged state of the floating gate, $k$ is the Boltzmann constant, and $T$ is the absolute temperature. Between two pulses (while $V_{syn} = 0 \text{ V}$), the carriers now leave the floating gate by natural detrapping, partially recovering the channel current, expressed as

$$I_{n+1} = I_{n+} \exp \left( -\frac{W}{\tau_d} \right) + I_0 \left[ 1 - \exp \left( -\frac{W}{\tau_d} \right) \right]$$

(2)

where $T_p$ is the pulse time period and $\tau_d$ is the detrapping time constant. Merging Equations (1) and (2) gives the final model

$$I_{n+1} = I_n \exp \left( -\frac{W}{\tau_1} \right) \exp \left( -\frac{W}{\tau_2} \right) + I_0 \left[ 1 - \exp \left( -\frac{W}{\tau_1} \right) \right] \exp \left( -\frac{W}{\tau_2} \right) + \left[ 1 - \exp \left( -\frac{W}{\tau_2} \right) \right]$$

(3)

To gain insights into the voltage-dependent signal transmission properties, we experimentally recorded the STP behavior of the same transistor, at different magnitudes of $V_{syn}$ as $-4$, $-6$, $-8$, and $-10 \text{ V}$. The composition of the input signals (i.e., the frequency sequence and the number of spikes at each stage) was kept the same except for the voltage magnitude. Our test input waveforms consisted of six stages with the frequencies of 5, 1, 0.2, 2, 4, and 0.5 Hz. These frequencies determine the value of $T_p$, and $W$ was fixed as 20 ms. Therefore, the remaining task in modeling is to fit the experimental $I_{syn}$ data by determining four parameters, which are $I_0$, $\Delta E_F$, $\tau_1$, and $\tau_d$. Instead of setting all these fitting parameters free, we employed a correlative extraction approach for more physically reliable results. The main idea is that the asymptotic final current $I_0 \exp(-\Delta E_F/kT)$ should reflect the same amount of trapped carriers, and therefore have a quadratic dependence on the $V_{syn}$ magnitude considering the forced saturation-regime transistor operation. To systematically apply this method, we first extracted the four fitting parameters from the data set at the lowest value of $V_{syn} = -4 \text{ V}$. Then, we calculated the $I_0 \exp(-\Delta E_F/kT)$ value for $V_{syn} = -4 \text{ V}$, and then let this base asymptotic limit quadratically increase with increasing $V_{syn}$. Therefore, for the three other data sets ($V_{syn} = -6$, $-8$, and $-10 \text{ V}$), the apparent initial $I_0$ value together with the prefixed $I_0 \exp(-\Delta E_F/kT)$ value allowed for the unambiguous calculation of $\Delta E_F$ for each $V_{syn}$.

Figure 2a shows that $I_0$ monotonously increases in magnitude with increasing $V_{syn}$ values, which is accounted for by the channel current flow enhanced by both gate (free carrier density) and drain voltages (lateral electric field) [18]. Interestingly, the $\Delta E_F$ follows a similar trend before experiencing a small drop at a high $V_{syn}$. This evidences that gate-induced trapping (decreasing the free carriers) and
gate-enhanced hole accumulation act together to set the right balance for the Fermi level approachable at the fully charged state [22]. The inset of Figure 2a confirms that the magnitude of \( V_{\text{syn}} \) and the asymptotic synaptic current follows the quadratic dependence, evidenced by slope 2 on this log-log representation.

Figure 2. (a) The change of \( I_0 \) and \( \Delta E_F \) as a function of voltage, estimated by the correlative approaches. Inset: the log-log plot showing the quadratic dependence of the final current on the synaptic voltage. (b) The extracted time constants for the trapping and detrapping processes.

Having determined the values of \( I_0 \) and \( \Delta E_F \), the two timing constants were estimated by performing global fitting to the experimental results. Figure 2b shows that despite the ultra-thin nature of our AlOx favoring spontaneous relaxation, the detrapping time constant \( \tau_d \) is greater than the trapping counterpart \( \tau_t \) at all voltage biases considered. Another important finding here is that the magnitude of \( V_{\text{syn}} \) can substantially influence the ratio between \( \tau_d \) and \( \tau_t \) values, implying a direct impact on the STP modulation.

Figure 3 shows the direct comparison between the experimental STP results and the model currents reproduced by inserting the parameters in Figure 2 into Equation (3). Similar STP behaviors have been observed in several field-effect synaptic transistors [14–16]. In brief, we can notice that even with the constant magnitude of \( V_{\text{syn}} \), the produced \( I_{\text{syn}} \) quite significantly changes its magnitude responding to the spiking frequency. At a high \( V_{\text{syn}} \) frequency, a monotonous decrease in current is monitored because the negative gate pulse traps holes from the channel into the floating gate. When this frequency decreases, the amount of holes escaping the traps (per time) can exceed that of the holes being trapped into the floating gate, so that the \( I_{\text{syn}} \) gradually recovers its strength. In Figure 3, the model-calculated values are in a broad agreement with the measurements, and showed a similar trend in STP modulation. With increasing \( V_{\text{syn}} \), the overall magnitude of output current \( I_{\text{syn}} \) went up, and it was necessary to introduce different timing parameters at each test voltage to fully explain the voltage-dependent transmission behavior. As shown in Figure 2b, the evolution of \( \tau_d \) was more dramatic than that of \( \tau_t \), which is reflected in Figure 3 as the suppressed potentiation at \( V_{\text{syn}} = -8 \) or \(-10 \) V. This result also indicates that further optimization in synaptic voltages or structural engineering of nanoscale trapping media [23] may enable a switchable short-term and long-term neuromorphic behavior out of the same base architecture.
Electronics 2020, 9, 4

Figure 3. Comparing the experimental and model-reproduced STP (short-term plasticity) in organic synaptic transistors, with the magnitude of $V_{\text{syn}}$ being (a) $-4$ V, (b) $-6$ V, (c) $-8$ V, and (d) $-10$ V. The test measurements consisted of six steps, the frequencies of which are denoted in (a). The same test condition applies to all the other panels.

4. Conclusions

We have reported on a combined experimental and theoretical analysis of the voltage-dependent synaptic plasticity in flexible OFETs. An iterative model was used in conjunction with the correlative extraction to understand the STP characteristics at different voltages. It was found that the applied voltage has a significant impact on $I_0$, $\Delta E_F$, and timing constants. Among them, the $\tau_d$ experienced a particularly remarkable rise, turning the device into a practically depressing synapse at large voltages. At the same time, we have noticed the limited applicability of the model, evidenced by fitting errors. This indicates that an advanced model will need to be developed based on the physical characteristics of each complex trapping mechanism, which may for instance include the multiple time constants with a direct functional link to the materials and operational conditions.

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