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A Reconfigurable Analog Baseband Circuitry for LFMCW RADAR Receivers in 130-nm SiGe BiCMOS Process

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Abstract: A highly reconfigurable open-loop analog baseband circuitry with programmable gain, bandwidth and filter order are proposed for integrated linear frequency modulated continuous wave (LFMCW) radar receivers in this paper. This analog baseband chain allocates noise, gain and channel selection specifications to different stages, for the sake of noise and linearity tradeoffs, by introducing a multi-stage open-loop cascaded amplifier/filter topology. The topology includes a course gain tuning pre-amplifier, a folded Gilbert variable gain amplifier (VGA) with a symmetrical dB-linear voltage generator and a 10-bit R-2R DAC for fine gain tuning, a level shifter, a programmable G_m-C low pass filter, a DC offset cancellation circuit, two fixed gain amplifiers with bandwidth extension and a novel buffer amplifier with active peaking for testing purposes. The noise figure is reduced with the help of a low noise pre-amplifier stage, while the linearity is enhanced with a power-efficient buffer and a novel high linearity G_m-C filter. Specifically, the G_m-C filter improves its linearity specification with no increase in power consumption, thanks to an alteration of the trans-conductor/capacitor connection style, instead of pursuing high linearity but power-hungry class-AB trans-conductors. In addition, the logarithmic bandwidth tuning technique is adopted for capacitor array size minimization. The linear-in-dB and DAC gain control topology facilitates the analog baseband gain tuning accuracy and stability, which also provides an efficient access to digital baseband automatic gain control. The analog baseband chip is fabricated using 130-nm SiGe BiCMOS technology. With a power consumption of 5.9~8.8 mW, the implemented circuit achieves a tunable gain range of −30~27 dB (DAC linear gain step guaranteed), a programmable −3 dB bandwidth of 18/19/20/21/22/23/24/25 MHz, a filter order of 3/6 and a gain resolution of better than 0.07 dB.

Keywords: analog baseband; DAC; DCOC; G_m-C filter; LFMCW; linear-in-dB; PGA; SiGe BiCMOS

1. Introduction

The booming smart portable devices has led to an imperative demand for multi-standard compatibility on mobile/wireless receivers in recent years, such as Global System for Mobile Communications (GSM), Bluetooth, Global Position System (GPS), Wideband Code Division Multiple Access (W-CDMA), Wireless Local Area Network (WLAN), Long Term Evolution (LTE), and so on. Therefore, industrial corporations and academic institutions have released diverse integrated solutions with different RF front-ends covering various bands and sharing one analog baseband, which performs channel selectivity and gains tunability functions after down conversion mixers. In general, the analog baseband should be optimized for multi-purpose application scenarios with a fundamental tradeoff

between noise figure, linearity, power consumption, channel selection and gain/bandwidth/filter order programmability in itself. The fundamental principle, which prevents the analog baseband from obtaining universality, is that: the noise figure is determined by the preceding stages while the linearity is decided by the backward ones. The major challenges to be settled in the design of flexible analog circuits are the following: a. performance programmability; b. specification compatibility; c. energy scalability; d. complexity and cost.

In direct conversion receivers, typical analog baseband consists of a programmable gain amplifier (PGA) and a low-pass filter (LPF) as depicted in Figure 1. Thus, two general architectures emerge with their respective pros and cons: the LPF-first topology is more suitable for the receivers with high linearity/medium noise figure, while the PGA-first topology fits the receivers more with low noise figure/medium linearity. The authors of [1] proposed a fourth-order Chebyshev active-R-C LPF + PGA + fourth-order Chebyshev active-R-C LPF topology, which emphasized the filtering capability. The authors of [2] proposed a third-order LPF + PGA topology. The authors of [3] proposed a discrete time IIR LPF + active FIR topology, which focuses on the discrete time filtering function. The authors of [4–8] proposed a typical LPF + VGA topology, with tunable cut-off frequency/noise/gain performances. The authors of [9] proposed a fourth-order merged closed-loop analog baseband topology, which integrates the channel selection and gain programmability in one merged PGA/LPF biquad. However, the closed-loop topology is intrinsically power-hungry and frequency limited since the operational amplifier should exhibit gain bandwidth product (GBW) several times larger than closed-loop bandwidth requirement [10,11]. Therefore, there is no unique optimum solution, but a myriad solution with a variety proportional to the number of input specifications, with the expectation of sufficiently fine gain resolution, bandwidth programmability, excellent noise/linearity performance, acceptable chip footprint and low power consumption.

In this paper, a highly reconfigurable open-loop analog baseband prototype chip is proposed with optimized noise/linearity/power consumption performance, and digitally programmable bandwidth/gain/filter order for integrated linear FMCW radar receivers. Power consumption minimization is achieved via two methods: a. open-loop analog baseband chain with feasible compensations for process/voltage/temperature (PVT) variations; b. allocating channel selection/signal amplification specifications to every block across the baseband chain, and adjusting current consumed for diverse gain levels. The noise figure is maintained low with the help of a low noise figure/high gain pre-amplifier, while the linearity of the G_m-C LPF is guaranteed with a novel connection style without any rise in power consumption. Moreover, a novel high linearity buffer amplifier with active peaking is designed for testing purposes. The proposed prototype is fabricated in a 130 nm SiGe BiCMOS process, and the experimental results demonstrate the practicality of the proposal.

The rest of the paper is organized as follows. After the introduction given in Section 1, Section 2 derives the LFMCW radar requirement on the overall analog baseband chain, Section 3 illustrates the detailed implementation schematic, Section 4 demonstrates the experimental results and Section 5 concludes the paper.

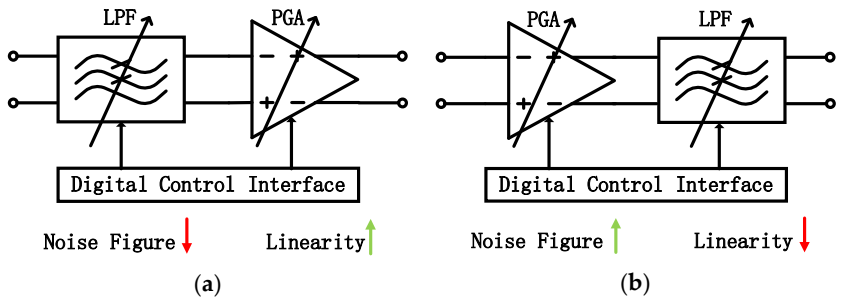

Figure 1. Typical architectures of analog baseband: (**a**) low-pass filter (LPF)-first topology; (**b**) programmable gain amplifier (PGA)-first topology.

2. Analog Baseband Architecture for LFMCW Radar

LFMCW radars are expansively used in automotive anti-collision, security check, imaging and presence detection applications when high range resolution is required in localization/tracking. A variety of modulation schemes are available, with a transmitted frequency signal acting as sine wave, sawtooth wave, triangular wave or square wave. In a sawtooth wave-based FMCW radar, the achievable range and velocity resolution depend on the transmitting signal bandwidth BW and the linear chirp period T_m, as seen in Figure 2. The range resolution Δr, which refers to the minimum detectable separation distance of two targets of equal cross sections that can be differentiated as distinct targets, is proportional to *c*/2/*BW*, where *c* is the velocity of light. This means that a large modulation bandwidth *BW* is needed for a fine range resolution. For a transceiver operating at 94 GHz, a modulation period in the order of 100 µs, a modulation bandwidth of higher than 500 MHz, the analog baseband bandwidth can be calculated as follows:

$$K = \frac{BW}{T_m} \tag{1}$$

$$f_{doppler} \approx \frac{2 \cdot v}{c} \cdot f_o \tag{2}$$

$$f_{IF,static} = \frac{2 \cdot K \cdot r}{c} \tag{3}$$

$$f_{IF,moving} = \frac{2 \cdot K \cdot r}{c} + f_{doppler} \tag{4}$$

where BW is the transmitting signal bandwidth, T_m is the linear chirp period, K is the FMCW slope, f_o is the center operating frequency, v is the target velocity, c is the velocity of light, r is the distance from source to target, $f_{IF,static}$ is the analog baseband frequency for static target ranging, and $f_{IF,moving}$ is the analog baseband frequency for moving target ranging. After setting BW = 500 MHz, T_m = 100 µs, $c = 3 \times 10^8$ m/s, r = 6~7 km into Equations (1)–(4), we can calculate the $f_{IF,static}$ to be 20~23.4 MHz. When doppler radar effect is taken into account, the IF frequency should cover the range of 18~25 MHz. Therefore, for generally used LPFs, the analog baseband −3 dB bandwidth is set to be 18/19/20/21/22/23/24/25 MHz, with 3-bit digital control words to cover the frequency shift coming from potential target moving.

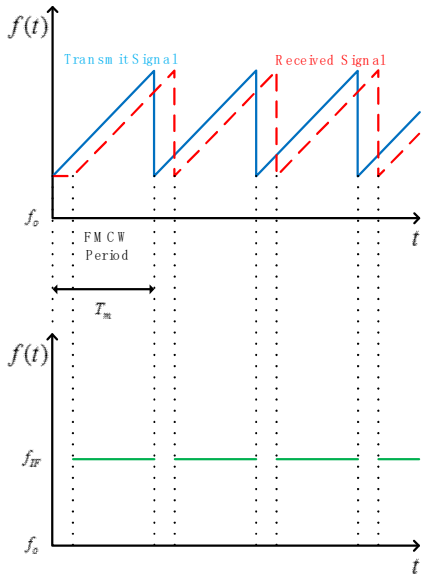

Figure 2. Linear frequency modulated continuous wave (LFMCW) signal analysis.

In this LFMCW radar, direct conversion architecture is adopted to evade image rejection problems and, thus, the analog baseband consumes lower power, since its bandwidth is half of that in low-IF/super heterodyne receivers. Paradoxically, typical dynamic range of direct conversion receiver is lower than that of low-IF/super heterodyne ones. Therefore, novel dynamic range optimization techniques are investigated in two directions: lower noise figure and higher linearity. Merged PGA/LPF biquads in [9] simultaneously optimized the two specifications owing to a closed-loop topology with switchable filter orders. However, this kind of topology becomes power-hungry when the frequency rises, and its gain resolution depends on the resistor/capacitor array size. In other words, the merged analog baseband compromises power consumption and chip size for noise/linearity/gain/filter order reconfigurability. What is more, the noise figure of PGA/LPF is normally higher than 25 dB, which deteriorates the receiver noise specification, since the front-end (including a low noise amplifier and a mixer) of the linear FMCW receiver usually possesses a gain of lower than 20 dB. Thus, architectures in Figure 1 and the merged analog baseband in [9] cannot satisfy the noise/linearity/power consumption requirement concurrently.

This paper makes a modification to the LPF-first/PGA-first topology by adding a programmable gain pre-amplifier with course gain tuning ability to its front, as depicted in Figure 3, which forms a PGA-LPF-PGA topology. In detail, this topology includes a pre-amplifier for noise optimization and course gain tuning, a folded Gilbert variable gain amplifier (VGA) with a symmetrical exponential voltage generator and a 10-bit R-2R DAC for fine gain tuning, a level shifter, a programmable G_m-C LPF, a DC offset cancellation (DCOC) circuit, two fixed gain amplifiers (FGA) with bandwidth extension and a novel buffer amplifier with active peaking for testing purposes. DC coupling is utilized on account of spectrally efficient modulation schemes [12]. The architecture in Figure 3 is open-loop and thus, frequency/power scalable. From the LPF-first viewpoint, this topology optimizes noise figure with another PGA ahead. From the PGA-first viewpoint, this topology ameliorates linearity with another PGA behind. Nonetheless, a heavy signal-processing burden is placed upon the LPF and its high linearity is a prerequisite.

In search of a high linearity LPF, researchers proposed numerous high linearity structures, such as active-R-C and class-AB G_m-C ones [6,13–16]. Linearity is refined with a compromise of power consumption and operation frequency, which is fundamentally determined by the closed-loop LPF topology and the complex routings inside the trans-conductor. Thus, high linearity open loop LPFs, which theoretically decouples the linearity from power consumption, are urgently needed.

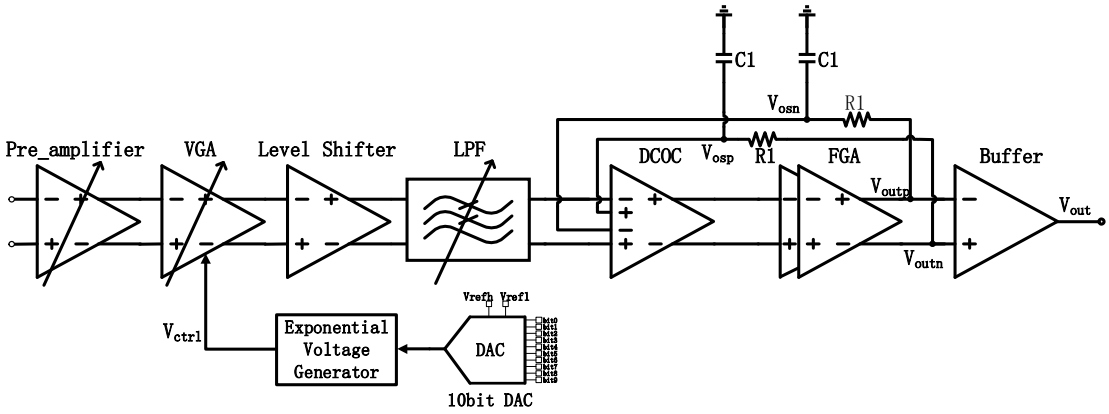

Figure 3. Analog baseband architecture.

3. Detailed Circuit Designs

In this section, detailed sub-block circuit schematics and their respective design procedures are presented.

3.1. Pre-Amplifier

As the first stage in the analog baseband chain, the pre-amplifier should exhibit low noise figure and simultaneously sufficient gain to suppress the noise contribution from the following stages to the overall analog baseband circuitry. Moreover, the gain programmability serves as a critical safeguard for large variations in input signal strength and a powerful certification of automatic gain control (AGC). Class-A/AB amplifiers are usually selected with common mode stability circuitry, with a high noise figure attributed to circuit complexities. Although the three fundamental gain programmability schemes, including current switching/bleeding, load resistor switching and source degeneration, are reported as depicted in Figure 4, their merits and demerits are evident: a. current switching method dynamically varies gain by correspondingly adjusting biasing current. High gain typically corresponds to high linearity/low noise figure/high dynamic range, while low gain is in accordance with low linearity/high noise figure/low dynamic range. Therefore, the dynamic range fluctuates over all gain settings; b. load resistor switching assumes a gain switching scheme with little noise figure variations, since the noise contribution from load resistors is restrained by amplifying the transistors. However, the load resistor switching has a detrimental effect on voltage swings and thus, the voltage swing varies with gain; c. the source degeneration scheme monitors the transconductance of main amplification transistors with a corresponding adjustment in noise figure and linearity. When the gain is high, a weak source degeneration is formed with a low noise figure and a medium linearity. When the gain is low, a strong source degeneration is constructed with a high linearity and a medium noise figure. Nevertheless, the current consumption is stable over all gain settings, which deteriorates the power dissipation self-adaptability. The advantages and disadvantages of them are listed in Table 1.

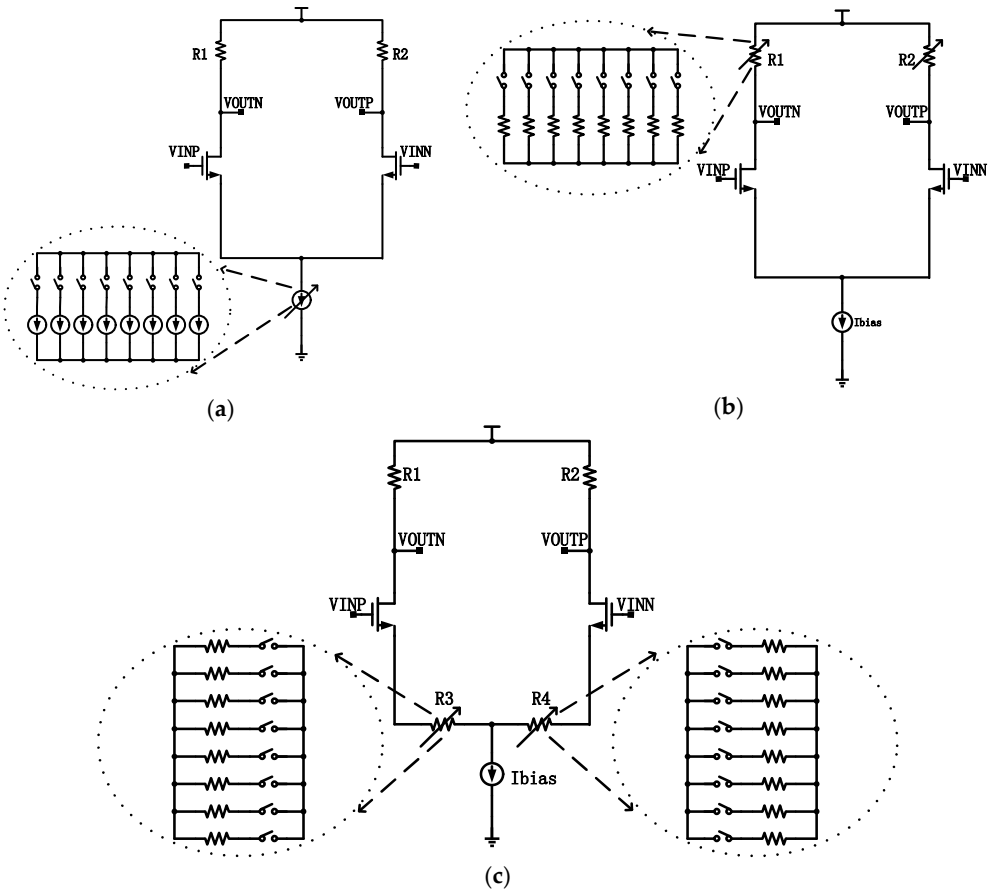

Figure 4. Typical architectures of analog baseband: (**a**) current switching topology; (**b**) load resistor switching topology; (**c**) source degeneration topology.

Forasmuch as the low noise and course gain tuning requirements, this paper utilizes a limiting amplifier structure with no common mode control [12] and adds 3-bit gain programmability with a switched resistor source degeneration technique, which is depicted in Figure 5. The common mode stabilization is left to following stages with noise figure optimization. Although the issue of stable current consumption still exists as one in source degeneration structure, the limiting amplifier structure avoids the common mode control circuitry, which is usually power-hungry. In short, the power consumption problem is partially circumvented. The component sizes and post-simulated specifications at TT 27° are given in Table 2.

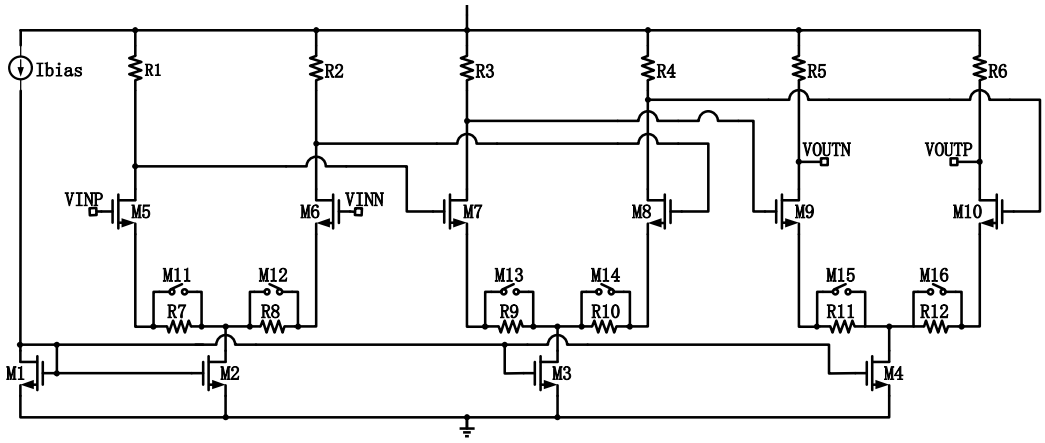

Figure 5. Pre-amplifier structure.

Table 1. Comparison of three gain programmability schemes.

Category	Merits	Demerits
Current switching	Current reconfigurability	Dynamic range varies across all gain settings
Load resistor switching	Noise figure relatively stable across all gain settings	Output voltage swing varies across all gain settings
Source degeneration	Dynamic range relatively stable across gain settings	Current stable across gain settings

Table 2. Component sizes and simulated performance specifications.

Transistors sizes W/L (μm/μm)	M1	20/2
	M2	20 × 5/2
	M3	20 × 5/2
	M4	20 × 5/2
	M5	5/0.13
	M6	5/0.13
	M7	5/0.13
	M8	5/0.13
	M9	5/0.13
	M10	5/0.13
	M11	0.2/0.13
	M12	0.2/0.13
	M13	0.2/0.13
	M14	0.2/0.13
	M15	0.2/0.13
	M16	0.2/0.13

Table 2. *Cont.*

Resistor value (Ohm)	R1	18 K
	R2	18 K
	R3	18 K
	R4	18 K
	R5	18 K
	R6	18 K
	R7	18 K
	R8	18 K
	R9	18 K
	R10	18 K
	R11	18 K
	R12	18 K
Gain & Bandwidth (dB/MHz)	Typical/Typical 27°	1/2/3/4/5/6/7/8 dB with 3-bit digital control & 40 MHz

3.2. VGA and Symmetrical Exponential Voltage Generator

Intrinsically, Gilbert structure can be regarded as a hybrid combination of current switching and load resistor switching since the current is simultaneously split between load resistors R_1/R_2 and tail currents I_{tail1}/I_{tail2} in Figure 6. Therefore, an optimization regarding the pros and cons of the two schemes can be conducted for the sake of dynamic range expansion. In essence, the Gilbert cell adjusts its gain via the current switching technique, but the difference between current switching and Gilbert cell lies in the current feeding through load resistors. In the Gilbert cell, the current through load resistors is stable across all gain settings, which circumvents dynamic range fluctuations encountered in current switching technique. Thus, the Gilbert structure is utilized for its wide gain tuning range and robustness, while a dB-linear voltage generator with an R-2R DAC is utilized for digital gain tuning precision. The variable gain amplifier cell with its control voltage generator is depicted in Figure 6. Moreover, dual supply voltages 1.2 V/1.8 V are adopted for power optimization. Specifically, 1.8 V feeds VGA, while 1.2 V feeds the voltage exponential generator.

In the VGA cell, assuming the transistors are working in strong saturation regions and square law model is adopted, the linear relationship between the input and output of VGA is expressed as follows:

$$\begin{aligned} V_{out} &= (g_{m1,2} - g_{m3,4}) \cdot R_{1,2} \cdot (V_{inp} - V_{inn}) \\ &= \sqrt{\frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2,3,4}}{2I_{tail}}} \cdot g_{m5,6} \cdot R_{1,2} \cdot 2 \cdot R_{3,4} \\ &\cdot I_{saturation} \cdot \exp\left(\frac{V_{ctrl}}{V_T}\right) \cdot (V_{inp} - V_{inn}) \end{aligned} \tag{5}$$

where μ_n is the low field mobility coefficient, C_{ox} is the unit area oxide capacitance and W/L is the aspect ratio of the transistors. The voltage gain is in a dB-linear relationship with the input voltage as expressed in Equation (5). The component sizes and post-simulated specifications at TT 27° are given in Table 3.

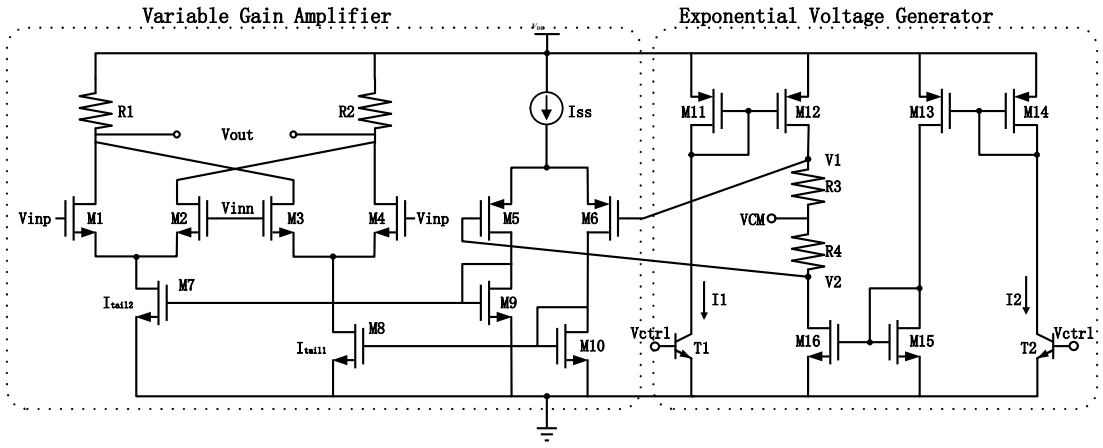

Figure 6. Variable gain amplifier (VGA) and dB-linear voltage generator schematic.

Table 3. Component sizes and simulated performance specifications.

Transistors sizes W/L (μm/μm)	M1	8/0.13
	M2	8/0.13
	M3	8/0.13
	M4	8/0.13
	M5	10/0.13
	M6	10/0.13
	M7	10 × 4/1
	M8	10 × 4/1
	M9	10/1
	M10	10/1
	M11	20 × 10/1
	M12	20 × 10/1
	M13	20 × 10/1
	M14	20 × 10/1
	M15	7 × 10/1
	M16	7 × 10/1
Resistor value (Ohm)	R1	2 K
	R2	2 K
	R3	60
	R4	60
Gain & Bandwidth (dB/MHz)	Typical/Typical 27°	−60~0 dB with analog continuous tuning & 100 MHz

3.3. DAC

R-2R DAC is employed to facilitate the digital control of the dB-linear voltage generator and to ensure fine gain resolution, with a single pole double throw (SPDT) based gain tuning scheme, switchable between analog continuous tuning and digital step tuning [8]. A 10-bit R-2R DAC with its output buffer is depicted in Figure 7. Two respective voltage ports named V_{refh} and V_{refl} refer to the high and low reference voltages, which are in accordance with Figure 3. The unit resistor value is selected to be 14.95 Kohms, with accuracy in mind.

In the design of a 10-bit DAC, component accuracy, symmetry of differential components and environmental consistency are three crucial points in layout floor planning. Thus, dummy cells near key components, shielded signal path optimization should be iterated several times. In addition, the output buffer should possess rail to rail output swing and acceptable drive capability. Therefore, the folded cascode topology depicted in Figure 7b is chosen with a linearization technique.

In the static simulation of the whole DAC, the full voltage range is 1.2 V, the INL is 0.17 LSB and the DNL is 0.34 LSB. In dynamic simulations, a sampling frequency of 1 MHz, with a sinusoidal input signal of 0.4961 MHz, is chosen and the effective number of bits (ENOB) is higher than 9.88 bits.

The component sizes and post-simulated specifications at TT 27° are given in Table 4.

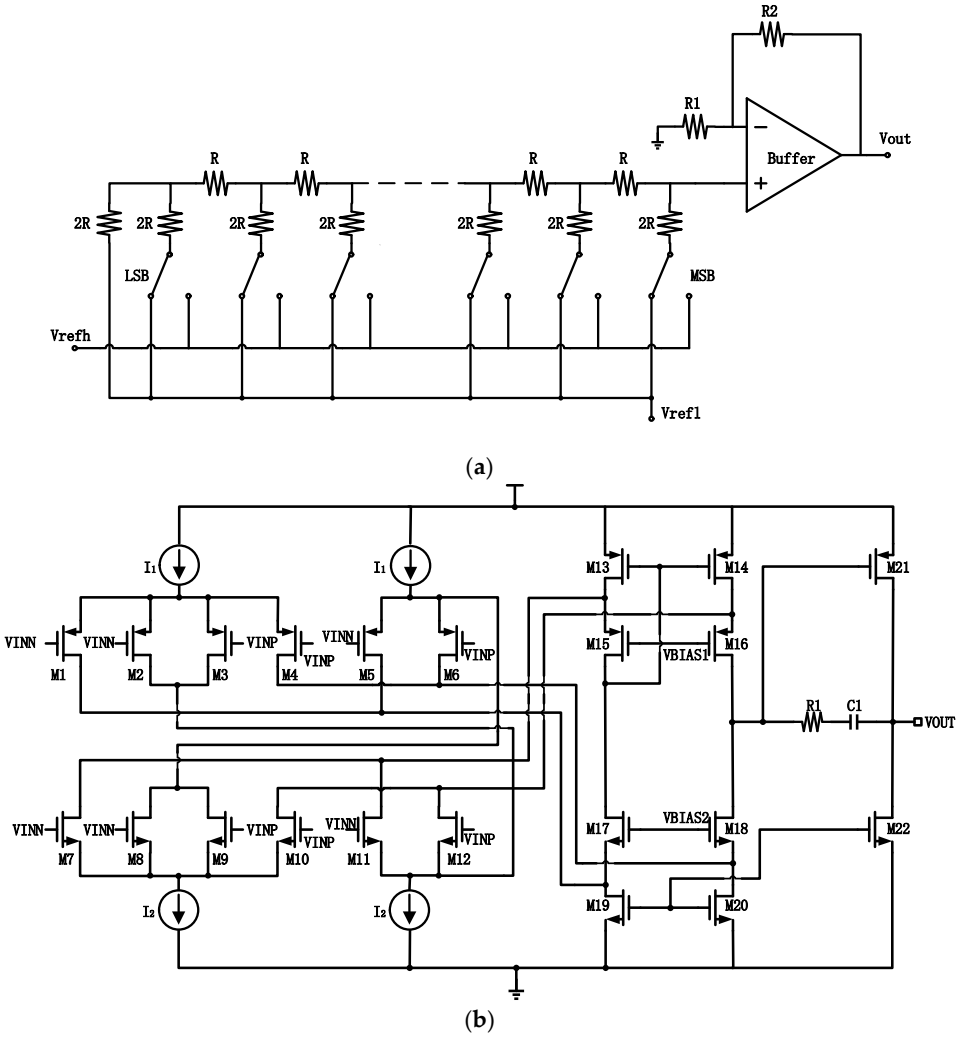

Figure 7. DAC schematic (**a**) DAC; (**b**) rail-to-rail buffer.

Table 4. Component sizes and simulated performance specifications.

Transistors sizes W/L (μm/μm)	M1	8.2/1
	M2	8.2/1
	M3	8.2/1
	M4	8.2/1
	M5	8.2/1
	M6	8.2/1
	M7	4/1
	M8	4/1
	M9	4/1
	M10	4/1
	M11	4/1
	M12	4/1
	M13	9/1
	M14	9/1
	M15	3/1
	M16	3/1
	M17	3/1
	M18	3/1
	M19	6/1
	M20	6/1
	M21	9 × 16/1
	M22	10 × 4/1

Table 4. *Cont.*

Resistor (Ohm)	R1	1 K
Capacitor (fF)	C1	600
Gain & Bandwidth (dB/MHz)	Typical/Typical 27°	Closed-loop 0 dB gain & 100 MHz

3.4. Level Shifter

In between VGA and LPF, a level shifter is inserted for the sake of common mode voltage stabilization, since its preceding pre-amplifier and VGA do not provide this kind of function. The level shifter is depicted in Figure 8, and a typical one-stage amplification with two-stage DC voltage feedback is used. R_2/C_1 performs the gain/phase margin compensation and snake resistors layout are utilized with large MOS-capacitors. The component sizes and post-simulated specifications at TT 27° are given in Table 5.

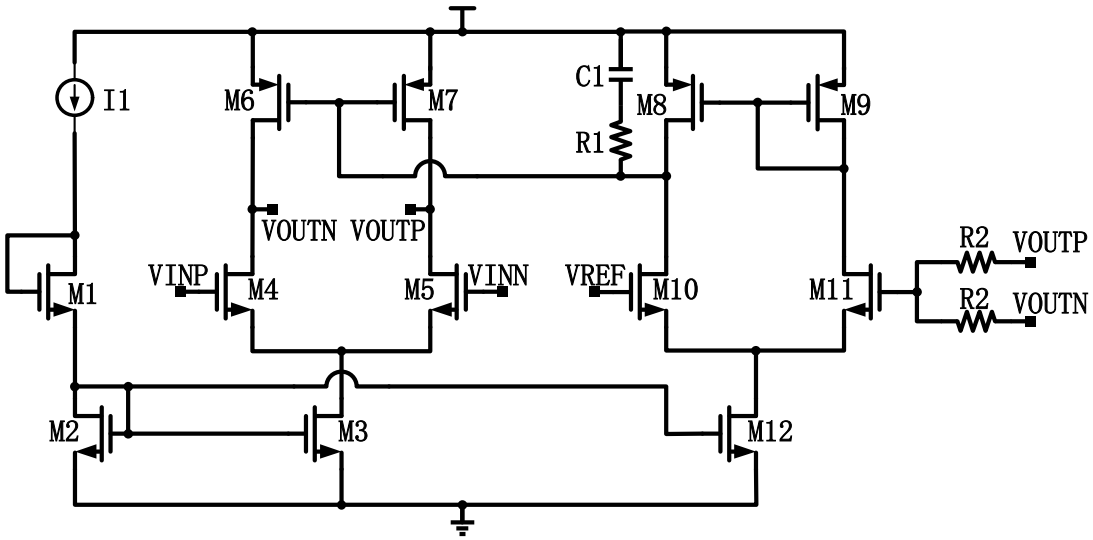

Figure 8. Level shifter.

Table 5. Component sizes and simulated performance specifications.

Transistors sizes W/L (μm/μm)	M1	22/0.13
	M2	10/2
	M3	10 × 8/2
	M4	0.3/0.13
	M5	0.3/0.13
	M6	10/1
	M7	10/1
	M8	10/1
	M9	10/1
	M10	22/0.13
	M11	22/0.13
	M12	10 × 8/2
Resistor (Ohm)	R1	1.85 K
	R2	22 K
Capacitor (fF)	C1	12,000
Gain & Bandwidth (dB/MHz)	Typical/Typical 27°	0 dB gain & 100 MHz

3.5. Programmable G_m-C LPF

G_m-C filters are well known for their open loop and frequency scalable characteristics. In theory, the G_m-C topology with simplicity, modularity and programmability would be the perfect choice for high frequency continuous-time filter designs. However, the mediocre linearity specification limits its potential use in analog baseband chain of direct conversion receivers. Therefore, linearity improvement techniques are pursued in two aspects: a. the transconductor cell [5–8]; b. the filter architecture. Most relevant work focuses on the former one with an emphasis on class AB transconductors. Nonetheless, class-AB transconductors are inherently power-hungry and possess a medium noise figure [10]. In addition, its common mode feedforward and feedback circuitry needs special care in common mode analysis, and its layout and routing are complex [6,13]. Moreover, previously reported linearity enhancement techniques in class-A transconductors are categorized into five groups: a. source degeneration; b. cross coupled transistors; c. load switching; d. current bleeding; e. local g_m-boosting feedback. None of them offers an architectural approach to promote linearity. This paper proposes a modified 3rd order Butterworth LPF with 3-bit logarithmic bandwidth tuning ability, as depicted in Figure 9.

Traditional third-order Butterworth LPF is depicted in Figure 9a, with a bandwidth tuning technique. From the bi-quad cascading viewpoint, an exchange of V_{2+} and V_{1-} is conducted as in Figure 9b. The voltage-current relationships of the two bi-quads are derived as follows.

$$\begin{aligned} I_{c,left} &= g_m{\cdot}(V_{1+} - V_{2+}) + g_m{\cdot}(V_{2-} - V_{1-}) \\ &= g_m{\cdot}(V_{1+} + V_{2-} - V_{1-} - V_{2+}) \end{aligned} \tag{6}$$

$$\begin{aligned} I_{c,right} &= g_m{\cdot}(V_{1+} - V_{1-}) + g_m{\cdot}(V_{2-} - V_{2+}) \\ &= g_m{\cdot}(V_{1+} + V_{2-} - V_{1-} - V_{2+}) \end{aligned} \tag{7}$$

Therefore, the output current remains the same for the two bi-quads. A quick glimpse of the right half of Figure 9b reveals that for a typical transconductor cell (G_m in Figure 9), the differential input signal swing is replaced by common mode input signal swing. Since the major nonlinearity is attributed to the transconductor itself, this change circumvents the differential signal processing vulnerability, with a new burden on common mode signal processing ability. On one hand, differential input signals experience the same voltage-to-current transformation in transconductor cells. Therefore, the frequency response remains the same after the modifications. On the other hand, common mode input signals experience different path, which results in larger variations in common mode signal swing. In short, the modification method essentially linearizes the LPF with an increase in common mode voltage variation, and a corresponding reduction in the differential mode voltage swing in the meantime. Therefore, the common mode rejection ratio and common mode feedback circuit should be designed iteratively with an emphasis on common mode stability. It should be cautious to use traditional sharing technique of common mode feedback circuit.

Afterwards, similar input exchange procedures are executed in Figure 9a and, thus, Figure 9c demonstrates the modified Gm-C LPF with its individual transconductor cell and switched capacitor array. Simulation results show that the output third-order interception point (OIP3) of a third-order Butterworth LPF is elevated from around 4.5 dBm to 14.5 dBm.

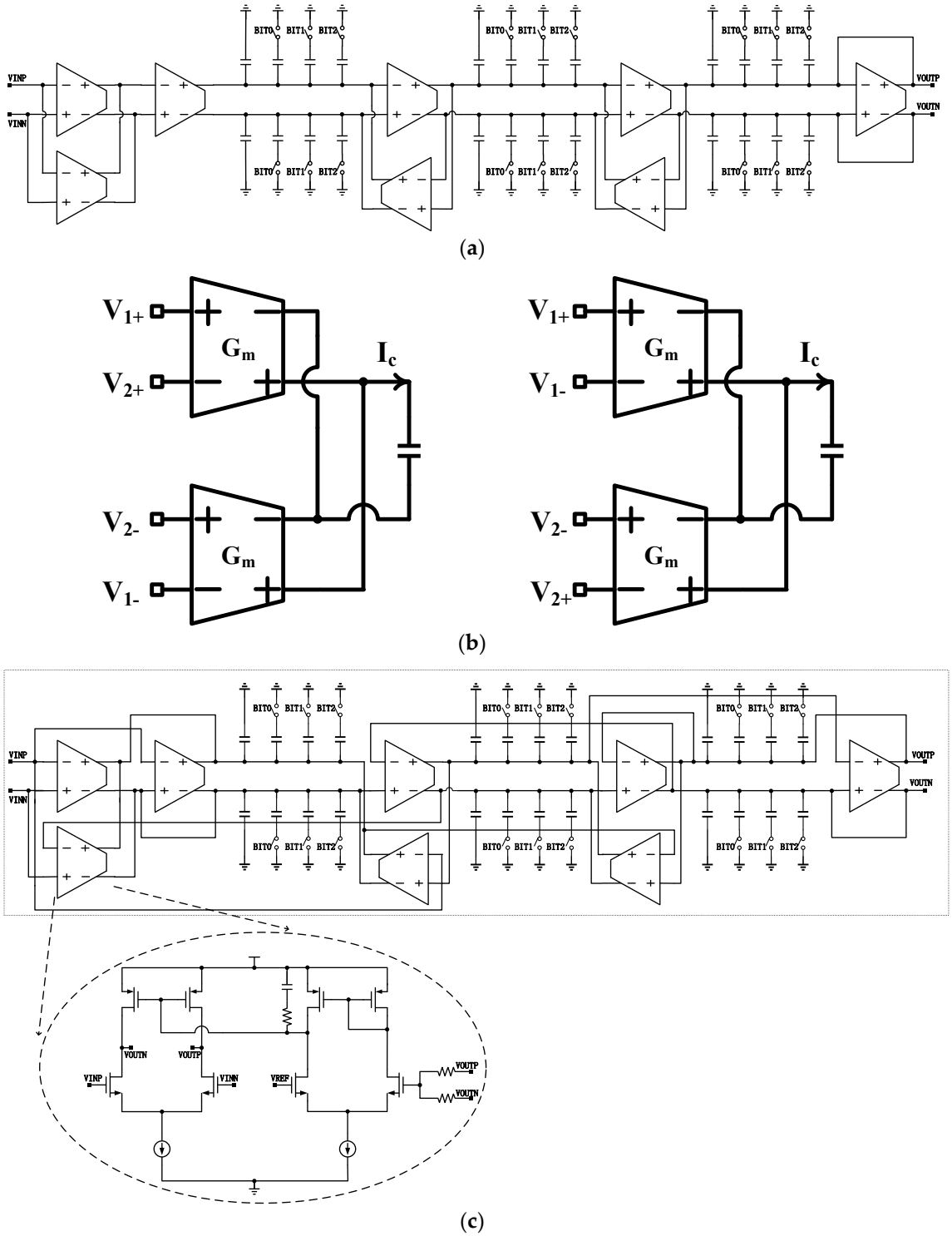

Figure 9. Traditional G_m-C low-pass filter (LPF) with its modification: (**a**) traditional G_m-C LPF; (**b**) modification method; (**c**) modified G_m-C LPF.

As to the bandwidth tuning aspect, typical binary capacitor array cannot set the bandwidth linearly when the operation frequency range covers several decades. For typical LPF, the −3 dB bandwidth is determined as follows.

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{8}$$

where f_o is the −3 dB cutoff frequency, L is the inductance value and C is the capacitance value. Thus, C is in a square root relation with f_o. For example, in order to achieve 2% step size in bandwidth over two decades of the frequency range, a 6-bit resolution in bandwidth programmability is required ($2^6 > 1/2\%$), while higher than 12-bit resolution is a prerequisite in capacitor array ($100^2/98^2$ requires another resolution of 6-bit for the lower than 0.025 capacitance resolution), which wastes the majority of the chip area. Therefore, the logarithmic bandwidth tuning technique is also adopted in the LPF design, as depicted in Figure 9c, since the logarithmic equation shrinks the capacitor array into small scale. The individual capacitor value can be calculated with a Taylor series expansion method, as follows:

$$\begin{aligned} C_{3bit,total} &= C_{unit}\cdot 2^{\frac{4b_2+2b_1+b_0}{2}} \\ &= C_{unit}\cdot[1+\log_{10}(2\cdot\tfrac{4\cdot b_2+2\cdot b_1+b_0}{2})+\tfrac{1}{2}\cdot(\log_{10}(2\cdot\tfrac{4\cdot b_2+2\cdot b_1+b_0}{2}))^2]+\cdots \\ &= C_{unit}\cdot[1+(\sqrt{2}-1)b_0+b_1+\sqrt{2}b_1b_0+3b_2+(3\sqrt{2}-3)b_2b_0+3b_2b_1+3\sqrt{2}b_2b_1b_0] \end{aligned} \quad (9)$$

where C_{unit} is the unit capacitor and $b_2/b_1/b_0$ are three digital control bits. This logarithmic tuning theoretically relaxes the passive array resolution by half. The post-simulated specifications of a third-order Butterworth LPF is listed in Table 6.

Table 6. Post simulated performance specifications of a third-order Butterworth LPF.

BW Tuning Range (MHz)	17/18/19/20/21/22/23/24
Noise figure (dB)	20.5
OIP3 (dBm)	14.5

3.6. DC Offset Cancellation (DCOC)

Unlike the typical DC stabilization circuitry used in level shifter and LPF, an f_T doubler based DC offset cancellation circuit is proposed for the sake of reduced parasitics, as depicted in Figure 10. The DC extraction LPF is given in Figure 3, which is composed of R_1 and C_1. C_1 is an area efficient MOS-capacitor. The −3 dB corner frequency of the LPF is around 100 kHz. The component sizes and post-simulated specifications at TT 27° are given in Table 7.

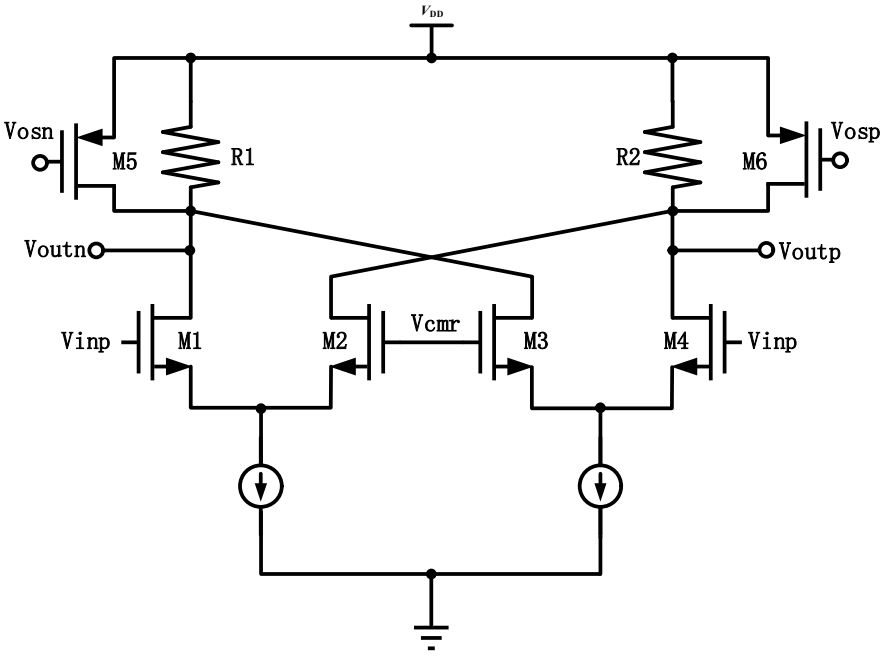

Figure 10. DC offset cancellation (DCOC) schematic.

Table 7. Component sizes and simulated performance specifications.

Transistors sizes W/L (μm/μm)	M1	2/0.13
	M2	2/0.13
	M3	2/0.13
	M4	2/0.13
	M5	2/2
	M6	2/2
Resistor (Ohm)	R1	1.85 K
	R2	22 K
Gain & Bandwidth (dB/MHz)	Typical/Typical 27°	0 dB gain & 100 MHz

3.7. Fixed Gain Amplifier (FGA)

Two FGAs are used to meet the gain compensation and stability requirement. Figure 11 illustrates one FGA with three gain stages with an active inductive peaking technique, which is formed by M7/M8. It should be pointed out that active peaking in itself affects frequency dependent group delay and, thus, data dependent jitter is worsened more or less. Therefore, group delay should be carefully verified in the FGA design. The component sizes and post-simulated specifications at TT 27° are given in Table 8.

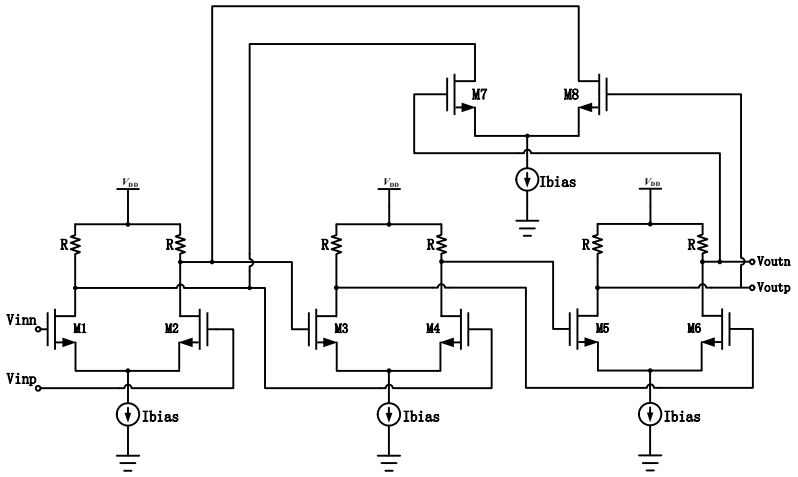

Figure 11. Fixed gain amplifier (FGA) schematic.

Table 8. Component sizes and simulated performance specifications.

Transistors sizes W/L (μm/μm)	M1	5/0.13
	M2	5/0.13
	M3	5/0.13
	M4	5/0.13
	M5	5/0.13
	M6	5/0.13
Resistor (Ohm)	R	16.5 K
Gain & Bandwidth (dB/MHz)	Typical/Typical 27°	20 dB gain & 100 MHz

3.8. Buffer Amplifier

A low power transconductance-linearized buffer with bandwidth extension technique is proposed, as depicted in Figure 12. An internal negative feedback is formed by M1/M3/M5/M6, and the output voltage can be expressed as follows.

$$\frac{V_{out}}{V_{in}} = \frac{g_{m3}\cdot(r_{o3} \parallel r_{o6}) + \frac{1}{2}\cdot g_{m3}\cdot R_1 - g_{m1}/g_{m5}}{1 + 1/(g_{m5}\cdot r_{o1} \parallel r_{o5}) - g_{m6}\cdot(r_{o3} \parallel r_{o6}) - \frac{1}{2}g_{m6}\cdot R_1} \tag{10}$$

If we assume the ideal output resistance is infinite and neglect parasitic capacitance of transistors, we can derive a simplified version of Equation (10), which intrinsically demonstrates a voltage buffer feature.

$$V_{out} = -\frac{g_{m3}}{g_{m6}} V_{in} \tag{11}$$

In summary, the presented buffer has triple fold advantages. Firstly, the transconductance linearization technique involves cross-coupling CMOS pairs. Secondly, the output load is lowered with the source follower topology and, hence, the bandwidth is broadened compared to common source based ones. Thirdly, the voltage headroom is $V_{gs,PMOS} + 2 \times V_{ds,NMOS}$, which suits low voltage buffer design well. The component sizes and post-simulated specifications at TT 27° are given in Table 9.

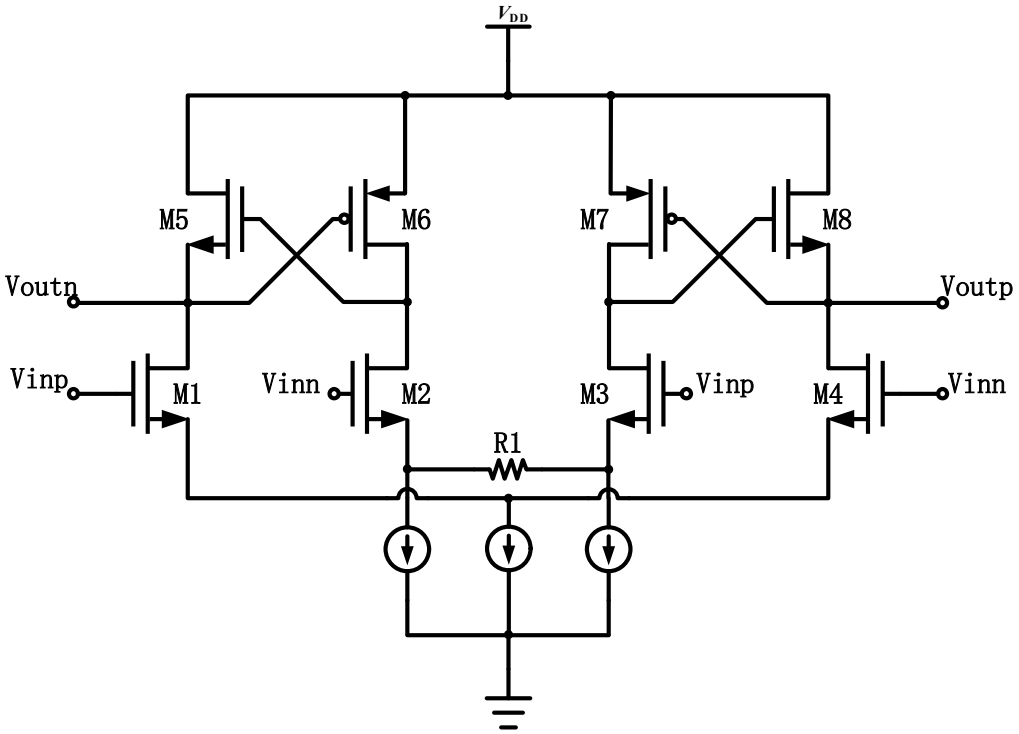

Figure 12. Buffer schematic.

Table 9. Component sizes and simulated performance specifications.

Transistors sizes W/L (μm/μm)	M1	0.3/0.13
	M2	14/0.13
	M3	14/0.13
	M4	0.3/0.13
	M5	40/0.13
	M6	3/0.13
	M7	3/0.13
	M8	40/0.13
Resistor (Ohm)	R1	71
Gain & Bandwidth (dB/MHz)	Typical/Typical 27°	0 dB gain & 100 MHz

4. Experimental Results

The proposed analog baseband is implemented in a 130 nm SiGe BiCMOS technology. The chip photograph is given in Figure 13 and its chip area is 1400 µm × 800 µm, with its core area of 1000 µm × 300 µm. The extra area occupied is used for on-chip measurement and on-chip decoupling capacitors. The voltage gain tuning range is −30~35 dB, when the DAC reference voltage V_{refh} and V_{refl} are set between 0.6 V and 0.95 V as depicted in Figure 14. However, when a dB-linear voltage gain curve is required, V_{refh} and V_{refl} should be set as 0.68 V and 0.9 V, which reduces the voltage gain range to −28~32 dB. The measured gain resolution is better than 0.1 dB, which is in accordance with the post-simulated DAC performance. The programmable cut-off frequency response is measured as depicted in Figure 15, when voltage gain is around −7 dB. The biasing current of trans-conductors is adjusted to match the LPF bandwidth requirement. Therefore, the −3 dB cutoff frequency via programmable capacitor array is listed as 17~24 MHz, with a 1 MHz step. The filter order is configured for different requirements in Figure 16 with orders of three and six. The chip adopted a dual power supply of 1.2 V/1.8 V for optimized power consumption. The power consumption is 2.9 mA@1.8 V and 0.3~2.5 mA@1.2 V, which is divided to sub-blocks as depicted in Figure 17. The measured OP1 dB is around −3 dBm when the input signal is at 20 MHz. A general comparison with related works is summarized in Table 10. The proposed analog baseband exhibits comparable specifications with previous works, while the voltage gain resolution is far better, thanks to the DAC and exponential voltage generator. In future research, the minimum bit of the LPF will be modified to obtain more desirable results.

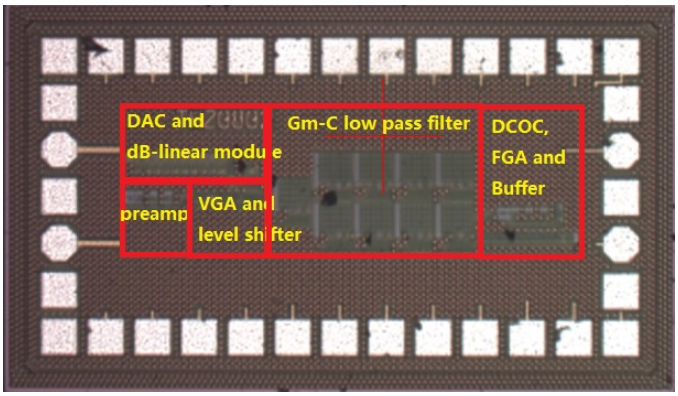

Figure 13. Chip microphotograph.

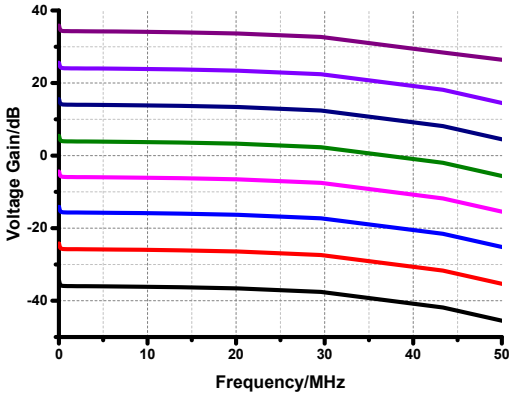

Figure 14. Measured voltage gain tuning response of the proposed chip with LPF bypassed (PGA + buffer).

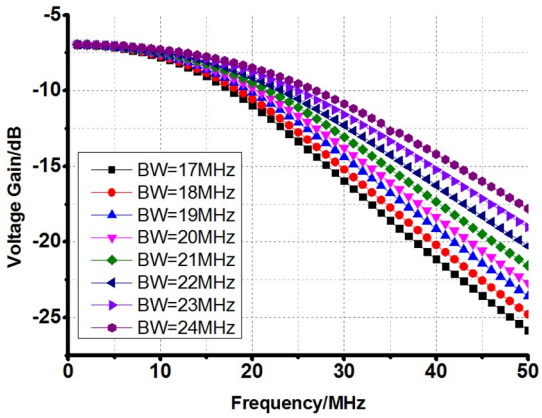

Figure 15. Measured frequency tuning response of the LPF (1 stage third-order LPF).

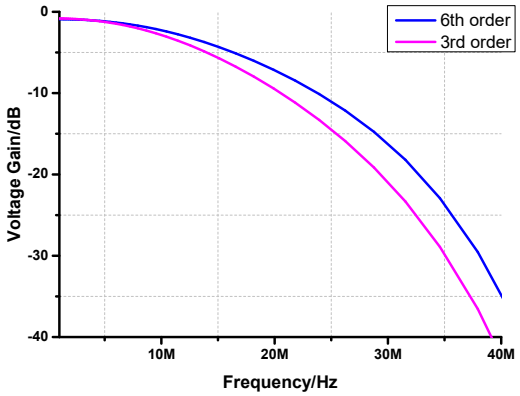

Figure 16. Measured frequency tuning response with filter order programmability (LPF order varies from third-order to sixth-order).

Table 10. Performance Comparison.

Specification	[5]	[10]	[11]	[12]	This Work
Technology	65-nm CMOS	65-nm CMOS	90-nm CMOS	65-nm CMOS	130-nm BiCMOS
Power (mW)	1.72~9.6	10.78	3	11.5	5.9~8.8
Power/pole (mW)	N/A [d]	1.08	0.75	1.92	0.93~1.37
Structure	Active-R-C	Active-R-C	G_m-C	Active-R-C	G_m-C
Filter order	2/4/6/8	5	2	3	3/6
Area (mm^2)	0.8	2.03	1.1	0.45	0.3/1.12 [a]
Gain range (dB)	0~72	−24~69	0~71	−18~67	−30~35
Gain resolution (dB)	N/A	0.5	1	N/A	0.1
BW (MHz)	0.2~20	0.09~14.2	0.3~30	0.7~5.2	0.01~18/24.7
Noise Figure (dB)	N/A [b]	18.35	18	21.24	16.2 [c]
LPF OIP3 (dBm)	17.8	22.43	−8.7	24	14.5

[a] Core area is 0.3 mm^2 and total chip area is 1.12 mm^2; [b] The author did not give the port impedance levels; [c] The noise figure is post-simulated at maximum gain; [d] The filter order is programmable and thus this parameter varies across filter order settings.

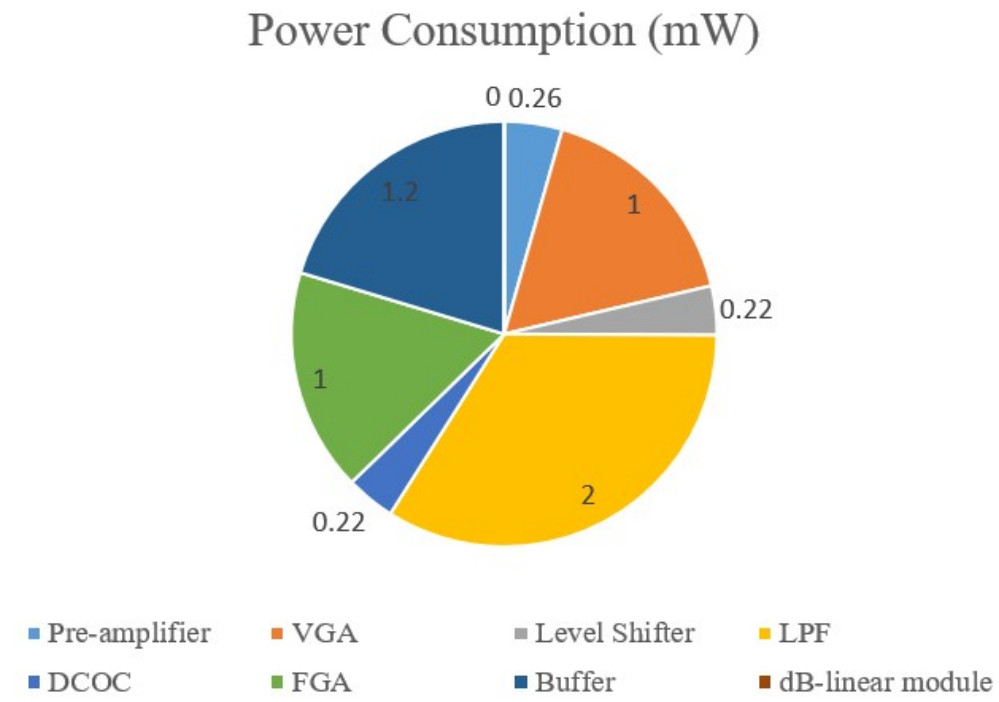

Figure 17. Power consumption pie chart. (dB-linear module working in lowest power consumption mode).

5. Conclusions

This paper proposed a reconfigurable analog baseband circuitry for LFMCW RADAR receivers with bandwidth/gain/filter order programmability. Measurement results are acceptable and match the simulations well. Although the majority of performance specifications are acceptable with respect to recent references, there is still no clear distinction between the closed loop analog baseband and an open loop one in the facet of power consumption. However, when operating frequency rises, closed loop architecture will soon evaporate, owing to the upper limit of GBW and power consumption. In future research, the reconfigurable analog baseband should be updated with a bandpass filter or complex filter, in order to reduce the in-band integrated noise for better receiver detection specification.

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