A Novel Switched-Capacitor Multilevel Inverter Topology for Energy Storage and Smart Grid Applications

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Abstract: The recent advancement in the application of the internet of things in the smart grid has led to an industrial revolution in the power industry. The Industry 4.0 revolution has already set in, allowing computers to interact for an efficient and intelligent approach in solving smart grid issues. Multilevel inverters (MLIs) are an integral part of the smart grid system for integrating the distributed generation sources and storage energy systems into the smart grid. It attracted attention in industrial applications as they can handle high power and high voltage with an inherent feature of superior output voltage waveform quality. Moreover, its variant, the switched-capacitor MLI (SCMLI), has the added benefit of lesser DC supply requirement. In this paper, a switched-capacitor multilevel inverter topology has been proposed, which can operate in symmetric and asymmetric mode. The proposed SCMLI generate thirteen and thirty-one level output voltages for symmetric and asymmetric selection of DC voltage sources, respectively. The proposed SCMLI has a smaller number of switching devices for a given output voltage level as compared to other recently proposed topologies. A thorough comparison is presented with the recently proposed topologies on several parameters, including cost function. To validate the proposed topology, symmetric and asymmetric cases were simulated using Matlab® 2018a and the results were verified using an experimental hardware setup.

Keywords: energy storage systems; multilevel inverter; switched-capacitor; total harmonic distortion; nearest level control

1. Introduction

The increasing cost of limited fossil fuel resources has led to a massive investment of economic and human resources to develop its substitute in the form of a cheaper and cleaner energy resource. Recently, researchers and industries have seriously looked upon solar and wind energy resources to meet future energy demand. The negligible environmental effects and economic benefits are the advantages associated with using these sources. Due to the advancements in power electronics
technology, highly efficient converters have been developed for energy conversion applications. The AC drives and grid applications require power inverters. While a conventional two-level inverter has been used in industrial use, it has some serious shortcomings in power quality [1]. As a result, there is a competition in the market to develop more efficient high-voltage and high-current handling inverters with superior power quality to meet the guidelines of IEEE 1547 standards of the smart grid system. The smart grid can be described as a powerful grid connecting the consumers with applications and integrating the distributed power generation system into an optimized centralized power system [2]. Physical attacks, cyber-attacks, or natural disasters are significant threats to smart grid deployment, which can even lead to blackouts, privacy breaches, infrastructural failures, operating personnel safety issues, or energy theft [3]. Multilevel inverters (MLIs) garnered a lot of concern owing to their output waveforms of high-quality along with low $\frac{dv}{dt}$ stress. Low total harmonic distortion (THD) of the output waveform is obtained by increasing the number of output voltage levels of the inverters, which results in the reduction of the size of output filters. MLIs have several DC voltage supplies, capacitors, power diodes, and switches along with driver circuits to obtain proper output voltage using a suitable switching pattern [1,4–8].

Flying-capacitor, diode-clamped, and cascaded MLIs are topologies that are conventional as well as well-recognized. But there are certain shortcomings of these conventional inverters. The limitations of flying capacitor and diode-clamped MLIs are that they have a high number of capacitors and diodes for a higher-level generation, while cascaded H-bridge inverters have many isolated DC supplies and a large number of power switches for high-power applications. Additionally, external circuits are a basic necessity for maintaining the capacitor voltage [9–12].

Consequently, newer MLI topologies that offer to overcome the shortcomings of these traditional MLIs were reported in the literature. MLIs using symmetrical DC supply to obtain multilevel staircase sinusoidal voltage waveforms were presented in [13–17]. The converters mentioned above posed a combined setup of power semiconductor devices and the supply of voltage. A step-up sinusoidal output voltage may be obtained by the use of an applicable switching pattern. It was evident from the outcomes that MLI’s performance improved as we increased the voltage level tally, but it led to more circuit components and complexity in control [18–20]. MLIs with asymmetrical DC voltage supply, where the number of levels was increased manifold with fewer circuit elements, were reported in [21–23]. However, the use of isolated DC supply was still a drawback here, leading to a cost increment.

Switched-capacitor MLIs (SCMLIs) came into the picture for a reduction in the estimate of separated DC voltage supply [24]. A lot of work was reported in the area of SCMLI. Researchers are coming with different switched-capsulator MLI topologies with self-balancing forms and self-voltage boosting capabilities, as was reported in [4,25–28]. SCMLI application areas include high-frequency AC (HFAC) system of distribution of power [29,30], HFAC microgrids [31], X-rays, UPS, LASERs, etc. In [32], SCMLI, with a cascaded structure having a boost converter (SC-based) connected with a two-level inverter, was proposed. The boost converter generated the multilevel step voltage, and the inverter was used to generate polarity. As in [32], authors of [33] proposed a novel SCMLI having an Switched Capacitor-frontend and H-bridge backend where the SC-frontend was used to increase output levels by converting series and parallel connections. In [34], a step-up multilevel converter topology was proposed for both asymmetric as well as symmetric types of DC supplies of voltage. Its main feature was the inherent voltage balancing capability of its capacitors. A new design of converter of switched-capacitor type was proposed in [35], where the authors used only one DC voltage supply. As a result, the total standing voltage (TSV) and maximum switch-stress voltage were reduced. Both symmetric and asymmetric topologies were presented in [36] with a reduced number of switch counts. A converter (DC to AC) with an ability to increase voltage along with voltage self-balancing was shown in [37]. Peak inverse voltage (PIV) and TSV were lower as it had one DC supply and no H-bridge. Most of the above topologies suffered from capacitor self-voltage balancing problems or high-voltage stress on switches.
This study proposes a topology for single-phase switched-capacitor multilevel inverter (SCMLI) with some novel characteristics, which operates in both symmetrical and asymmetrical configuration types to generate a 13- and 31-level output, respectively. The study aims to reduce switch count, low total standing voltage, and low individual voltage stress of the circuit components for higher output levels and capacitor self-voltage balancing capability. The only issue is its slightly higher THD due to capacitor charging and discharging. The paper is structured in the following manner. The proposed topology for symmetric and asymmetric configuration with its working is given in Section 2. Section 3 explains the modulation technique used here, i.e., nearest level control. A comparative analysis of SCMLI proposed here with other topologies presented recently is mentioned in Section 4. Power loss analysis with efficiency calculation using PLECS software is given in Section 5. Experimental and simulation results for the proposed topology is given in Section 6. Finally, the concluding remarks are mentioned in Section 7.

2. Proposed Topology

The description of the proposed SCMLI topology is shown in Figure 1. The circuit had eight switches (T₁–T₈) of unidirectional nature, three DC voltage sources, two switches (S₁ and S₂) that are bidirectional, and four capacitors. The switch pairs T₃–T₄ and T₅–T₆ were complementary, thus avoiding short-circuiting problems in the DC voltage supply. Similar topology works for asymmetrical and symmetrical configuration based on the intensity of V₁, V₂, and V₃, DC voltage supplies.

![Figure 1. Proposed switched-capacitor multilevel inverter (SCMLI) topology.](image)

2.1. Symmetrical Configuration

For this configuration, all the sources (V₁, V₂, and V₃) of DC voltage have the same magnitude, i.e., V₁ = V₂ = V₃ = Vdc. Therefore, the proposed topology with symmetric configuration can generate 13 levels at the output (six positives, six negative, and zero). All the switching states of this configuration are shown in Table 1. The switching diagrams for all the thirteen switching states are shown in Figure 2. In the switching description, the undotted line indicates the active circuit having current flow. The voltage across C₁ and C₂ will be half of the voltage V₁, and voltage across C₃ and C₄ will be half of the voltage V₃. Total standing voltage (TSV) is a parameter that was essential for inverter configuration selection. It is the sum of the absolute maximum blocking voltages through each switch. Also, there will be the same voltage stress for complementary switches. Therefore, according to the basic circuit given in Figure 1, voltage stresses across the switches:

Switches, T₁ and T₂,

\[ V_{S1} = V_{S2} = V_1 = V_{dc} \]  \hspace{1cm} (1)

Complementary switches, T₃ and T₄,

\[ V_{S3} = V_{S4} = V_1 + V_2 = 2V_{dc} \]  \hspace{1cm} (2)
Table 1. Switching states for the symmetrical configuration.

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Complementary switches, $T_5$ and $T_6$,

$$V_{S5} = V_{S6} = V_2 + V_3 = 2V_{dc}$$

(3)

Switches,

$$V_{S7} = V_{S8} = V_3 = V_{dc}$$

(4)

For bidirectional switches, each unidirectional switch of $S_1$ and $S_2$ had to block the voltage of both switches of bidirectional switch $S_1$,

$$V_{S1'} = V_1 = V_{dc}$$

(5)

Both switches of bidirectional switch $S_2$,

$$V_{S2'} = V_3 = V_{dc}$$

(6)

Therefore,

$$TSV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} + V_{S7} + V_{S8} + 2V_{S1'} + 2V_{S2'}$$

(7)

(2 is for the 2 bidirectional switches $S_1$ and $S_2$).

Using Equations (1) to (6) in Equation (7), we have

$$TSV = 2(V_{S1} + V_{S3} + V_{S5} + V_{S7} + V_{S1'} + V_{S2'})$$

$$= 2(V_{dc} + 2V_{dc} + 2V_{dc} + V_{dc} + V_{dc} + V_{dc})$$

$$= 16V_{dc}$$

(8)

For per unit $TSV$, the $TSV$ is divided by the peak of the output voltage. Therefore,

$$TSV_{p.u} = \frac{16V_{dc}}{6V_{dc}} = 2.67$$

(9)
Figure 2. All the thirteen switching states of the symmetrical configuration.
2.2. Asymmetrical Configuration

The same topology can generate more output levels using asymmetrical configuration. However, determining the appropriate ratio of the voltage sources to have maximum output levels was essential for lowering down the THD. After analyzing the combinations for the three DC voltage sources, the one with $V_1 = 12 \ V_{dc}$, $V_2 = V_{dc}$, and $V_3 = 2 \ V_{dc}$ gave the highest number of output levels. Thirty-one output levels can be obtained using this combination of supply of DC voltage for the same topology. Table 2 shows distinct states of switching for the configuration. The switching diagrams for some of the 31 switching states are shown in Figure 3. Voltage stresses across the switches:

$$V_{S1} = V_{S2} = V_1 = 12 \ V_{dc}$$

$$V_{S1} = V_{S2} = V_1 = 12 \ V_{dc}$$

$$V_{S5} = V_{S6} = V_2 + V_3 = 3 \ V_{dc}$$

$$V_{S7} = V_{S8} = V_3 = 2 \ V_{dc}$$

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<td>OFF</td>
<td>$-11V_{dc}$</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>$-12V_{dc}$</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>$-13V_{dc}$</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>$-14V_{dc}$</td>
</tr>
</tbody>
</table>

For bidirectional switches, each unidirectional switch of $S_1$ has to block the voltage of

$$V_{S1f} = V_1 = 12V_{dc}$$
and, each unidirectional switch of \( S_2 \) has to block the voltage of

\[
V'_{S2} = V_3 = 2V_{dc}
\]  

(15)

Therefore,

\[
TSV = 2(V_{S1} + V_{S3} + V_{S5} + V_{S7} + V_{S1'} + V_{S2'})
\]  

(16)

Using Equations (10) to (15) in Equation (16), we have

\[
TSV = 2(12V_{dc} + 13V_{dc} + 3V_{dc} + 2V_{dc} + 12V_{dc} + 2V_{dc}) = 88V_{dc}
\]  

(17)

For per unit TSV,

\[
TSV_{p,u} = \frac{88V_{dc}}{15V_{dc}} = 5.87
\]  

(18)

3. Nearest Level Control

Modulation techniques are of great importance for multilevel inverters as they influence harmonics, control dynamics, switching loss, filter size, etc. [38]. Traditional modulation methods have the standard features of high switching loss, switching harmonics, increased switching frequency, and high complexity as submodules increases, etc. Nearest level control (NLC) has the advantage of having more voltage levels as it approximates the reference voltage with the nearest voltage level, which results in fundamental switching frequency having low switching losses [39]. This method was useful for higher output voltage applications as the switching losses and low-order harmonics were minimized. This method can operate at 50 Hz and is extendable to N-Levels. This method was more straightforward, and the round-off method was used for the calculation of normalized value. The amplified signal was obtained by multiplying the reference signal by \( A \), as given in Figure 4b. After comparing the signals obtained with constants, the pulses thus obtained were combined according to logic for switching to get the required pulses of switching. NLC was applied for controlling the voltage at the output of
the proposed multilevel inverter for both symmetric and asymmetric configurations. The working principle of the NLC is mentioned as part of Figure 4a,b. There was a variation in the reference voltage (Vref) to change the modulation index (MI), which is given as:

$$\text{Modulation Index} = \frac{V_{\text{ref}}}{V_{\text{out}}} = \frac{2V_{\text{ref}}}{(N - 1)V_{\text{dc}}}$$

(19)

![Figure 4](image)

(a) Nearest level control (NLC): (a) NLC having sampled reference voltage, (b) workings of NLC.

4. Comparative Analysis

In this section, the SCMLI proposed is compared with the formerly presented SCMLIs. A thorough comparison was carried out considering TSVp.u; the number of components required; cost function (CF), which is taken from [7]; etc. Estimation of the overall cost of each topology was done using the ratio of cost function over the output voltage levels.

$$CF = \left( N_{\text{sw}} + N_{\text{dr}} + N_{\text{cap}} + N_{\text{di}} + \gamma \ TS V_{p.u} \right) \times N_{V_{dc}}$$

(20)

where, $N_{\text{sw}}$ represents the switch count, $N_{\text{dr}}$ represents gate drivers’ count, $N_{\text{cap}}$ represents the number of capacitors, $N_{\text{di}}$ represents the diode count, $N_{V_{dc}}$ represents the number of dc voltage sources, $\gamma$ represents weight coefficient, $TS V_{p.u}$ represents total standing voltage.

Different components required, such as gate drivers, switches, capacitors, diodes, and isolated sources of DC voltage and total standing voltage per unit, were suitably considered for the estimation of the cost function. For selecting proper switches for any topology, the TSV of the structure will be necessary. A weight coefficient ($\gamma$) was multiplied with $TS V_{p.u}$ to precisely apply its impact on the proposed CF. $\gamma$ greater than or less than one selects which among TSV and the number of switches was the most relevant quantity. The comparative analysis is done in the following two sections.

4.1. Comparison with a Single Source and Symmetric Topologies

Here, the general features of the proposed 13-level symmetric topology are compared with some recent topologies of SCMLIs and are summarized in Table 3. One of the notable merits of the proposed structure was its lowest $TS V_{p.u}$ among the papers presented in [7,33–37,40–42]. It also had the lowest number of switch count among its 13-level counterparts. Value of $\frac{CF}{N_{level}}$ was also low for both conditions of $\gamma = 0.5$ and $\gamma = 1.5$ for 13 levels. Value of $\frac{CF}{N_{level}}$ was very high in [33,36] as compared to the proposed topology. Structures in [7,40] had a lower value of $\frac{CF}{N_{level}}$ than the proposed one as they have a single DC source, and their TSV was higher.
Table 3. Comparison of the proposed symmetric topology with different single source and symmetric topologies of similar voltage levels.

<table>
<thead>
<tr>
<th>SCMLI Presented in</th>
<th>$N_{\text{level}}$</th>
<th>$N_{\text{sw}}$</th>
<th>$N_{\text{Vdc}}$</th>
<th>$N_{\text{dr}}$</th>
<th>$N_{\text{cap}}$</th>
<th>$N_{\text{di}}$</th>
<th>$C_{\text{F}}$</th>
<th>$T_{\text{SV}}$</th>
<th>$P_{\text{pu}}$</th>
<th>$\gamma = 0.5$</th>
<th>$\gamma = 1.5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7] sym</td>
<td>9</td>
<td>10</td>
<td>1</td>
<td>8</td>
<td>2</td>
<td>1</td>
<td>6.00</td>
<td>2.70</td>
<td>3.33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[7] asym</td>
<td>17</td>
<td>18</td>
<td>2</td>
<td>14</td>
<td>4</td>
<td>2</td>
<td>6.00</td>
<td>4.82</td>
<td>5.52</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[33]</td>
<td>13</td>
<td>18</td>
<td>3</td>
<td>18</td>
<td>3</td>
<td>3</td>
<td>5.00</td>
<td>10.27</td>
<td>11.42</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[34]</td>
<td>13</td>
<td>14</td>
<td>2</td>
<td>14</td>
<td>4</td>
<td>4</td>
<td>5.30</td>
<td>5.95</td>
<td>6.76</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[35]</td>
<td>13</td>
<td>16</td>
<td>2</td>
<td>16</td>
<td>4</td>
<td>2</td>
<td>5.60</td>
<td>6.27</td>
<td>7.13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[36]</td>
<td>13</td>
<td>14</td>
<td>6</td>
<td>14</td>
<td>0</td>
<td>0</td>
<td>4.70</td>
<td>13.11</td>
<td>16.20</td>
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<td></td>
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<tr>
<td>[37]</td>
<td>13</td>
<td>29</td>
<td>1</td>
<td>29</td>
<td>5</td>
<td>0</td>
<td>4.83</td>
<td>5.03</td>
<td>5.40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[40]</td>
<td>9</td>
<td>8</td>
<td>1</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>4.00</td>
<td>2.90</td>
<td>3.33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[41]</td>
<td>17</td>
<td>14</td>
<td>4</td>
<td>14</td>
<td>4</td>
<td>8</td>
<td>4.25</td>
<td>9.91</td>
<td>10.91</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[42]</td>
<td>17</td>
<td>10</td>
<td>2</td>
<td>10</td>
<td>2</td>
<td>4</td>
<td>5.50</td>
<td>3.38</td>
<td>4.03</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Proposed multilevel inverters (MLI) 13 12 3 10 4 0 2.17 6.08 6.75

4.2. Comparison with a Symmetric Topologies

Asymmetric topologies have come into the picture for obtaining output levels in higher numbers. The proposed asymmetric topology was compared with recent SCMLIs of similar voltage levels comprehensively, which is shown in Table 4. For higher levels (here 31), this topology did not have a marked difference in the different properties given in the table. The value of $C_{\text{F}}$ in the proposed MLI was less than the structures presented in [23,43]. The number of drivers and switch count used here was lowest. Most importantly, the same topology was used for symmetric as well as asymmetric design in the topology proposed.

Table 4. Comparison of the proposed asymmetric topology with asymmetric topologies of similar voltage levels.

<table>
<thead>
<tr>
<th>SCMLI Presented in</th>
<th>$N_{\text{level}}$</th>
<th>$N_{\text{sw}}$</th>
<th>$N_{\text{Vdc}}$</th>
<th>$N_{\text{dr}}$</th>
<th>$N_{\text{cap}}$</th>
<th>$N_{\text{di}}$</th>
<th>$T_{\text{SV}}$</th>
<th>$P_{\text{pu}}$</th>
<th>$\gamma = 0.5$</th>
<th>$\gamma = 1.5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[34]</td>
<td>31</td>
<td>14</td>
<td>2</td>
<td>14</td>
<td>4</td>
<td>4</td>
<td>5.33</td>
<td>2.49</td>
<td>2.83</td>
<td></td>
</tr>
<tr>
<td>[35]</td>
<td>31</td>
<td>16</td>
<td>2</td>
<td>16</td>
<td>4</td>
<td>2</td>
<td>5.67</td>
<td>2.63</td>
<td>3.00</td>
<td></td>
</tr>
<tr>
<td>[42]</td>
<td>25</td>
<td>12</td>
<td>2</td>
<td>12</td>
<td>2</td>
<td>2</td>
<td>5.00</td>
<td>2.44</td>
<td>2.84</td>
<td></td>
</tr>
<tr>
<td>[43]</td>
<td>31</td>
<td>14</td>
<td>6</td>
<td>10</td>
<td>0</td>
<td>0</td>
<td>5.33</td>
<td>5.16</td>
<td>6.19</td>
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<tr>
<td>[23]</td>
<td>25</td>
<td>12</td>
<td>4</td>
<td>10</td>
<td>0</td>
<td>0</td>
<td>5.00</td>
<td>3.92</td>
<td>4.72</td>
<td></td>
</tr>
<tr>
<td>[34]</td>
<td>49</td>
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<td>2</td>
<td>18</td>
<td>6</td>
<td>6</td>
<td>5.50</td>
<td>2.07</td>
<td>2.30</td>
<td></td>
</tr>
<tr>
<td>[44]</td>
<td>25</td>
<td>14</td>
<td>2</td>
<td>10</td>
<td>4</td>
<td>0</td>
<td>5.83</td>
<td>2.47</td>
<td>2.94</td>
<td></td>
</tr>
</tbody>
</table>

Proposed MLI 31 12 3 10 4 0 5.87 2.80 3.37

5. Power Loss Analysis

Losses in terms of power and efficiency in the overall sense of suggested topology were estimated by using PLECS software. Conduction and switching losses for all the switches and losses across the capacitors were calculated precisely using thermal modeling in the software. IGBT switch IGA30N60H3 manufactured by Infineon was taken for this analysis. The turn ON, turn OFF, and conduction loss model of the IGBT taken is given in Figure 5, respectively. Here three main types of losses were taken into account: switching losses ($P_{S}$) and conduction losses ($P_{C}$) of all the semiconductor devices and ripple loss ($P_{R}$) of the capacitors.
5. Power Loss Analysis

Losses in terms of power and efficiency in the overall sense of suggested topology were estimated by using PLECS software. Conduction and switching losses for all the switches and losses across the capacitors were calculated precisely using thermal modeling in the software. IGBT switch IGA30N60H3 manufactured by Infineon was taken for this analysis. The turn ON, turn OFF, and conduction loss model of the IGBT taken is given in Figure 5, respectively. Here three main types of losses were taken into account: switching losses ($P_{\text{ON}}$) and conduction losses ($P_{\text{CON}}$) of all the semiconductor devices and ripple loss ($P_{\text{RIP}}$) of the capacitors.

5.1. Switching Losses ($P_S$)

Switching losses were there at the instant when the switches turn ON or OFF. The following equations can be expressed for the $k$th switch considering approximation in a linear sense between current and voltage of switches during the period of switching [45]:

Loss of power during switching

\[
\text{ON} = P_{S,\text{on},k} = f \int_{t_{\text{on}}}^{t_{\text{off}}} v(t) i(t) dt = f \int_{0}^{t_{\text{off}}} V_{S,k} \left(-\frac{l_k}{l_{\text{on}}} (t - t_{\text{on}})\right) dt = \frac{1}{6} f V_{S,k} l_k t_{\text{on}}
\]  

(21)

Loss of power during switching

\[
\text{OFF} = P_{S,\text{off},k} = f \int_{0}^{t_{\text{off}}} v(t) i(t) dt = f \int_{0}^{t_{\text{off}}} V_{S,k} \left(-\frac{l_k'}{l_{\text{off}}} (t - t_{\text{off}})\right) dt = \frac{1}{6} f V_{S,k} l_k' t_{\text{off}}
\]  

(22)

where $l_k$ and $l_k'$ denote currents across the $k$th switch when it was turned ON, and prior to turning it OFF, respectively. $f$ is the frequency of switching and $V_{S,k}$ denotes voltage for the OFF-state of the $k$th switch. For calculating the loss in switching as total, the ON ($N_{\text{on}}$) and the OFF number of switching states ($N_{\text{off}}$) for each cycle are multiplied with (21) and (22) following (23):
5.2. Conduction Losses ($P_C$)

The internal resistance of each component, i.e., semiconductor devices and capacitors, had to be addressed to calculate losses in conduction at the condition of steady-state. Each capacitor was assumed to be the same. The results were taken using the PLECS software for a resistive load since the state of resistive loading is said to be the worst-case scenario in the analysis of loss of power for the SCMLIs [45,46].

5.3. Capacitor Ripple Losses ($P_R$)

Ripple losses occurred by the difference between the input voltage ($V_{in}$) and the voltage across the capacitors ($V_{Cj}$($j = 1,2,3,4$)), when the capacitors are connected in parallel [46]. It was assumed that the capacitor was fully charged to $V_{in}$ during the charging state.

The capacitor ripple voltage is taken as:

$$\Delta V_{Cj} = \frac{1}{C_j} \int_{t'}^{t} i_{Cj}(t) dt \quad \text{for} \quad j = 1, 2, 3, 4 \quad (24)$$

Here, $i_{Cj}$ denotes passing current of the $j$th capacitor. The discharging period is $[t' - t]$. Thus, the total ripple loss in the duration of the output waveform cycle is given by (25).

$$P_R = \frac{f}{2} \sum_{j=1}^{4} C_j \Delta V_{Cj}^2 \quad (25)$$

From (24) and (25), it is evident that ripple loss is inversely proportional to the capacitance. Thus, larger capacitance leads to less ripple loss and hence improved efficiency. The efficiency of the overall proposed inverter is given by (26).

$$\eta = \frac{P_o}{P_o + P_S + P_C + P_R} \quad (26)$$

The efficiency versus output power curve for both symmetrical and asymmetrical configurations is shown in Figure 6 for a resistive load. Maximum efficiency was achieved with about 98.7% along with a 100-watt output power for both the configurations in which capacitor ripple loss had neglected. Capacitor ESR loss (conduction loss due to internal resistance of the capacitors (here 0.1 ohm is taken)) was taken in its place. Power loss distribution among different switches and capacitors are given in Figure 7 for both settings. $S_1$ and $S_2$ were the bidirectional switches, as shown in Figure 1. Both switches of the bidirectional switches had the same loss. All the complementary switches also had the same losses as the number of states when they were turned ON and turned OFF for a full cycle.
0.16%, respectively. Voltage and current THD was obtained as 2.63% and 97.5%, respectively. For symmetrical configuration, the magnitude of the three DC voltage sources was similar, and for simulation purposes, it was taken to be 100 volts. The resultant voltage at the output had a peak voltage of 300 V with 50-V steps and 13 levels in totality. All four capacitances were considered to be 4700 µF. The current waveform and voltage at the output for Z = 50 Ω +100 mH as the R-L load with varying MI are presented in Figure 8a. The number of levels for voltage at the output was directly proportional to the MI. At MI = 0.5, the output voltage levels were reduced by half, which can be analyzed from Figure 8a. The current waveform and voltage at the output with a load change of Z = 50 Ω +100 mH to Z=25 Ω +100 mH, which are given in Figure 8b–d, show the harmonic analysis of the voltage obtained and the current waveforms for Z = 50 Ω +100 mH, respectively. Voltage and current THD was achieved as 6.36% and 0.56%, respectively. Current THD was lower as the inductive load reduced the high-frequency current components.

For the asymmetrical case, V₁ = 240 V, V₂ = 20 V, and V₃ = 40 V. The resultant output waveform has a peak voltage of 300 Volts with a step size of 20 Volts. Figure 9a shows the current waveform and voltage at the output for Z = 50 Ω +100 mH as the R-L load with varying MI. Figure 9b presents the current waveform and voltage at the output with Z = 50 Ω +100 mH to Z = 25 Ω +100 mH as the change in load. Harmonic analysis for the obtained voltage and current waveforms for Z = 50 Ω +100 mH, as shown in Figure 9c,d, respectively. Voltage and current THD was obtained as 2.63% and 0.16%, respectively.

**Figure 6.** Efficiency versus output power curve for both symmetrical and asymmetrical configurations.

**Figure 7.** Distribution of power loss for (a) symmetrical 13-level topology and (b) asymmetrical 31-level topology.

### 6. Results and Discussions

Simulation of the suggested topology for asymmetric and the symmetric case was done using Matlab® 2018a and for verifying the results obtained, experimental results were also taken. Both of these results are discussed in the subsequent subsection.

#### 6.1. Simulation Results

For symmetrical configuration, the magnitude of the three DC voltage sources was similar, and for simulation purposes, it was taken to be 100 volts. The resultant voltage at the output had a peak voltage of 300 V with 50-V steps and 13 levels in totality. All four capacitances were considered to be 4700 µF. The current waveform and voltage at the output for Z = 50 Ω +100 mH as the R-L load with varying MI are presented in Figure 8a. The number of levels for voltage at the output was directly proportional to the MI. At MI = 0.5, the output voltage levels were reduced by half, which can be analyzed from Figure 8a. The current waveform and voltage at the output with a load change of Z = 50 Ω +100 mH to Z=25 Ω +100 mH, which are given in Figure 8b–d, show the harmonic analysis of the voltage obtained and the current waveforms for Z = 50 Ω +100 mH, respectively. Voltage and current THD was achieved as 6.36% and 0.56%, respectively. Current THD was lower as the inductive load reduced the high-frequency current components.

For the asymmetrical case, V₁ = 240 V, V₂ = 20 V, and V₃ = 40 V. The resultant output waveform has a peak voltage of 300 Volts with a step size of 20 Volts. Figure 9a shows the current waveform and voltage at the output for Z = 50 Ω +100 mH as the R-L load with varying MI. Figure 9b presents the current waveform and voltage at the output with Z = 50 Ω +100 mH to Z = 25 Ω +100 mH as the change in load. Harmonic analysis for the obtained voltage and current waveforms for Z = 50 Ω +100 mH, as shown in Figure 9c,d, respectively. Voltage and current THD was obtained as 2.63% and 0.16%, respectively.
6.2. Experimental Results

Inductive load reduced the high-frequency current components. The current waveform and voltage at the output with a load change can be analyzed from Figure 8a. The current waveform and voltage at the output with $Z = 50 \Omega$ can be compared in Figure 8b–d, respectively. Voltage and current THD was obtained as 2.63% and 0.16%, respectively.

(a) (b)

Figure 8. Simulation results of 13-level symmetric topology with (a) dynamic change of modulation index, (b) output waveforms for varying load, (c) Harmonic profile of the output voltage for $Z = 50 \Omega + 100 \text{ mH}$, and (d) Harmonic profile of the output current for $Z = 50 \Omega + 100 \text{ mH}$.

(c) (d)

Figure 9. Simulation results of 31-level asymmetric topology with (a) dynamic change of modulation index, (b) Harmonic profile of the output voltage for $Z = 50 \Omega + 100 \text{ mH}$, (c) output waveforms for varying load of $Z = 50 \Omega + 100 \text{ mH}$ to $Z = 25 \Omega + 100 \text{ mH}$, and (d) Harmonic profile of the output current for $Z = 50 \Omega + 100 \text{ mH}$.

6.2. Experimental Results

Figure 10 shows that the above results obtained were verified using an experimental prototype for both symmetrical and asymmetrical cases. Toshiba IGBT GT50J325 was taken as the switch, and the dSPACE 1104 controller was used to obtain gating pulses for these switches. Figure 11a,b shows the output voltage and current waveforms for RL load of $200 \Omega + 100 \text{ mH}$ and a resistive load of $120 \Omega$, respectively, for the symmetrical case. In this case, $V_1 = V_2 = V_3 = 80 \text{ V}$ was chosen. The thirteen-level output had the peak voltage of 240 V with a step voltage of 40 V. The output waveforms with load change and MI change are given in Figure 11c,d. The load change was from $120 \Omega$ to $60 \Omega$, and MI...
change was from 0.33 to 1. The 13-level output is shown in Figure 12a. For the asymmetrical case, \( V_1 = 240 \, \text{V} \), \( V_2 = 20 \, \text{V} \), and \( V_3 = 40 \, \text{V} \) were taken. Figure 12b shows the output waveform having a load change from no load to 120 \( \Omega \) to 60 \( \Omega \). Figure 12c shows the thirty-one-level output voltage with the maximum voltage of 300 volts having steps of 20 volts. The output waveform for a resistive load of 32 \( \Omega \) is given in Figure 12d.

![Figure 10. Experimental setup of the proposed topology.](image)

Figure 11. Experimental results: (a) Output voltage and current for the symmetric case with Resistive-Inductive (R-L) load; (b) output waveform with R-load; (c) output waveform with load change; (d) output waveform with Modulation Index (MI) change.
was carried out to verify the simulation results under the condition of varying load and modulation indexes. Thus, the proposed topology is the right candidate to be used in the smart grid system 4.0, function, and it stands well with other topologies shown in Tables 3 and 4. Hardware implementation in Section 4.1 and given in Table 3. Its economic aspect was also taken into account using the cost function, and it stands well with other topologies shown in Table 3 and Table 4.

Apart from lower switch count, TSV was also remarkably lower for the symmetrical case and comparable with other recent topologies in the asymmetrical case. It had the lowest switch count compared to other 13-level topologies presented, as discussed in Section 4.1 and given in Table 3. Its economic aspect was also taken into account using the cost function, and it stands well with other topologies shown in Tables 3 and 4. Hardware implementation was carried out to verify the simulation results under the condition of varying load and modulation indexes. Thus, the proposed topology is the right candidate to be used in the smart grid system 4.0, which has a stringent requirement under IEEE 1547 standards.

**7. Conclusions**

An innovative SCMLI topology is suggested here. The mentioned topology could operate for symmetrical as well as the asymmetrical case. Apart from lower switch count, TSV was also remarkably lower for the symmetrical case and comparable with other recent topologies in the asymmetrical case. It had the lowest switch count compared to other 13-level topologies presented, as discussed in Section 4.1 and given in Table 3. Its economic aspect was also taken into account using the cost function, and it stands well with other topologies shown in Tables 3 and 4. Hardware implementation was carried out to verify the simulation results under the condition of varying load and modulation indexes. Thus, the proposed topology is the right candidate to be used in the smart grid system 4.0, which has a stringent requirement under IEEE 1547 standards.


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