An FPGA-Based Neuron Activity Extraction Unit for a Wireless Neural Interface

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Abstract: As computational and functional brain model development are solely dependent upon the data acquired from the neural interface, this device plays a vital role in both prosthetic developments and neurological experiments. A wireless neural interface is preferred over a traditional wired one because it can maximize the comfort of the subject and ensure the freedom of movement while implemented. This paper describes the field programmable gate array (FPGA) prototype design of a low-power multichannel neuron activity extraction unit suitable for a wireless neural interface. To achieve the low-power requirement, we proposed a novel neural signal extraction algorithm which can provide an up to 6000X transmission rate reduction considering the input signal. Consequently, this technique offers at least 2X power reduction compared to the state-of-the-art systems. We implemented this scheme in Xilinx Zynq-7000 FPGA, which can be used as an intermediate transition towards the application specific integrated circuit (ASIC) design for on-chip neural signal processing. The proposed FPGA prototype offers reconfigurable computability, which means the model can be modified and verified according to prerequisites before the final ASIC design. This prototype consists of a signal filtering unit and a signal extraction unit which can be used either as stand-alone units or combined as a complete system. Our proposed scheme also provides a provision to work as a single-channel or a scalable multichannel interface based on user's demands. We collected practical neural signals from rat brains and validated the efficacy of the implemented system using in-silico signal processing.

Keywords: FPGA; signal processing; neural signal extraction

1. Introduction

A neural interface is used for gaining access to the brain's circuits. It creates a direct information pathway between the brain and the outside world [1] as a gateway component of neural devices. With the recent drastic advancement in experimental neuroscience, the neural interface is becoming sophisticated and miniaturized [2–6]. The longer-term procedure especially requires miniaturized and wireless devices to ensure patients' comfort and flexibility [7–9]. The wireless neural interface is also suitable for preclinical experiments with nonhuman behaving animals [10–13]. The wireless nature of the experiment ensures untethered movement during the procedure [14]; hence, more naturalistic brain signal recording is possible.

As most of the brain signals are collected using multiple channels, the raw neural signal contains a bulk-load of information which needs to be transmitted for further processing [15–17]. For example,

if we consider 8 bits/sample for a 64-channel system, the required data transmission rate will be more than 11 Mbps [18]. Traditional wired neural devices can transmit this high a volume of data with ease using an appropriate serial or a parallel communication protocol. However, if we consider wireless neural devices, this massive amount of data creates a bottleneck for the technology, as the system will then consume significant battery power. Hence, a standalone wireless system would have to undergo frequent battery replacement which would disrupt a continues procedure. Additionally, higher power consumption is associated with a considerable amount of heat dissipation which may cause critical tissue damage. Therefore, a systemic approach is needed to lower the transmission rate by filtering out redundant parts of the signals. In this work, we developed a novel algorithm to ensure a lower data transmission rate for wireless neural signal transmission.

To implement the proposed algorithm at the circuit level, we have incorporated a field programmable gate array (FPGA) to design the hardware and verify the algorithm. A field programmable gate array (FPGA) is an integrated circuit which can be reconfigured according to the users' requirements [19]. Besides, when it comes to the question of processing multiple signals at the same time, a FPGA performs notably faster due to its inherent capacity of parallel computation [20,21]. As brain signals are typically collected using multiple channels, the FPGA presents itself as an optimum candidate to design the system. We have used the development board ZedBoard for the implementation of our design. This board utilizes Xilinx Zynq-7000 SoC as the FPGA chip for signal processing. In this paper, we present this FPGA prototype design, and we checked in different configurations which intermediary platform can be converted into an ASIC according to specific user demands.

The wireless neural interface is gaining popularity due to its convenience and flexibility. Most studies are primarily concentrated on wireless communication technology [11,12], wireless power transmission techniques [13,22] and compatible electrode development [23,24]. Only a few of them focus on dedicated signal processing algorithms for neural data [25,26]. To the best of our knowledge, none of these studies presented any design which is reconfigurable according to the end-user's demands. The major concern of this research was to develop circuit-level implementations of algorithms for data reduction to reduce the data transfer rate, which would in turn decrease the power consumption for wireless systems. Herein, we also introduce a digital filtering scheme that can be incorporated with the signal extraction unit if the user wants to omit some signal preprocessing steps. Besides, our prototype presents a design to serve as either a single-channel or a multichannel (with scalable number of channels) scheme based on design requirements. Finally, we evaluated our design with neural signals collected from rat brains to validate the prototype.

2. Methodology

As a multichannel input with high sampling frequency, the neural signal acquires a large amount of data per second which contains information that may be redundant for a specific application or neural experiment. For designing the prototype, we have considered an experiment which collects single-neuron activity signals from rat brain cells using a wireless neural interface.

As it is a standalone transmission system, the high data transmission rate consumes a large amount of power and consequently lowers the battery life. Therefore, the total possible time for conducting such a contentious experiment is short. To increase the duration of this procedure, we propose an algorithm that can reduce the data transmission rate. We have considered three factors for this design. Firstly, single-neuron activity in the rat brain is predominantly a high-frequency signal (>300 Hz) [27]. Secondly, due to the sparse nature of the neural signal, it is rare that all channels are activated at the same time [28].

Finally, signal epochs containing neural activities can be detected with a threshold voltage. This threshold is dependent on the noise level of the signal acquisition system [29]. Therefore, we only need to transmit when a particular channel is recording a high-frequency signal above a certain voltage, and we need to know the starting time and peak amplitude of that signal epoch. Considering these parameters, we have designed our proposed system, as shown in Figure 1.
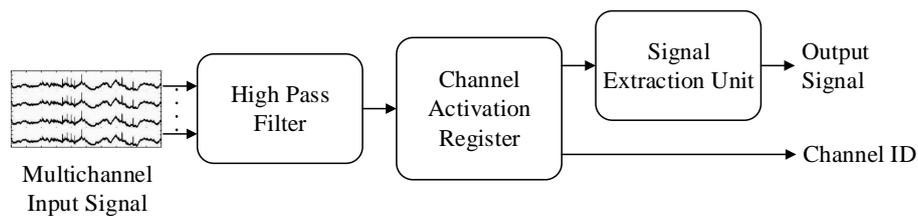
Figure 1. Simplified block diagram of the proposed system.

This system has three subunits. At first, the signal goes through the high pass filter to drop out the lower frequency signal. The filtered signal then passes through the signal extraction unit, which excludes the insignificant low voltage signal. A signal higher than a predefined threshold voltage can pass through this unit and the channel activation register unit records the relevant channel identification remarks. The output contains the waveform when the neuron is activated. It also includes the timestamp of the neuron activation, the peak amplitude during each activated epoch and the credential of the channel associated. At this point, it should be noted that, as an FPGA prototype, our design is easy to reconfigure as per the user's demand before ASIC implementation. For example, the filter parameter can be modified to select a desired passband, or the threshold value of the signal extraction unit can be adjusted. Additionally, we can choose the number of channels of the system to make it compatible with any distinct experiment parameters. This scalability is one of the unique features of the proposed design.

3. System Architecture

For the ease of explanation, we divided the prototype into three subsystems—i, a neural signal filter unit; ii, a neuron activity extraction unit; and iii, a channel activity register. The extraction unit is the fundamental part of this system which cannot be omitted in any design. The other two units can be excluded depending on the design requirements. For example, if there is a built-in analogue filter available with the signal collecting electrode assembly, then the filter unit becomes redundant. Similarly, if there is only one channel for signal acquisition, then the channel activation register is not required.

For this research, we have incorporated all three subunits to facilitate our desired specifications. Xilinx System Generator—a MathWorks Simulink toolbox—was used for FPGA programming. The system architecture is described in the following three subsections. It should be noted that this is a reconfigurable hardware model. Therefore, anyone can modify this FPGA design according to their needs before the final ASIC implementation.

3.1. Neural Signal Filter Unit

As mentioned in the section methodology, we need to filter out the low-frequency ($\leq$300 Hz) components for extracting single-neuron activity from rat brain signals, as they do not contain any significance. For this purpose, we designed a high-pass equiripple FIR filter. The design parameters were selected as follows: stop-band frequency, F_{stop} = 300 Hz; pass-band frequency, F_{pass} = 400 Hz; stop-band attenuation, A_{stop} = 80 dB; pass-band attenuation, A_{pass} = 1 dB; density factor, D = 16. Considering a minimum order design, we get the frequency response of this filter as shown in Figure 2. Here the cutoff frequency is approximately 375 Hz, which is sufficient [27] for neural activity extraction.
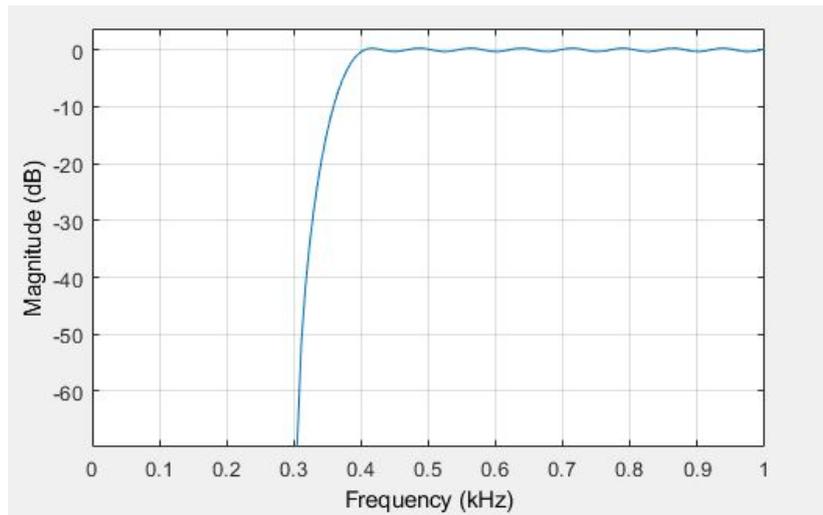
Figure 2. Frequency response of the neural signal FIR filter.

3.2. Neuron Activity Extraction Unit

In this subsection, the design of a neural activity extractor is discussed. As mentioned in the previous section, the brain signal indicates any neural activity only when it has a value greater than the noise voltage level. In our experiment, the collected signals become significant when they cross the 40 μV voltage level. Therefore, we are only required to transmit the signal when the input crosses this threshold voltage. There is a way of lowering the data transmission rate further—by transmitting only timestamps and peak amplitudes of the neural activation events. This process can drastically reduce the data transmission rate and power consumption. However, the processed data will contain only a fraction of the information compared to the original signal. Depending on the application requirement, the user can decide what type of output is needed.

Algorithm 1 characterizes the proposed methodology of neural activity extraction with three output components which are computed under a loop: (i) the time-stamp (OP_Time) is represented by lines 5 and 6; (ii) the peak amplitude (OP_Amp) is found by lines 7–13; and (iii) the brain wave throughput (OP_Wave) is presented by lines 3 to 9. At first, the input signal is compared with the threshold voltage. We have chosen 40 μV as the threshold voltage for this research. If the input voltage is higher than this level, the signal is passed, and the starting time of this event is recorded. A separate memory block is initialized during each episode, to keep track of the peak amplitude.

The system architecture of this subsystem is shown in Figure 3. Here, the input signal (Signal_In) of this subsystem is the filtered neural signal. This signal may come directly from an analog filter or from the filter described in the previous subsection. The signal extraction process starts by comparing the input signal with the threshold voltage. When the input signal becomes higher than that voltage, it is allowed to produce the output signal (OP_Wave). At the same time, a count-up timer circuit is used to keep track of time, and the starting time of each neural event is transmitted (OP_Time). Subsequently, a memory block is activated in every epoch to record the peak amplitude (OP_Amp). This value is computed throughout a neural activity, and this block only updates its stored data if the incoming neural signal possesses a greater value than its predecessor. The final value is then transmitted right after each epoch completion.
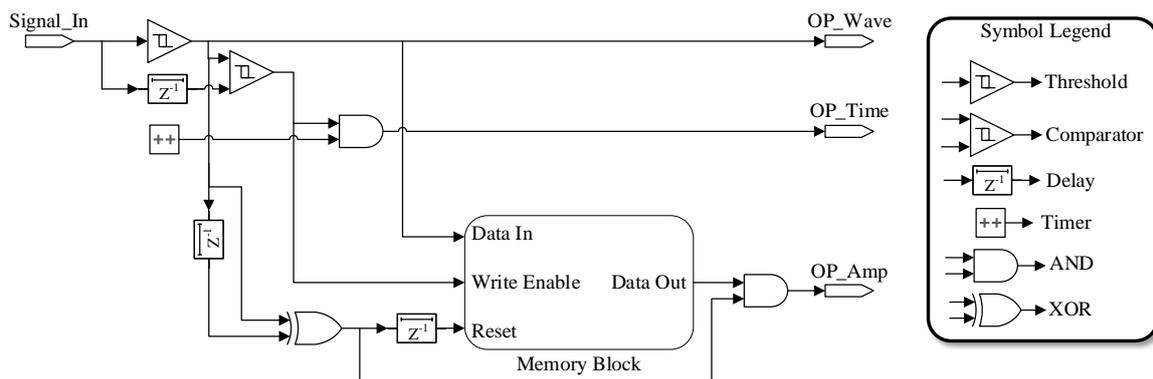
Figure 3. System architecture of the neuron activity extraction unit.

Algorithm 1: Neuron activity extraction.

Input: *Signal_In*
Output: *OP_Time*, *OP_Amp*, *OP_Wave*
1   $Op\_Amp\_Temp \leftarrow 0$
2   **for** $t \leftarrow 0$ *to* t **do**
3   **if** *absolute* $(Signal\_In(t)) > 40$ **then**
4          $OP\_Wave(t) \leftarrow Signal\_In(t)$
5   **if** *absolute* $(Signal\_In(t-1)) > 40$ **then** $OP\_Time \leftarrow t$
6   **else** $OP\_Time \leftarrow 0$
7   **if** *absolute* $(Signal\_In(t)) > absolute$ (OP_Amp_Temp) **then**
           $OP\_Amp\_Temp \leftarrow Signal\_In(t)$
8   **else**
9          $OP\_Wave(t) \leftarrow 0$
10   **if** *absolute* $(Signal\_In(t-1)) > 40$ **then**
11             $OP\_Amp \leftarrow OP\_Amp\_Temp$
12             $OP\_Amp\_Temp \leftarrow 0$
13   **else** $OP\_Amp \leftarrow 0$
14 **return** OP_Time, OP_Amp, OP_Wave

3.3. Channel Activity Register

For a multichannel system, we need to include an additional component—a channel activation register. It records the channel identity during a neural activation epoch. This register enables the user to find out from which electrode the neural signal is recorded during an activity epoch. Algorithm 2 presents the working principle of this subsystem. If the signal from any channel exceeds the predefined threshold (in this case 40 μV), this unit displays that channel number once per epoch—at the beginning of each neural event. This subsystem also passes the input signal when it is higher than that threshold. This signal will act as the input of the extraction subsystem in a multichannel system.

Figure 4 illustrates the proposed channel activation register architecture for a two-channel system. Nonetheless, this design can be replicated for any number of input channels specified by the user. The proposed subsystem takes the filtered signal as its input, and if it has a value higher than the threshold, the subsystem passes the associated channel identification information (Ch_ID) to the buffer register for transmission. Additionally, this unit works as a multiplexer, as it takes multichannel inputs and produces single-channel output (Ch_Out). As previously mentioned, a neural signal is sparse in nature—only one channel is activated during a neural epoch. Here, this single-channel output

(Ch_Out) is the activated neural signal which works as the input for the neural activity extraction subsystem of a complete multichannel system.
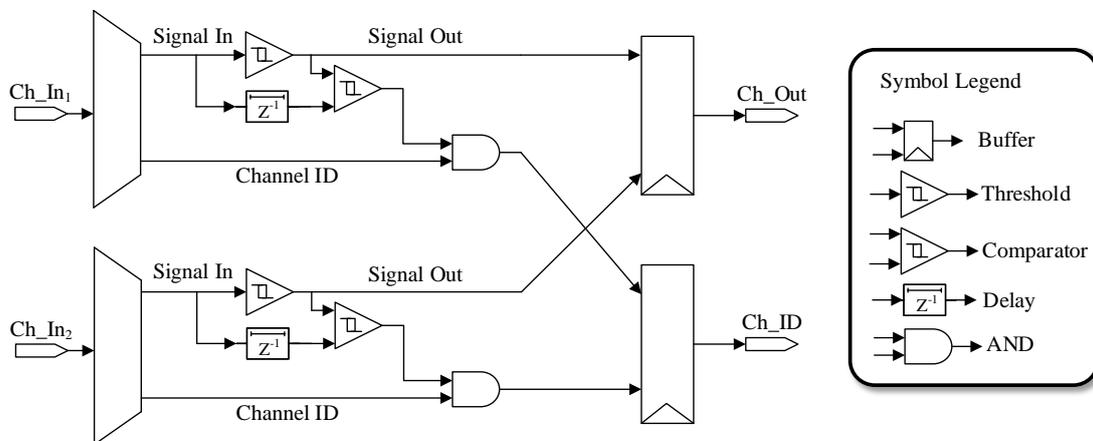

Figure 4. System architecture for a channel activation register unit with 2 input channels.

Algorithm 2: Channel activation register.

Input: *Ch_In*
Output: *Ch_Out*, *Ch_ID*

1   **for** $i \leftarrow 0$ *to* N **do**
2   **for** $t \leftarrow 0$ *to* t **do**
3   **if** *absolute* $(Ch\_In(t)) > 40$ **then**
4         $Ch\_Out(t) \leftarrow Ch\_In(t)$
5   **if** *absolute* $(Ch\_Out(t-1)) <= 40$ **then** $Ch\_ID \leftarrow i$
6   **else** $Ch\_ID \leftarrow 0$
7   **else**
8         $Ch\_Out(t) \leftarrow 0$
9         $Ch\_ID = 0$
10   **return** Ch_Out, Ch_ID

3.4. Complete Model

We have already discussed the design of three subsystems which are essential components of the complete model of the prototype. There are four possible configurations for the complete setup based on the input parameters-

1. Single-channel filtered (SCF) input;
2. Single-channel unfiltered (SCUF) input;
3. Multichannel filtered (MCF) input;
4. Multichannel unfiltered (MCUF) input.

We can reconfigure the FPGA to choose from any of these configurations and test the efficacy of the system before the final ASIC implementation. If the system has one channel with a filtered input, only the signal extractor unit will be adequate as the complete model. Figure 5 illustrates this design setup.
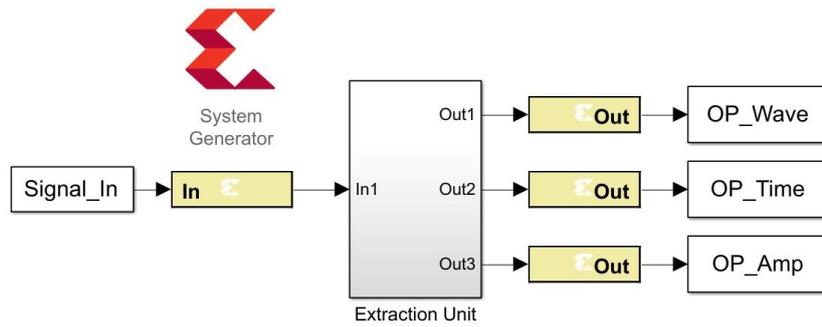
Figure 5. Design of a single-channel filtered input system (SCF) in SysGen.

For a single-channel system with an unfiltered input, we need to concatenate the filter unit with the signal extractor unit, as presented in Figure 6.
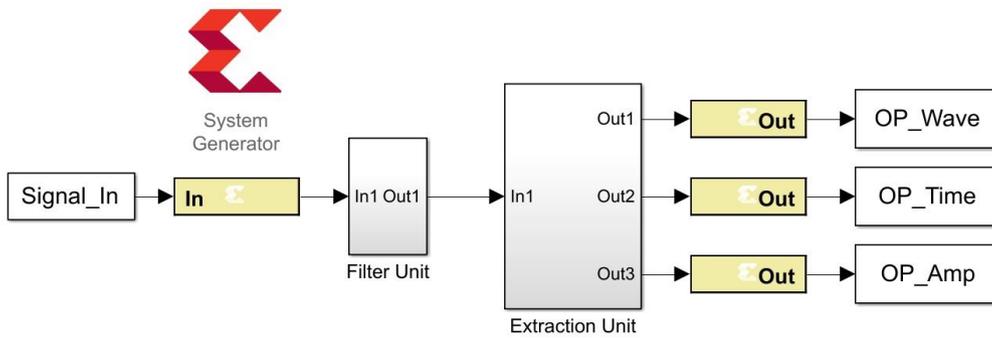

Figure 6. Design of a single-channel unfiltered input system (SCUF) in SysGen.

For multichannel systems, we need to include the channel activation register to record the channel identity during a neural activation epoch. Two-channel systems are presented here as examples of multichannel systems. The configuration of a multichannel system with filtered input is demonstrated in Figure 7.
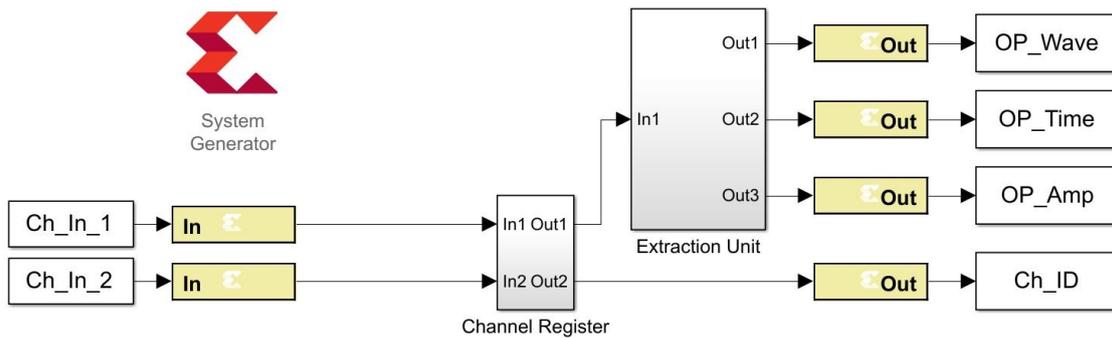

Figure 7. Design of a multichannel filtered input system (MCF) in SysGen.

The design of the multichannel system with unfiltered input is similar to its filtered counterpart except for the addition of the filtering subsystems as shown in Figure 8.
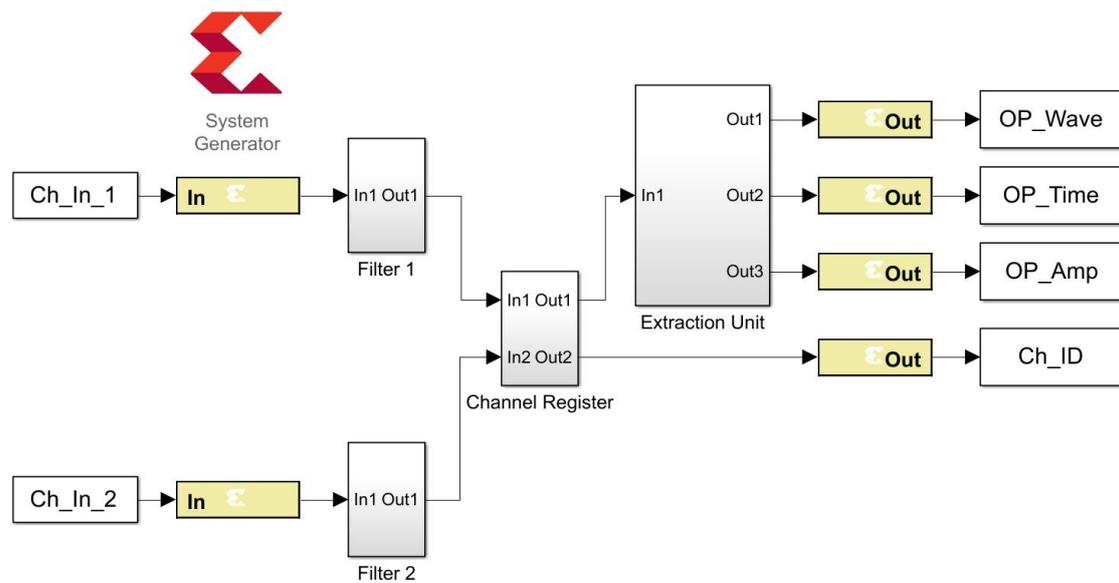
Figure 8. Design of a multichannel unfiltered input system (MCUF) in SysGen.

4. Implementation and Results

We have implemented the prototype system in Xilinx Zynq-7000 (Artix-7) FPGAs on ZedBoard. Although this FPGA development board provides a cost-effective [30] solution for our system implementation, the design is not limited to this board only; it can be implemented in any modern FPGAs. As described in the previous section, there are four possible configurations (SCF, SCUF, MCF and MCUF shown respectively in Figures 5–8) from which the user can select their required design. Table 1 shows the hardware resources required for each of these setups. In this table LUT, LUTRAM, FF, BRAM and DSP stand for look up table, look up table RAM, flipflop, block RAM and digital signal processing blocks respectively.

Table 1. System resource utilization.

Configuration	LUT	LUTRAM	FF	BRAM	DSP
SCF	34	0	1	0.5	0
SCUF	778	465	1353	0.5	26
MCF	35	0	1	0.5	0
MCUF	1500	930	2703	0.5	52

From the Table 1 it is evident that the systems with unfiltered inputs require more resources than the systems with filtered inputs. This is because the neural filter subsystem requires additional LUT, RAM and DSP blocks for signal processing. As more system resources consume more power and require extra floor space for the ASIC chip implementation [31], we suggest using filtered input for better performance if the design permits. Since analogue filters are inexpensive and have the capability of real-time filtering [32], they are suitable for the proposed neural signal extraction system. However, the performances of the digital filters are predominantly better than those of their analogue counterparts [33]. Therefore, in our reconfigurable design, the user can decide which configuration is the most suited for any specific system requirement.

It should be noted that we have used two-channel systems as representatives of multi-channel models. To analyze the consequences of additional input channels on resource utilization, we have also implemented four, eight, sixteen, thirty-two and sixty-four channel filtered input systems.

Figure 9 demonstrates this resource evaluation. Here, IO represents the number of input–output blocks in the FPGA. To explain the comparative resource utilization of the systems with a different number of input channels, we need to focus on their design. As discussed in the previous section,

the prime difference between a single-channel filtered input system and a two-channel filtered input system is the inclusion of a channel activity register unit. Additionally, the two-channel filtered input system has an additional input and output (channel ID) compared to its single-channel counterpart. Therefore, the two-channel system needs to employ one extra LUT and two IO blocks to facilitate its design. However, when the number of input channels increases from two to sixty-four, no further logic components are needed; only the usage of IO blocks is gradually increased. This analysis indicates that we can effectively increase the number of input channels based on our requirement without overwhelming our system's resources. This ensures the scalability of the implemented prototype.
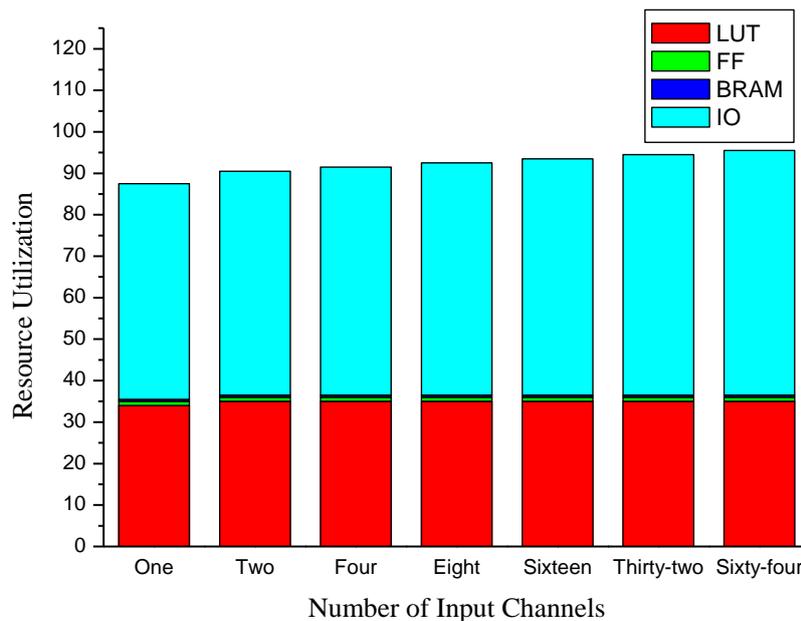

Figure 9. Comparative resource utilization for different numbers of channels.

To assess the FPGA prototype, we recorded spontaneous neural activity from rat CA1 region of the hippocampus using acutely implanted microelectrodes at the Biomedical Engineering Department of USC. We used these signals to formulate in-silico datasets for our experiment. The original neural signals include the broadband raw data from multichannel recordings along with the filtered output from a high-pass filter with 300 Hz cut-off frequency.

The resultant outputs from the single-channel unfiltered input system (Figure 6) and the multi-channel filtered input system (Figure 7) are shown in Figures 10 and 11 respectively. To demonstrate the outcome of the filtering subsystem, an internal signal (filter output) is added in Figure 10. The practical output consists of the waveform during neural activity, its timestamp and peak amplitude. Here, the threshold is for triggering transmission, not for spike sorting, although depending on applications, the timestamp and peak amplitude can be used as a simple spike sorting method. However, complete spike sorting can be performed after wireless transmission of the signal during neural activity; see Figure 10c. Figure 11 illustrates the signals from a multichannel system with two inputs. It has an additional channel identification output to display the associated channel number of any neural activity. This output is illustrated in Figure 11f.
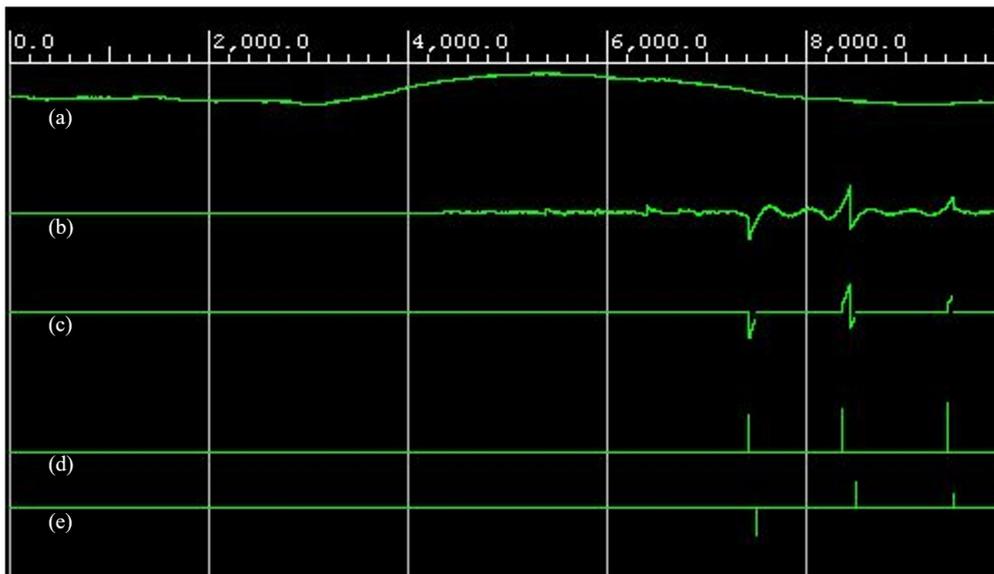
Figure 10. Waveforms from the single-channel unfiltered input system: (**a**) the input signal (Signal_In), (**b**) filter output (internal signal), (**c**) output wave during neural activity (Op_Wave), (**d**) timestamp (Op_Time) and (**e**) peak amplitude (Op_Amp).

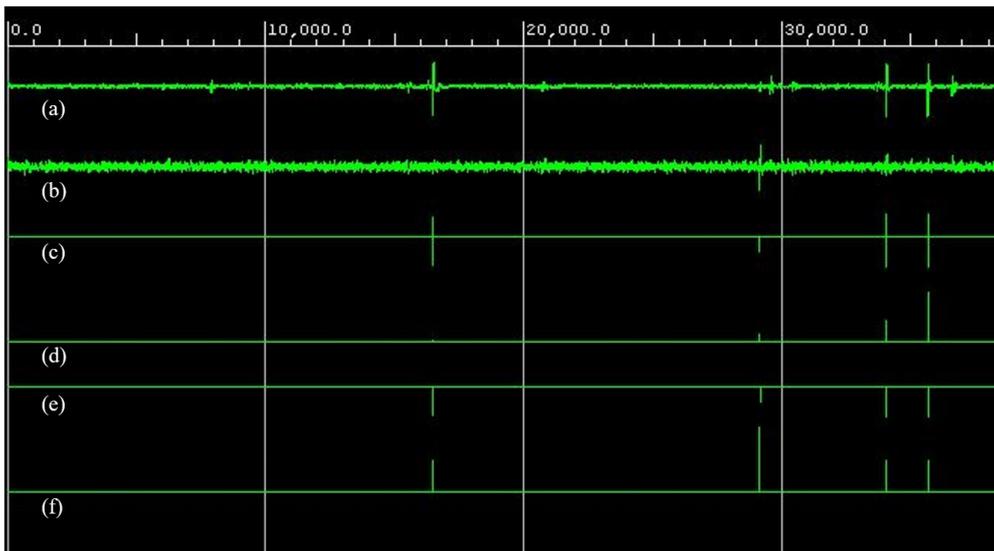**Figure 11.** Waveforms from the multichannel (two-channel) filtered input system: (**a**) input signal from Channel-1 (Ch_In_1), (**b**) input signal from Channel-2 (Ch_In_2), (**c**) output wave during neural activity (Op_Wave), (**d**) timestamp (Op_Time), (**e**) peak amplitude (Op_Amp) and (**f**) channel identification (Ch_ID).

If a wireless neural interface continuously transmits the raw signal collected from the brain, it will reduce the duration of an uninterrupted experiment by rapidly draining the battery. As previously mentioned, an 8 bits/sample sixty-four channel system requires an 11 Mbps transmission rate [18]. However, reference [34] reports that the average neural signal spiking rate is less than 0.5 Hz for awake rats. We programmed the neural interface to transmit only when the neural activity is occurring. Thus, our system can lower the transmission up to 1.6 Kbps for a 64-channel system (considering a 10 kHz sampling rate)—a 6000X transmission rate reduction comparing with the input.

According to the post-implementation report from Xilinx Vivado simulator, the on-chip dynamic power consumption of the prototype (a 64-channel filtered input system) is 3 mW—an at least 2X power reduction compared with state-of-the-art systems. As FPGA consumes more energy than

an application-specific IC, it is estimated that the power consumption will further reduce after ASIC implementation.

A comparative study between the implemented prototype and related previous works is presented in Table 2. Several research groups across the world are working on the development of wireless neural interfaces. Due to various components being required to build up the complete system, there are multiple aspects to contributions in this field, as seen in Table 2. Only a few research groups ([26,35]) worked on the signal processing perspective of the wireless neural interface. Among these works, our implemented system offers the minimum data transmission rate at the lowest power consumption. Moreover, apart from our proposed method, none of these previous works are reconfigurable and scalable. Therefore, our prototype's neural activity extraction unit is suitable for customizable system-level applications in wireless neural interfaces.

Table 2. Comparison with previous works.

Reference	Primary Focus	Implement	Reconfigurability	Scalability	Channel Count	Transmission/ Data Rate	Power
Farshchi et al. [8]	Communication technique	PCB	No	No	6	9.6 Kbps	66 mW
Borton et al. [12]	Communication technique	PCB	No	No	100	24 Mbps	90.6 mW
Lee et al. [11]	Communication technique	ASIC	No	No	32	9 Mbps	18.9 mW
Kim et al. [22]	Wireless power transmission	ASIC	No	No	16	15 Kbps	-
Lee et al. [13]	Wireless power transmission	ASIC	No	No	32	9 Mbps	35 mW
Lo et al. [23]	Electrode development	ASIC	No	No	160	2 Mbps	18 mW
Kang et al. [24]	Electrode development	PCB	No	No	5	2 Mbps	-
Bonfanti et al. [25]	Data compression	ASIC	No	No	64	1.25 Mbps	16.6 mW
Shahrokhi et al. [35]	Signal conditioning	ASIC	No	No	128	-	7 mW
Chae et al. [26]	Spike Sorting	ASIC	No	No	128	90 Mbps	6 mW
This work	Neuron activity extraction	FPGA	Yes	Yes	User Defined	1.6 Kbps	3 mW

5. Conclusions

As wireless devices ensure prolonged procedures without compromising the movement and comfort of a subject, their usage in both clinical rehabilitation and experimental research is expanding. In this research, we introduced a novel algorithm that can reduce the data transmission rate by up to 6000 times, which in turn consumes only 3 mW of dynamic power. This design presents an FPGA-based reconfigurable hardware framework which is a transitional step to the future ASIC chip that integrates a complete wireless neural interface system which can work for a longer duration without any interruption.

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References

1. Hatsopoulos, N.G.; Donoghue, J.P. The science of neural interface systems. *Annu. Rev. Neurosci.* **2010**, *32*, 249–266. [CrossRef]
2. Yuan, H.; He, B. Brain-computer interfaces using sensorimotor rhythms: Current state and future perspectives. *IEEE Trans. Biomed. Eng.* **2014**, *61*, 1425–1435. [CrossRef]
3. Elyahoodayan, S.; Jiang, W.; Xu, H.; Song, D. A Multi-Channel Asynchronous Neurostimulator with Artifact Suppression for Neural Code-Based Stimulations. *Front. Neurosci.* **2019**, *13*, 1011. [CrossRef]
4. Grill, W.M.; Norman, S.E.; Bellamkonda, R.V. Implanted neural interfaces: Biochallenges and engineered solutions. *Annu. Rev. Biomed. Eng.* **2009**, *11*, 1–24. [CrossRef]
5. Donoghue, J.P. Bridging the brain to the world: A perspective on neural interface systems. *Neuron* **2008**, *60*, 511–521. [CrossRef] [PubMed]

6. Gao, H.; Walker, R.M.; Nuyujukian, P.; Makinwa, K.A.; Shenoy, K.V.; Murmann, B.; Meng, T.H. HermesE: A 96-channel full data rate direct neural interface in 0.13 μm CMOS. *IEEE J. Solid State Circ.* **2012**, *47*, 1043–1055. [CrossRef]

7. Hampson, R.E.; Song, D.; Robinson, B.S.; Fetterhoff, D.; Dakos, A.S.; Roeder, B.M.; She, X.; Wicks, R.T.; Witcher, M.R.; Couture, D.E.; et al. Developing a hippocampal neural prosthetic to facilitate human memory encoding and recall. *J. Neural Eng.* **2018**, *15*, 36014. [CrossRef]

8. Farshchi, S.; Nuyujukian, P.H.; Pesterev, A.; Mody, I.; Judy, J.W. A TinyOS-enabled MICA2-based wireless neural interface. *IEEE Trans. Biomed. Eng.* **2006**, *53*, 1416–1424. [CrossRef]

9. Kueh, S.M.; Kazmierski, T.J. Low-Power and Low-Cost Dedicated Bit-Serial Hardware Neural Network for Epileptic Seizure Prediction System. *IEEE J. Transl. Eng. Health Med.* **2018**, *6*, 1–9. [CrossRef]

10. Szuts, T.A.; Fadeyev, V.; Kachiguine, S.; Sher, A.; Grivich, M.V.; Agrochão, M.; Hottowy, P.; Dabrowski, W.; Lubenov, E.V.; Siapas, A.G.; et al. A wireless multi-channel neural amplifier for freely moving animals. *Nat. Neurosci.* **2011**, *14*, 263. [CrossRef]

11. Lee, B.; Koripalli, M.K.; Jia, Y.; Acosta, J.; Sendi, M.S.; Choi, Y.; Ghovanloo, M. An Implantable Peripheral Nerve Recording and Stimulation System for Experiments on Freely Moving Animal Subjects. *Sci. Rep.* **2018**, *8*, 1–12. [CrossRef] [PubMed]

12. Borton, D.A.; Yin, M.; Aceros, J.; Nurmikko, A. An implantable wireless neural interface for recording cortical circuit dynamics in moving primates. *J. Neural Eng.* **2013**, *10*. [CrossRef] [PubMed]

13. Lee, B.; Jia, Y.; Abdollah Mirbozorgi, S.; Connolly, M.; Tong, X.; Zeng, Z.; Mahmoudi, B.; Ghovanloo, M. An Inductively-Powered Wireless Neural Recording and Stimulation System for Freely-Behaving Animals. *IEEE Trans. Biomed. Circ. Syst.* **2019**, *13*, 413–424. [CrossRef] [PubMed]

14. Chowdhury, M.; Hossain, Q.; Azad Hossain, M.; Cheung, R. Single feed circularly polarized crescent-cut and extended corner square microstrip antennas for wireless biotelemetry. *Int. J. Electr. Comput. Eng.* **2019**, *9*, 1902–1909. [CrossRef]

15. Mora Lopez, C.; Putzeys, J.; Raducanu, B.C.; Ballini, M.; Wang, S.; Andrei, A.; Rochus, V.; Vandebriel, R.; Severi, S.; Van Hoof, C.; et al. A Neural Probe with up to 966 Electrodes and up to 384 Configurable Channels in 0.13 μm SOI CMOS. *IEEE Trans. Biomed. Circ. Syst.* **2017**, *11*, 510–522. [CrossRef]

16. Chen, D.; Li, X.; Wang, L.; Khan, S.U.; Wang, J.; Zeng, K.; Cai, C. Fast and Scalable Multi-Way Analysis of Massive Neural Data. *IEEE Trans. Comput.* **2015**, *64*, 707–719. [CrossRef]

17. Shulyzki, R.; Abdelhalim, K.; Bagheri, A.; Salam, M.T.; Florez, C.M.; Velazquez, J.L.P.; Carlen, P.L.; Genov, R. 320-Channel Active Probe for High-Resolution Neuromonitoring and Responsive Neurostimulation. *IEEE Trans. Biomed. Circuits Syst.* **2015**, *9*, 34–49. [CrossRef]

18. Sodagar, A.M.; Perlin, G.E.; Yao, Y.; Najafi, K.; Wise, K.D. An Implantable 64-Channel Wireless Microsystem for Single-Unit Neural Recording. *IEEE J. Solid State Circuits* **2009**, *44*, 2591–2604. [CrossRef]

19. Chowdhury, M.H.; Cheung, R.C.C. Reconfigurable Computing and Hardware Acceleration in Health Informatics. In *Signal Processing Techniques for Computational Health Informatics*, 1st ed.; Ahad, M.A.R., Ahmed, M.U., Eds.; Springer International Publishing: New York, NY, USA, 2020; Chapter 9, pp. 209–229. [CrossRef]

20. Chowdhury, M.H.; Cheung, R.C.C. Reconfigurable Architecture for Multi-lead ECG Signal Compression with High-frequency Noise Reduction. *Sci. Rep.* **2019**, *9*, 17233. [CrossRef] [PubMed]

21. Chowdhury, M.H.; Cheung, R.C.C. Point-of-Care EMG Processor for the Differential Diagnosis of Neuropathy and Myopathy. In Proceedings of the IEEE EMB Special Topic Conference on Healthcare Innovations and Point-of-Care Technologies, Bethesda, MD, USA, 20–22 November 2019.

22. Kim, C.; Park, J.; Ha, S.; Akinin, A.; Kubendran, R.; Mercier, P.P.; Cauwenberghs, G. A 3 mm × 3 mm Fully Integrated Wireless Power Receiver and Neural Interface System-on-Chip. *IEEE Trans. Biomed. Circuits Syst.* **2019**, *13*, 1736–1746. [CrossRef]

23. Lo, Y.K.; Kuan, Y.C.; Culaclii, S.; Kim, B.; Wang, P.M.; Chang, C.W.; Massachi, J.A.; Zhu, M.; Chen, K.; Gad, P.; et al. A Fully Integrated Wireless SoC for Motor Function Recovery after Spinal Cord Injury. *IEEE Trans. Biomed. Circuits Syst.* **2017**, *11*, 497–509. [CrossRef]

24. Kang, Y.N.; Chou, N.; Jang, J.; Byun, D.; Kang, H.; Moon, D.; Kim, J.; Kim, S. An Intrafascicular Neural Interface With Enhanced Interconnection for Recording of Peripheral Nerve Signals. *IEEE Trans. Neural Syst. Rehabil. Eng.* **2019**, *27*, 1312–1319. [CrossRef]

25. Bonfanti, A.; Ceravolo, M.; Zambra, G.; Gusmeroli, R.; Borghi, T.; Spinelli, A.S.; Lacaita, A.L. A multi-channel low-power IC for neural spike recording with data compression and narrowband 400-MHz MC-FSK wireless transmission. In Proceedings of the ESSCIRC 2010 - 36th European Solid State Circuits Conference, Seville, Spain, 13–17 September 2010; pp. 330–333. [CrossRef]

26. Chae, M.S.; Yang, Z.; Yuce, M.R.; Hoang, L.; Liu, W. A 128-channel 6 mW wireless neural recording IC with spike feature extraction and UWB transmitter. *IEEE Trans. Neural Syst. Rehabil. Eng.* **2009**, *17*, 312–321. [CrossRef]

27. Harrison, R.R. A versatile integrated circuit for the acquisition of biopotentials. In Proceedings of the 2007 IEEE Custom Integrated Circuits Conference, San Jose, CA, USA, 16–19 September 2007; pp. 115–122.

28. Xu, H.; Hirschberg, A.W.; Scholten, K.; Berger, T.W.; Song, D.; Meng, E. Acute in vivo testing of a conformal polymer microelectrode array for multi-region hippocampal recordings. *J. Neural Eng.* **2018**, *15*, 16017. [CrossRef]

29. Liu, X.; Zhang, M.; Xiong, T.; Richardson, A.G.; Lucas, T.H.; Chin, P.S.; Etienne-Cummings, R.; Tran, T.D.; Van der Spiegel, J. A Fully Integrated Wireless Compressed Sensing Neural Signal Acquisition System for Chronic Recording and Brain Machine Interface. *IEEE Trans. Biomed. Circuits Syst.* **2016**, *10*, 874–883. [CrossRef]

30. Versen, M.; Kipfelsberger, S.; Soekmen, F. Model-Based Reference Design Projects with MathWorks' HDL Workflow Advisor for Custom-Specific Electronics with the Zedboard. In *ANALOG 2016; 15. ITG/GMM-Symposium*; VDE: Hong Kong, China, 2016; pp. 1–4.

31. Kang, J.; Yoon, C.; Lee, J.; Kye, S.; Lee, Y.; Chang, J.H.; Kim, G.; Yoo, Y.; Song, T. A System-on-Chip Solution for Point-of-Care Ultrasound Imaging Systems: Architecture and ASIC Implementation. *IEEE Trans. Biomed. Circuits Syst.* **2016**, *10*, 412–423. [CrossRef]

32. Rahane, S.B.; Kureshi, A.K.; Kharate, G.K. OTA-C Filters for Biomedical Signal Processing Applications using Hybrid CMOS-CNFET Technology. In Proceedings of the International Conference on Intelligent and Innovative Computing Applications (ICONIC), Tsim Sha Tsui, Kowloon, 6–7 December 2018; pp. 1–5.

33. Smith, S.W. *The Scientist and Engineer's Guide to Digital Signal Processing*; California Technical Pub.: San Diego, CA, USA, 1997.

34. Greenberg, D.S.; Houweling, A.R.; Kerr, J.N. Population imaging of ongoing neuronal activity in the visual cortex of awake rats. *Nat. Neurosci.* **2008**, *11*, 749–751. [CrossRef]

35. Shahrokhi, F.; Abdelhalim, K.; Serletis, D.; Carlen, P.L.; Genov, R. The 128-channel fully differential digital integrated neural recording and stimulation interface. *IEEE Trans. Biomed. Circuits Syst.* **2010**, *4*, 149–161. [CrossRef]