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Lumped Parameter Modeling Based Power Loop Analysis Technique of Power Circuit Board with Wide Conduction Area for WBG Semiconductors

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Abstract: With the development of wide-bandgap (WBG) power semiconductor technology, such as silicon carbide (SiC) and gallium nitride (GaN), the technology of power converters with high efficiency and high-power density is rapidly developing. However, due to the high rate-of-rise of voltage (dv/dt) and of current (di/dt), compared to conventional Si-based power semiconductor devices, the reliability of the device is greatly affected by the parasitic inductance component in the switching loop. In this paper, we propose a power loop analysis method based on lumped parameter modeling of a power circuit board with a wide conduction area for WBG power semiconductors. The proposed analysis technique is modeled based on lumped parameters, so that power loops with various current paths can be analyzed; thus, the analysis is intuitive, easy to apply and realizes dynamic power loop analysis. Through the proposed analysis technique, it is possible to derive the effective parasitic inductance component for the main points in the power circuit board. The effectiveness of the lumped parameter model is verified through PSpice and Ansys Q3D simulation results.

Keywords: WBG devices; power loop; wide conduction area; lumped parameter modeling; parasitic inductance



Citation: Lee, G.-Y.; Cho, M.-S.; Kim, R.-Y. Lumped Parameter Modeling Based Power Loop Analysis Technique of Power Circuit Board with Wide Conduction Area for WBG Semiconductors. *Electronics* **2021**, *10*, 1722. <https://doi.org/10.3390/electronics10141722>

Academic Editors: Ahmed Abu-Siada and Ali Mehri-Sani

Received: 29 May 2021

Accepted: 16 July 2021

Published: 18 July 2021

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1. Introduction

Power semiconductor devices such as MOSFETs and IGBTs are applied to various power electronics applications as key devices in power converters. Power electronics is a core technology applied to various power levels, from low-power fields of less than 1 kW to high-power fields of hundreds of kW. Accordingly, engineers and consumers in various fields are demanding higher power density and efficiency for power electronics devices. Conventional Si-based power semiconductor devices have continuously developed to meet these demands, but have reached technical and structural limitations [1–3]. Wide-bandgap (WBG) power semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN), which have recently appeared, have excellent material properties; this realizes higher efficiency and power density of power electronics devices through high-speed switching [4–11]. However, WBG devices are significantly affected by parasitic inductance, compared to conventional power semiconductor devices, between switching transitions due to their large rate-of-rise of voltage (dv/dt) and of current (di/dt) [9]. This effect appears in the form of ringing and overshoot of the switching voltage, which causes an increase in the loss of the switching devices and causes damage due to arm-short, in extreme cases [12,13]. Figure 1 is an example of a breakdown of WBG semiconductors by an abnormal switching voltage. Therefore, in order to apply WBG devices to power converters, it is necessary to reduce the unexpected effects of dv/dt and di/dt by reducing parasitic inductance. Therefore, to reduce parasitic inductance, it is important to analyze inductances in the dynamic power loop considering the current distribution for each switching transient [14–17]. If the parasitic inductance is reduced without considering

the dynamic power loop, the effective parasitic inductance that causes ringing and overshoot of switching voltage may not be effectively reduced even though the total parasitic inductance decreases.

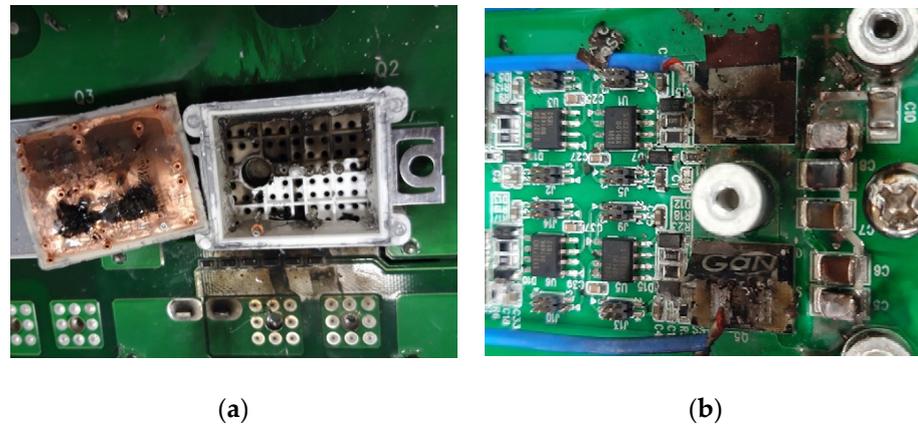


Figure 1. A photograph of burned-out WBG semiconductors by an abnormal switching voltage. (a) SiC MOSFET module. (b) GaN MOSFET.

The finite element method (FEM) is widely used to analyze circuit constants, such as parasitic inductance, existing in a power circuit [18–20]. The FEM is a mathematical technique for numerically solving differential equations in engineering modeling. Generally, FEM requires sufficient mesh division to ensure the high accuracy of circuit constant analysis. However, since the increment of mesh partitioning causes a larger amount of computation, large analysis costs are required. In references [18,19], FEM techniques were introduced to reduce analysis costs while securing the accuracy of analysis of circuit constants through effective mesh division. However, these FEM techniques are point-to-point analysis methods that analyze circuit constants between two limited points and it is difficult to present accurate analysis results for parasitic inductance in the power loop.

Various studies have been conducted to reduce or analyze parasitic inductance in the switching power loop. In reference [21], a vertical lattice loop structure was proposed to reduce parasitic inductance and presented the results of parasitic inductance analysis in a power loop using FEM. After analyzing the power loop to improve the analysis accuracy of the parasitic inductance, the parasitic inductance existing among the main elements in the loop was extracted. However, when analyzing the power loop, only the analysis result for a single static power loop, formed of two power semiconductors and a decoupling capacitor, was presented; thus, the actual effective parasitic inductance was not accurately presented. In addition, for simplified analysis of parasitic inductance, a single current path between major devices is assumed. For this reason, when the power loop is formed with a wide current conduction area, such as a power busbar or a copper plate in a printed circuit board (PCB), the error in the effective parasitic inductance analysis increases due to various current paths among the main elements in the loop. In reference [22], a method of constructing two dynamic power loops formed according to the switching transient was used and the accuracy of the effective parasitic inductance analysis was improved. However, the various current paths between the major devices due to the wide current conduction area were not considered.

In this paper, we propose a power loop analysis method based on lumped parameters that consider various current paths to analyze the effective parasitic inductance in a PCB. The proposed power loop analysis technique analyzes the dynamic power loop formed during switching, then applies FEM, that extracts the parasitic inductance between main devices using Ansys Q3D. In addition, to consider various current paths between main elements in a power circuit having a wide current conduction area, the effective parasitic inductance is extracted by selecting multiple points in which a current can flow. In order to verify the accuracy of the effective parasitic inductance analysis of various current paths,

a PSpice circuit model is constructed based on the extraction results and simulation is performed using a single frequency voltage source. Circuit simulation is performed by constructing a double pulse test (DPT) circuit model, using the extracted effective parasitic inductance to analyze the current distribution in the dynamic power loop of the PCB during switching. Finally, the influence of the effective parasitic inductance through changes in current and magnetic flux during the switching transient period is analyzed. The sequence of the proposed power loop analysis technique is established through a flow-chart and the analysis result for the target PCB is specified.

2. Conventional Power Loop Analysis Techniques

Power loop analysis to analyze the effect of switching voltage due to parasitic inductance generally consists of two processes. The first is the “DPT circuit modeling” process. After selecting a power loop and analyzing the parasitic inductance through FEM, a DPT equivalent circuit including the parasitic inductance is constructed based on the analysis result. The second is the “Power loop analysis” process, which analyzes the influence of parasitic inductance by performing circuit analysis on the DPT circuit constructed in the previous step [14–17,21,22]. The DPT circuit usually consists of a device under test (DUT), WBG MOSFET, diode D_F , inductor L and decoupling capacitor C , as shown in Figure 2. At this time, since L is usually designed to be large enough, it is regarded as a constant current source. If necessary, D_F is sometimes replaced by DUT for analysis of the reverse recovery characteristics. Table 1 shows the description of various parasitic inductance components in the DPT circuit.

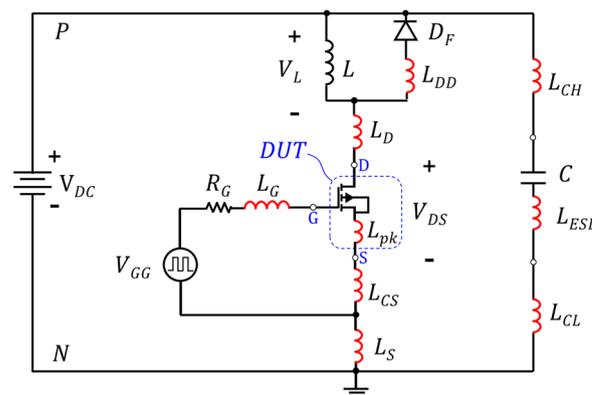


Figure 2. Equivalent circuit of DPT with parasitic inductance.

Table 1. Description of various parasitic inductance components in Figure 1.

Symbol	Description
L_{CH}	Parasitic inductance between C and D_F
L_{CL}	Parasitic inductance between C and node N
L_{ESL}	Equivalent series inductance of C (can be ignored)
L_{DD}	Parasitic inductance between D_F and L
L_D	Parasitic inductance between L and the drain of DUT
L_{pk}	Parasitic inductance in the DUT package
L_{CS}	Common source inductance
L_S	Parasitic inductance between ground of gate-driver and node N
L_G	Parasitic inductance in the loop of gate-driver

Figure 3 shows the static power loop applied in the reference [21]. As shown in the figure, a static power loop consisting of D_F , DUT and C was selected and inductance analysis was performed for L_{CL} , L_{DD} , L_D , L_S and L_{CH} . L_{pk} and L_{CS} were ignored for convenience of analysis. However, such an analysis of parasitic inductance by a static power loop has a problem, in which the current flow during actual switching cannot be

reflected. Therefore, the effective parasitic inductance that affects the switching voltage cannot be accurately analyzed. For example, the vertical lattice loop structure can be properly designed if the current flow from L_{CH} to L_{CL} and the current flow from L_{DD} to L_S have an opposite direction to cause magnetic flux cancellation. After that, if the parasitic inductance is analyzed through FEM, the result of the decreased total parasitic inductance can be carried out. However, the current flow during the actual switching period is generated differently from the static power loop, so that the desired magnetic flux cancellation does not occur suitably. For this reason, even if the vertical lattice loop structure is properly designed, the effective parasitic inductance that causes ringing and overshoot during switching is not effectively reduced.

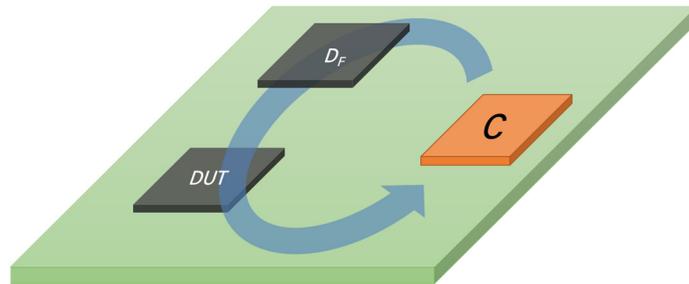


Figure 3. Single static power loop.

Figure 4 shows the dynamic power loop applied in reference [22]. As shown in the figure, each power loop is selected by reflecting the current flow and di/dt formed by the turn-on and turn-off of the DUT. After that, the integrated dynamic power loop is constructed and the parasitic inductance is analyzed to derive a valid analysis result. If the vertical lattice loop structure of [21] is applied based on the dynamic power loop, the current flow is accurately reflected during actual switching, so it is possible to design a vertical lattice loop structure in which a desired magnetic flux cancellation occurs. Therefore, to analyze the effective parasitic inductance that affects the switching, a power loop analysis based on a dynamic power loop is required.

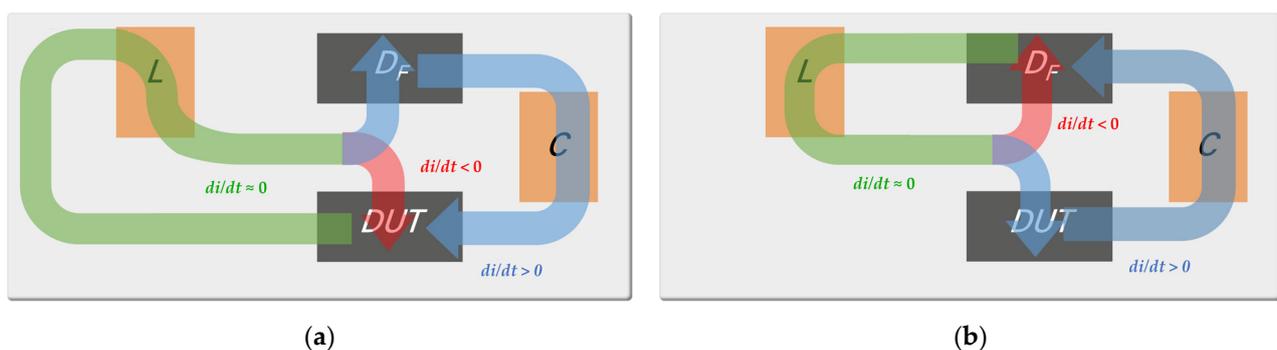


Figure 4. Dynamic power loop. (a) Turn-off path. (b) Turn-on path.

3. Proposed Power Loop Analysis Technique

The power loop analysis technique proposed in this paper includes two pre-processing steps, compared to a conventional technique. The first is the “Multi-node-based lumped parameter modeling” process and the second is the “Model validation”. Figure 5 shows the flow-chart of the proposed technique.

3.1. Step 1—Multi-Node-Based Lumped Parameter Modeling

In Step 1, various current paths in a wide conduction area formed among the main elements are analyzed. Figure 6a–c shows the analysis process at the top layer of the PCB

prototype, where the DPT circuit is implemented. First, as shown in Figure 6a, select a starting point and arrival point where current can be conducted. After that, select points considering all current flow paths to conduct from the starting point to the arrival point. At this time, points are selected to represent the direction of current branched by clearance. Then, as shown in Figure 6b,c, select a point by considering the step-by-step current path. Figure 6d shows the selected points through the process. Figure 7a,b show the same process as the sequence in Figure 6 at the bottom layer of the PCB prototype. Figure 7c shows the selected points through Figure 7a,b.

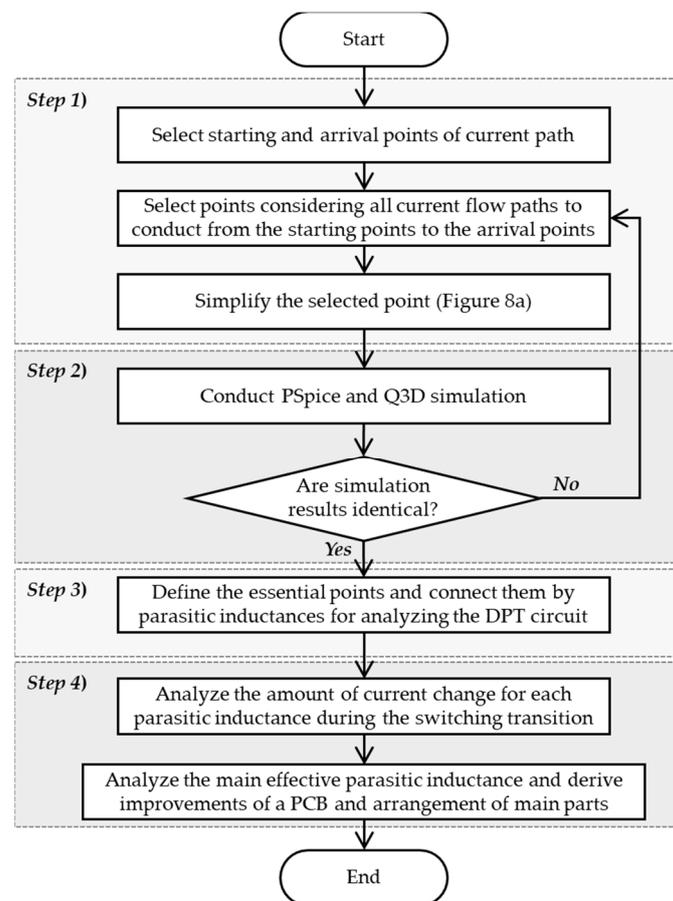


Figure 5. Flow chart of proposed power loop analysis technique.

In the case of the points selected in Figures 6d and 7c, however, dense points exist in the adjacent area. Here, since each point represents the direction of current branched by clearance, it is not efficient to have dense points in adjacent areas. Therefore, if the same current analysis is possible even if an arbitrary point is erased, an efficient result can be obtained by merging the points [9]. Figure 8a shows a method to simplify the selected point. Simplify the three points into one point by connecting adjacent points with a triangle and selecting the midpoint of the triangle as a new point. Select a point that can equally represent the current flowing to each vertex of the triangle and erase it, as shown in Figure 8a. Through this process, the point can be simplified, as shown in Figure 8b,c.

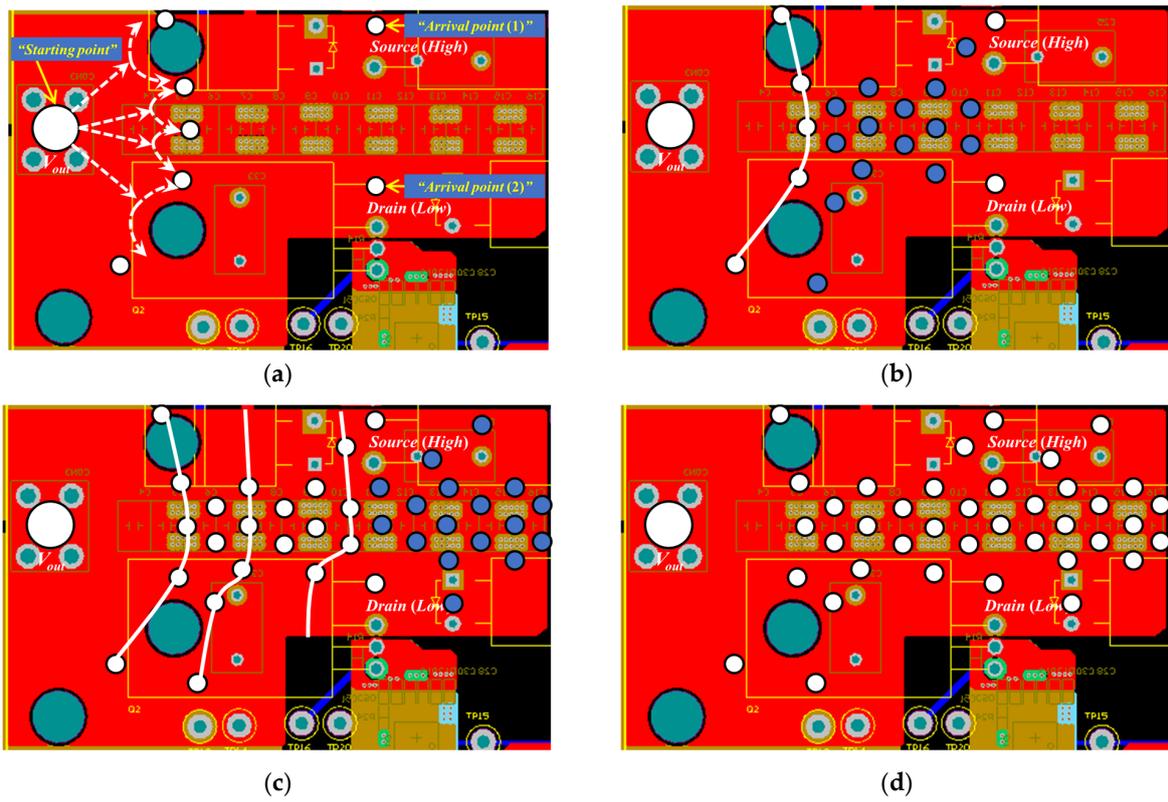


Figure 6. Lumped parameter modeling sequence at top layer. (a) Region 1. (b) Region 2. (c) Region 3. (d) Selected result.

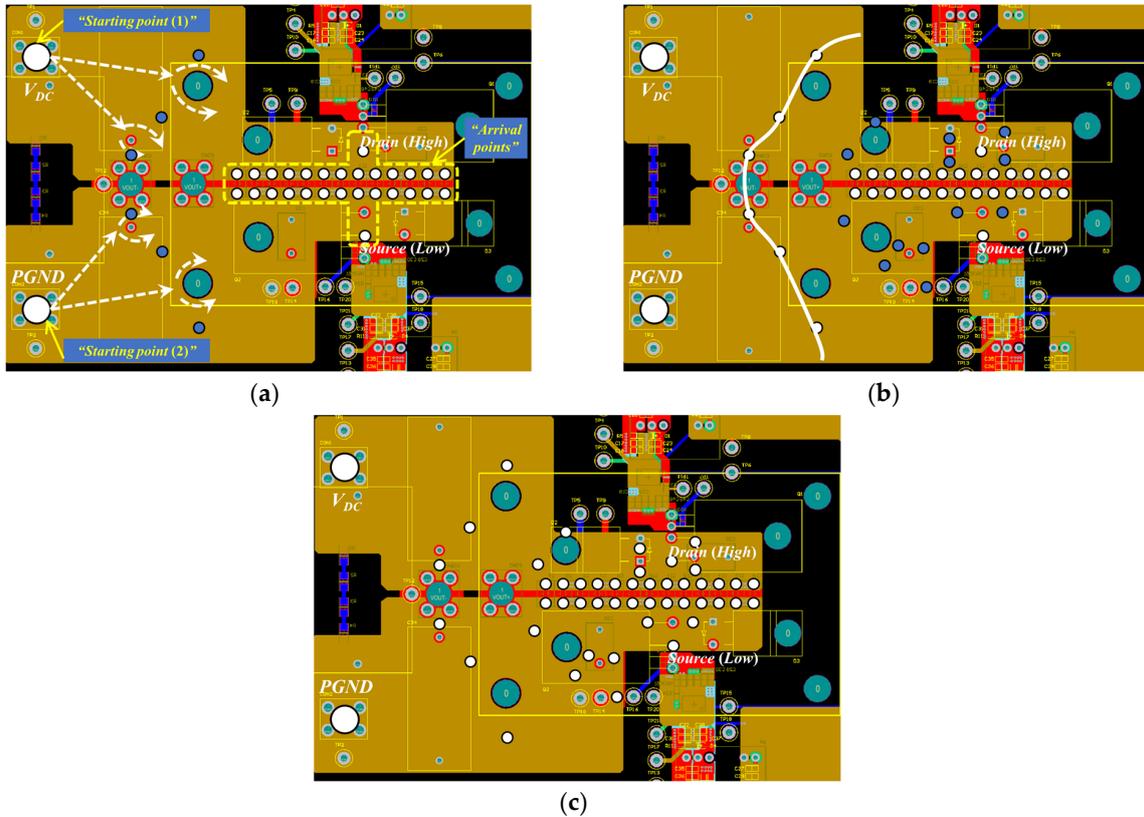


Figure 7. Lumped parameter modeling sequence (bottom layer of target PCB). (a) Region 1. (b) Region 2. (c) Selected result.

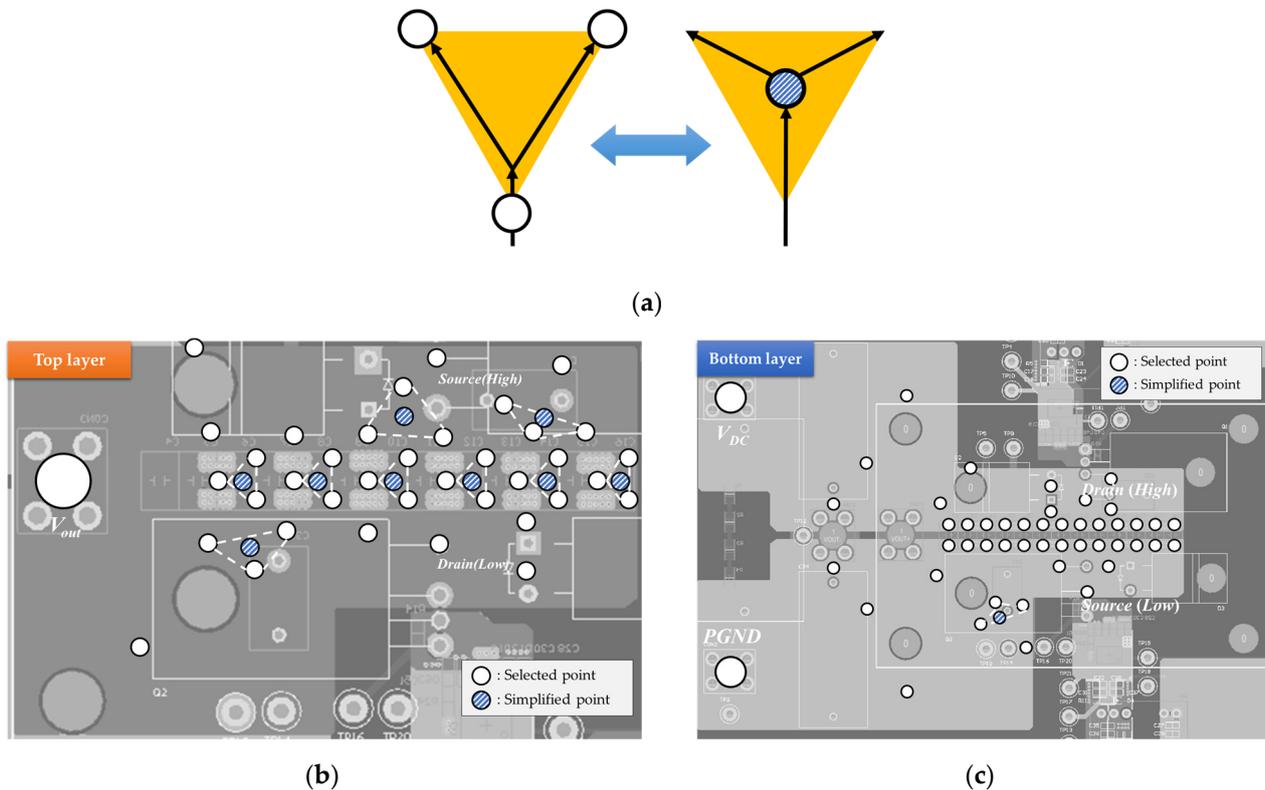


Figure 8. Simplification process of lumped parameter modeling. (a) Simplification method. (b) Simplified point at top layer. (c) Simplified point at bottom layer.

3.2. Step 2—Model Validation

In Step 2, a simulation model is constructed by connecting the simplified point in Figure 8b,c through inductance to validate the lumped parameter model derived in the previous step. The validity of the lumped parameter model is verified through a comparison of PSpice results and Q3D simulation results. In addition, to compare results in the same situation, the PSpice simulation operation conditions are set equal to the Q3D analysis frequency.

Figure 9 shows the current density and current flow extracted through Q3D simulation. Figure 10a shows the circuit in which the point selected in Figure 8b is connected by parasitic inductance. In addition, Figure 10b shows the current magnitude and current direction for each parasitic inductance when the input current applied to Figure 10a is maximized. The input current is a sine waveform and the frequency is 100 MHz. Comparing the results of Figures 9 and 10, it can be confirmed that the current flow and the magnitude are almost identical and, from these results, the feasibility of the modeling of Step 1 can be verified. If the circuit simulation result is not similar to the Q3D simulation result, repeat the point design in Step 1 until the two simulation results are similar.

In the same process, modeling results of the bottom layer are verified. Figure 11 shows the Q3D simulation results at the high and low side of the bottom layer. Figures 12a and 13a are circuit models in which the points in Figure 8c are connected by parasitic inductance. By comparing Figures 11–13, the validity of the modeling results can be confirmed. Through this procedure, the validity of the lumped parameter model for interpreting the parasitic component existing as a distributed constant is verified.

3.3. Step 3—DPT Circuit Modeling

In this step, a DPT circuit modeling process is described using only the essential points for dynamic power loop analysis among the points of the lumped parameter model. Figure 14 shows the essential points for analyzing the DPT circuit among the points in

Figure 8b,c. Here, the essential points mean the points that can represent the current path among the main elements constituting the DPT circuit. Therefore, the erasure of a point should proceed so that only the essential points must remain.

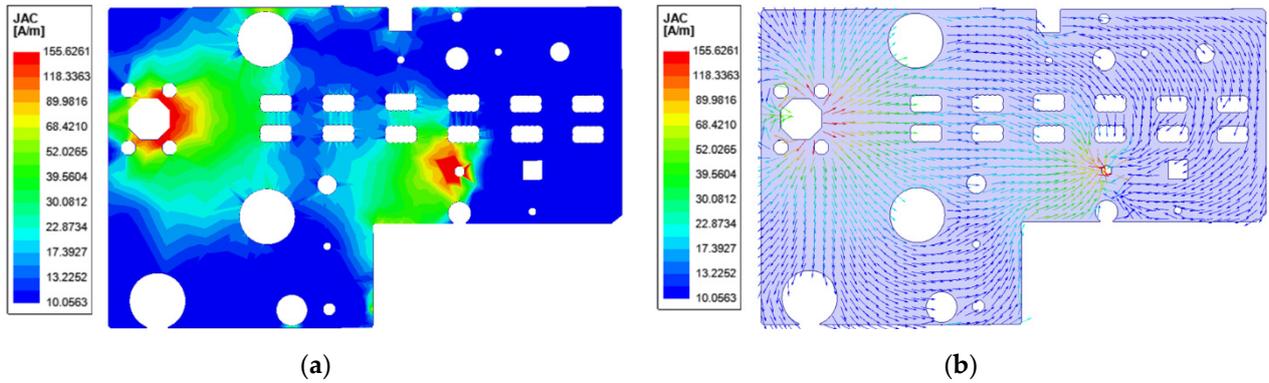


Figure 9. Q3D simulation results at top layer. (a) Current density. (b) Current flow.

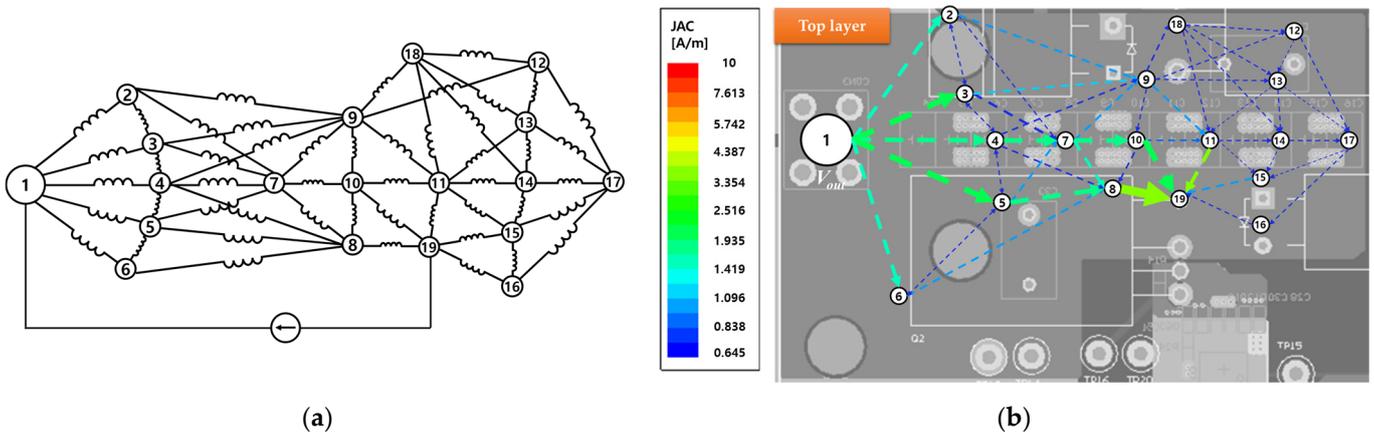


Figure 10. PSpice simulation at top layer. (a) Circuit model. (b) Simulation result.

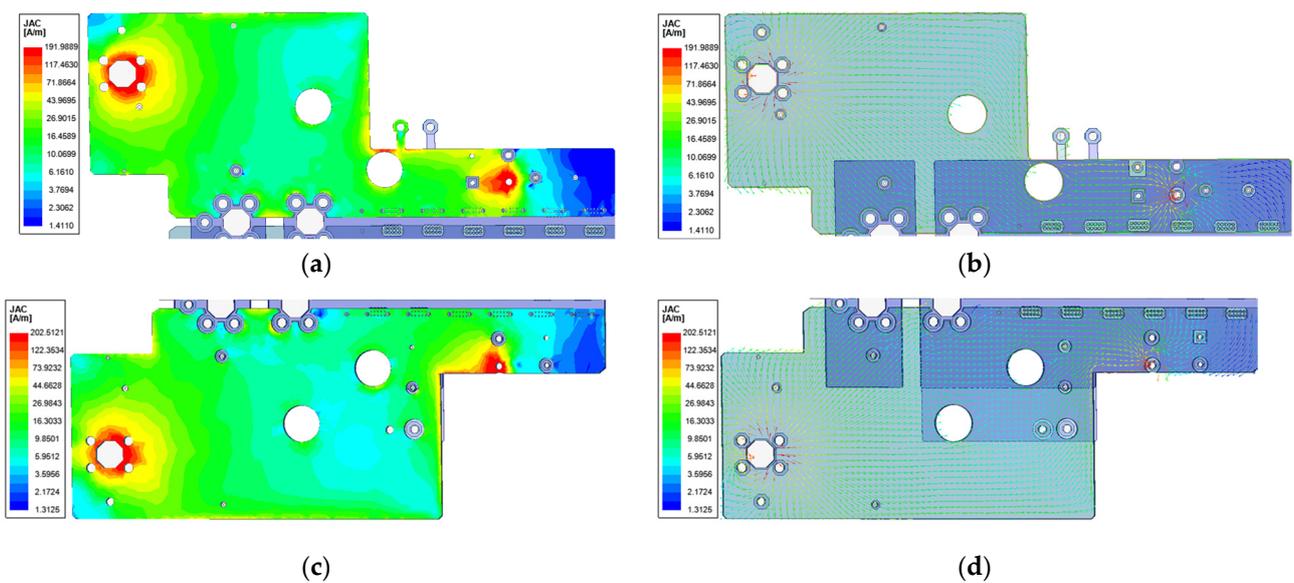
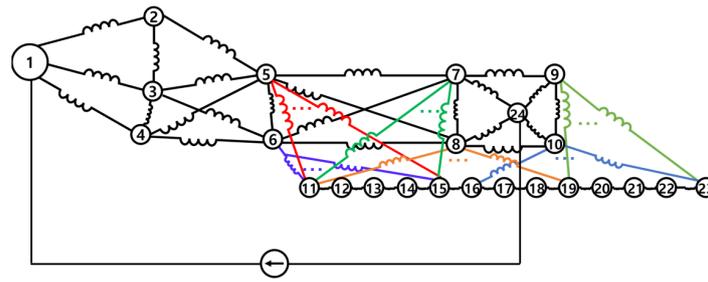
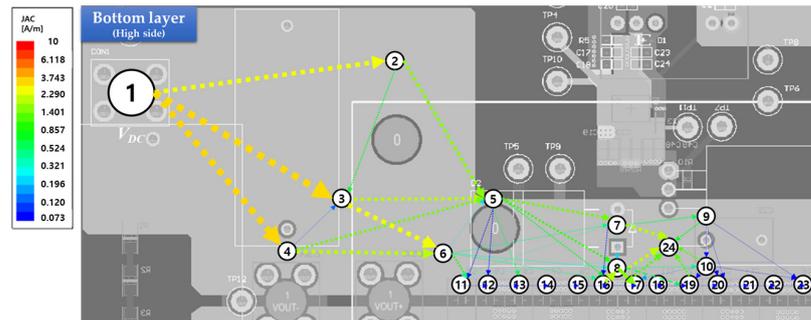


Figure 11. Q3D simulation results at bottom layer. (a) Current density of high side. (b) Current flow of high side. (c) Current density of low side. (d) Current flow of low side.

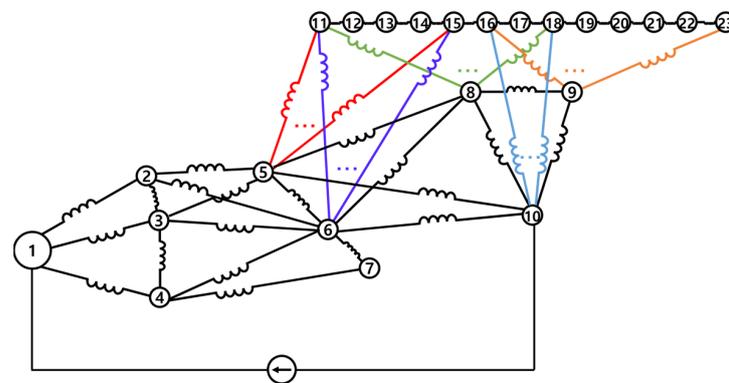


(a)

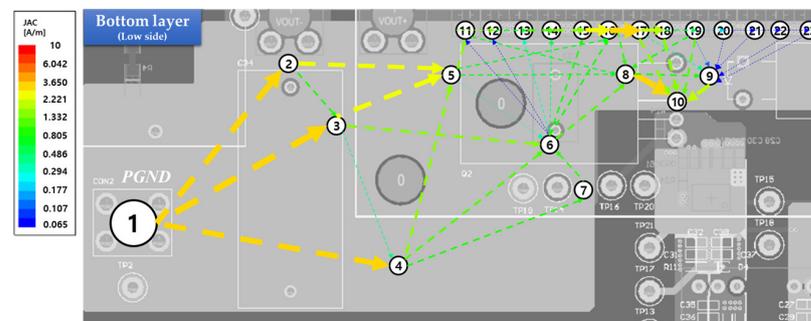


(b)

Figure 12. PSpice simulation at high side of bottom layer. (a) Circuit model. (b) Simulation result.



(a)



(b)

Figure 13. PSpice simulation at low side of bottom layer. (a) Circuit model. (b) Simulation result.

Figure 14a shows essential points that can represent the current path among V_{out} , the

source of the high switch and the drain of the low switch. Among them, the path between V_{out} and the source of the high switch is selected only as the straight line connecting the two points with the shortest distance and the adjacent point. For example, when considering the current path between V_{out} (point 1) and the source of the high switch (point 10), the path from point 1 to point 2, 6 and 10 can reflect most of the current in the upper area of point 2. Figure 15 shows the DPT circuit in which the points in Figure 14 are connected by parasitic inductances. In PSpice simulation, Roam SCT3030AR is used as the switching device, the load inductor is set to 100 μH and the DC voltage is set to 100 V.

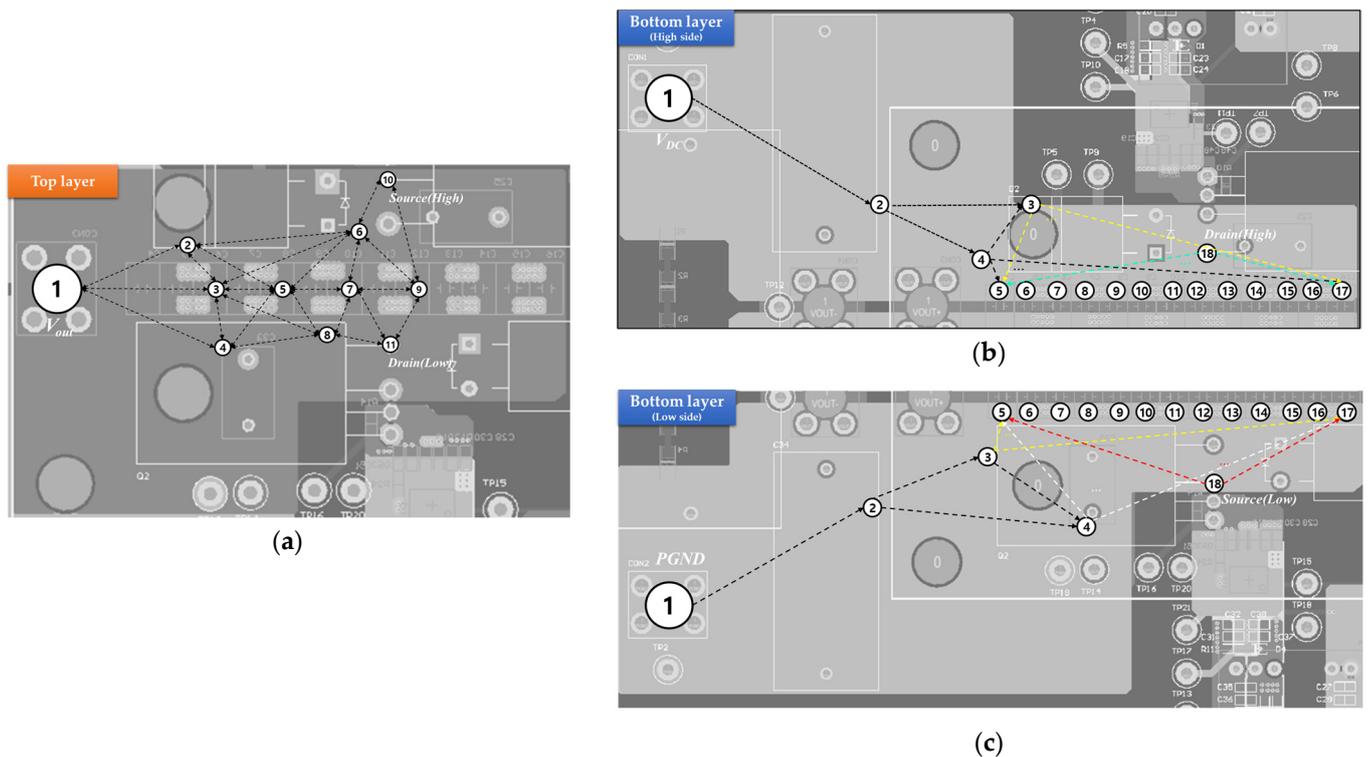


Figure 14. The simplified essential points from Figure 8b,c. (a) Top layer. (b) Bottom layer of high side. (c) Bottom layer of low side.

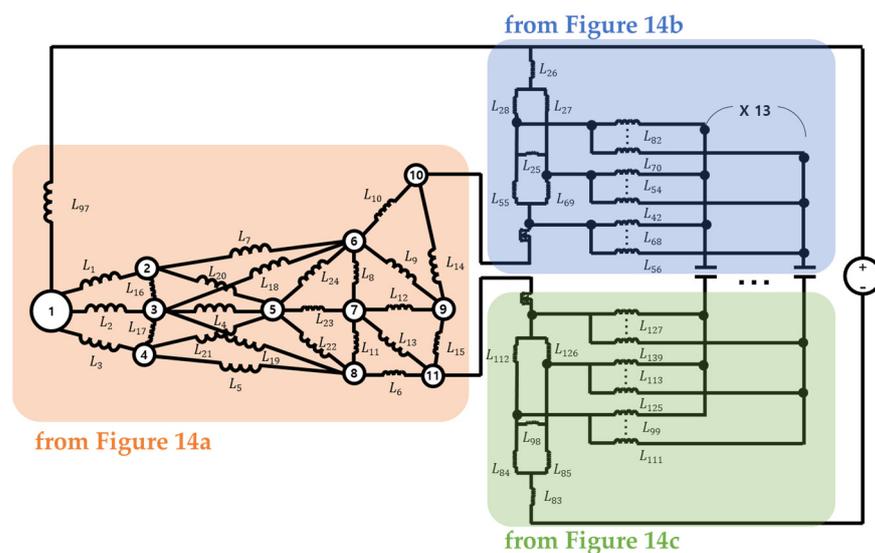


Figure 15. Derived equivalent circuit of DPT circuit.

3.4. Step 4—Dynamic Power Loop Analysis

Finally, in Step 4, the process of analyzing the power loop through the DPT circuit derived in the previous step is performed. Figure 16 shows the lumped parameter-based parasitic inductance model in one conductor. Here, L is the parasitic inductance, I is the current flowing through L and V is the voltage generated by L , corresponding to overshoot and ringing switching voltage. Φ represents the magnetic flux formed by I . V is expressed by Equation (1), according to the Faraday’s law. When the amount of change in magnetic flux, that changes during an arbitrary period, is expressed as $\Delta\Phi$, it can be defined as Equation (2).

$$V = -\frac{d\Phi}{dt} = -L\frac{dI}{dt} \tag{1}$$

$$\Delta\Phi = -L\cdot\Delta I \tag{2}$$

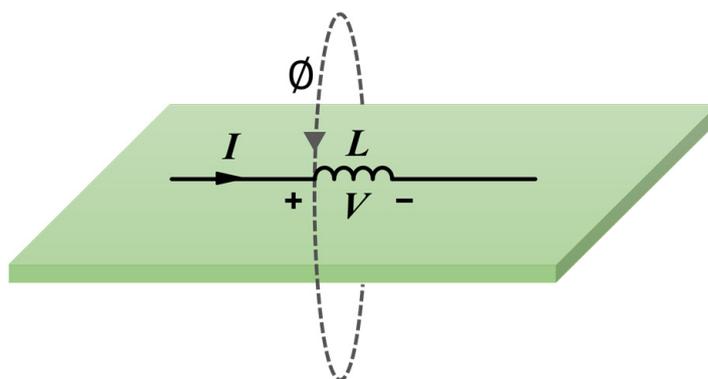


Figure 16. Lumped parameter-based parasitic inductance model.

As shown in Equation (1), the magnitude of V induced by the parasitic inductance is proportional to the amount of instantaneous change in Φ . Therefore, through the amount of $\Delta\Phi$ in Equation (2), it is possible to know how much voltage overshoot and ringing occurs due to the corresponding parasitic inductance during the same switching period. With this relationship, we analyze the power loop in Figure 15, after performing the simulation of the DPT circuit. First, to analyze the power loop, the switching transient period needs to be defined. Figure 17 shows the simulation waveforms of turn-on and turn-off of the low switch. Here, I_L is the load inductor current, $v_{gs,l}$ is the gate-source voltage of the low switch and $i_{d,h}$ and $i_{d,l}$ are the drain currents of the high and low switches, respectively. The switching transient period is defined as the time in which the switch drains current rises and reaches the peak.

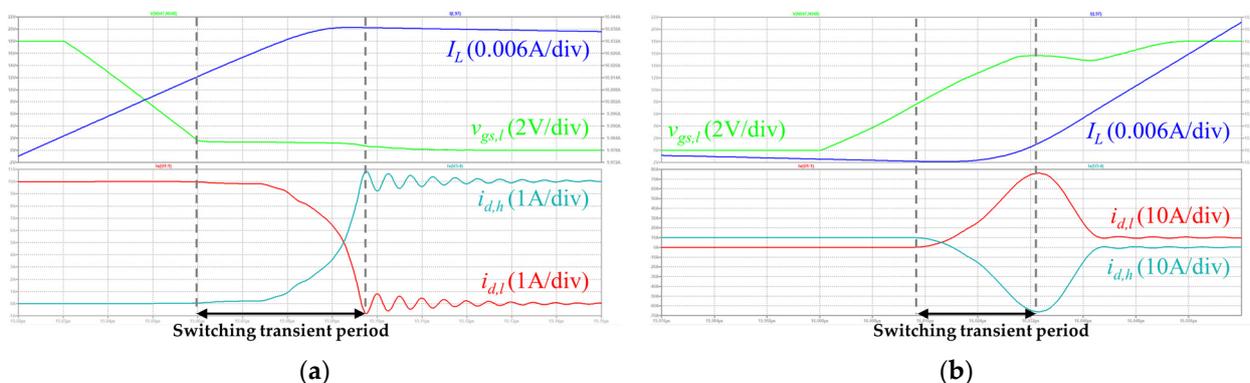


Figure 17. Switching transient waveform. (a) Turn-on. (b) Turn-off.

Next, analyze the amount of current change for each parasitic inductance during the switching transition. Figure 18 shows the current change for each parasitic inductance during the defined switching transient period. At the top layer, the current change is the largest between point 10 and point 11, as shown in Figure 18a,b. At the bottom layer, a relatively large current change is formed between the decoupling capacitor (points 5–17 and 23–35) and the high and low switches (points 18 and 36), as shown in Figure 18c,d. Through this process, it is possible to analyze the most important elements of parasitic inductance that cause overshoot and ringing during the switching transient period.

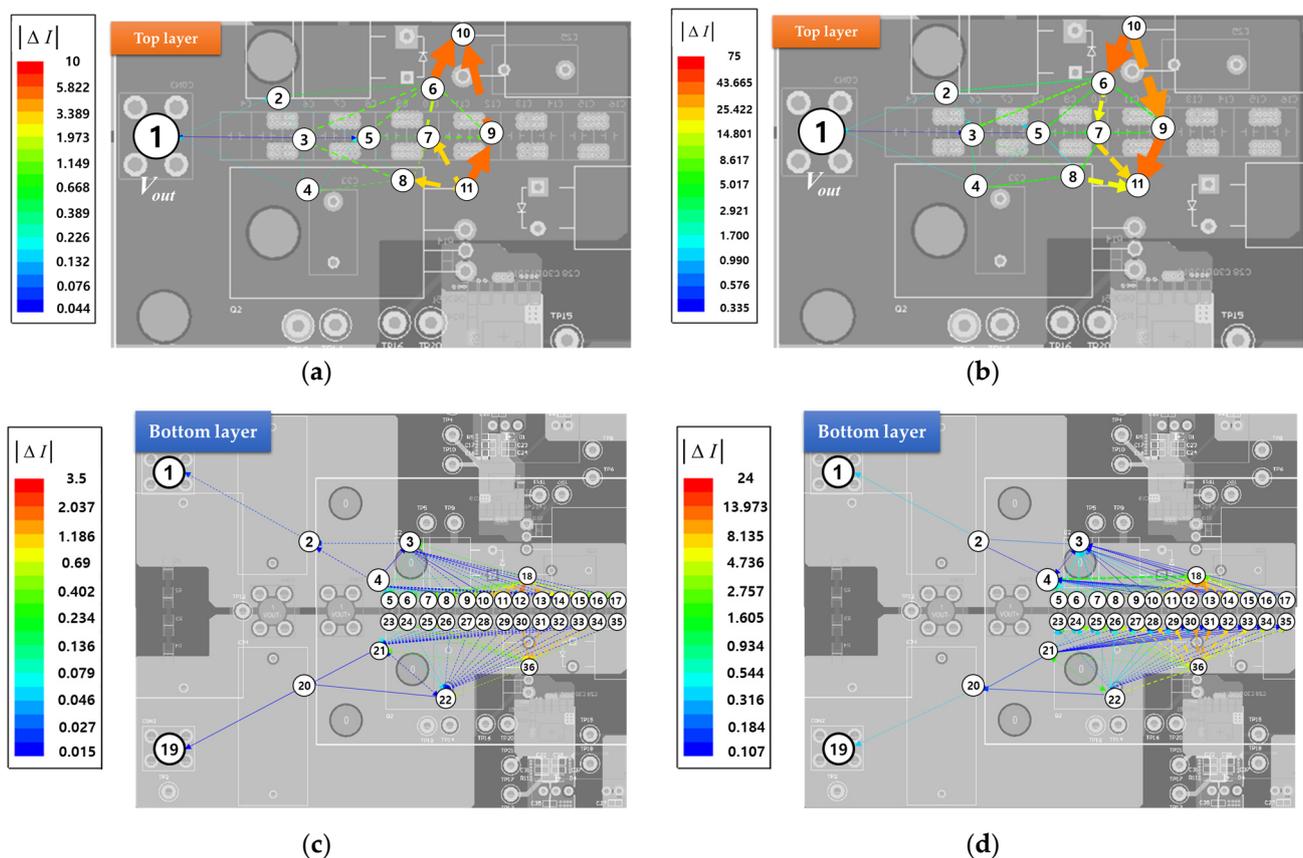


Figure 18. Amount of change in current distribution. (a) Turn-off at top layer. (b) Turn-on at top layer. (c) Turn-off at bottom layer. (d) Turn-on at bottom layer.

4. Analysis Results Based on Proposed Technique

The validity of the power loop analysis technique proposed in this paper is verified through the analysis results. Figure 19 shows the amount of change in the magnetic flux in Equation (2), according to the parasitic inductance component of each layer during turn-on and turn-off switching. Through this result, it is possible to grasp the degree to which the effective parasitic inductance affects voltage overshoot and ringing during switching transitions. For example, in Figure 19a, the effective parasitic inductances L_{14} , L_{10} , L_6 and L_{18} are mainly shown, which means that these effective parasitic inductances are the main factors that cause voltage overshoot and ringing during switching transient. Therefore, it can be seen, from the analysis results, that reducing the effective parasitic inductances on the analyzed main path is most effective in improving voltage overshoot and ringing.

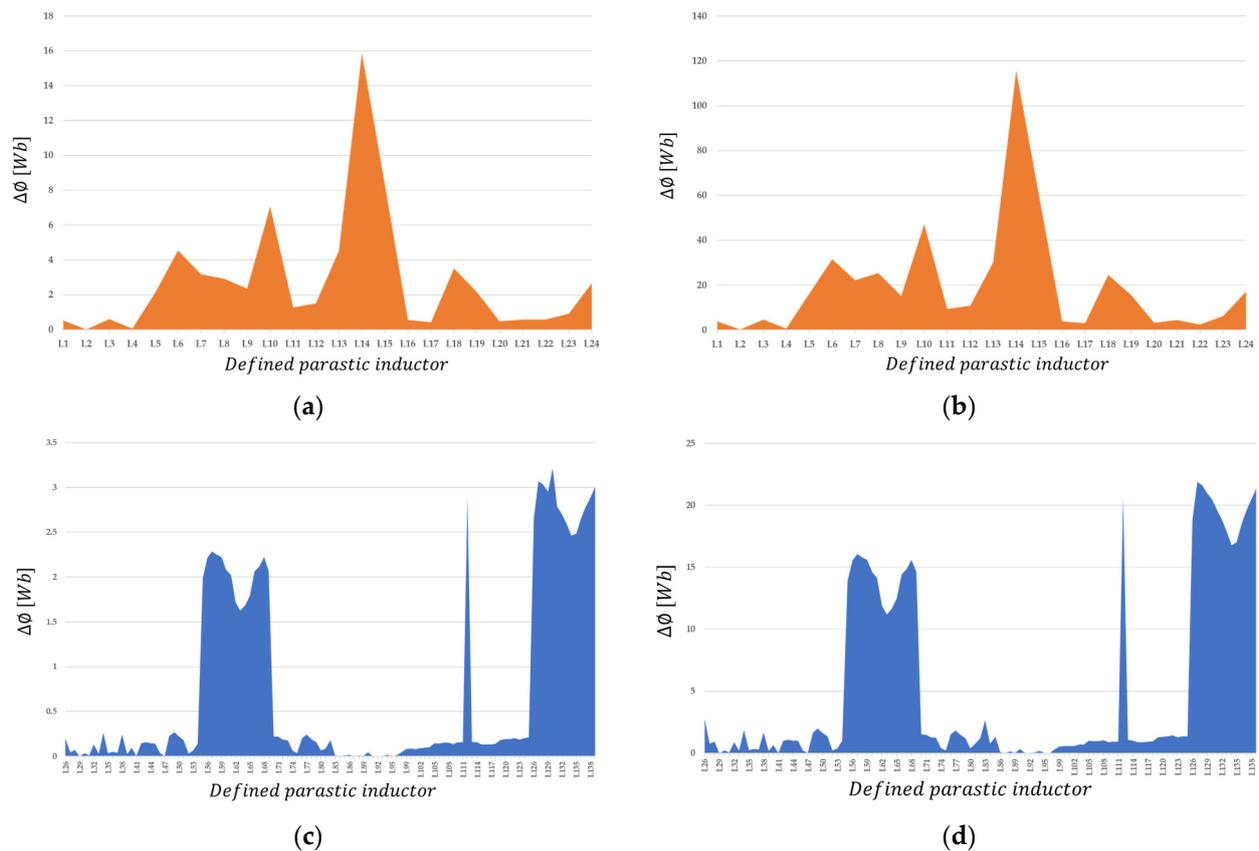


Figure 19. Amount of change in flux analysis. (a) Turn-off at top layer. (b) Turn-on at top layer. (c) Turn-off at bottom layer. (d) Turn-on at bottom layer.

5. Conclusions

In this paper, a lumped parameter-based power loop analysis technique for the effective parasitic inductance analysis of a PCB is proposed. The proposed analysis technique consists of four steps, including a process for considering various current paths among the main elements in a power circuit with a wide current conduction area and a process for analyzing parasitic inductances.

To analyze the effective parasitic inductance, a dynamic power loop was first formed and the parasitic inductance formed among the main elements was extracted. The accuracy of the effective parasitic inductance analysis under various current paths was verified through a comparison between the PSpice and the Q3D results. To analyze the current distribution in the dynamic power loop of the PCB, a DPT circuit simulation model was constructed using the extracted effective parasitic inductance. Finally, the main effective parasitic inductance was analyzed through the amount of change in magnetic flux for each inductance.

The proposed analysis technique can identify various current paths in a PCB with a wide current conduction area. Through this, it is possible to contribute to the provision of guidelines for efficient arrangement and number of decoupling capacitors and effective parasitic inductance reduction.

Author Contributions: Conceptualization, G.-Y.L., M.-S.C. and R.-Y.K.; methodology, G.-Y.L., M.-S.C. and R.-Y.K.; software, M.-S.C.; validation, M.-S.C. and R.-Y.K.; formal analysis, G.-Y.L. and R.-Y.K.; investigation, G.-Y.L.; resources, M.-S.C.; data curation, G.-Y.L. and M.-S.C.; writing—original draft preparation, G.-Y.L. and M.-S.C.; writing—review and editing, G.-Y.L. and R.-Y.K.; visualization, G.-Y.L. and M.-S.C.; supervision, R.-Y.K.; project administration, G.-Y.L. and R.-Y.K.; funding acquisition, G.-Y.L. and R.-Y.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and was granted financial resource by the Ministry of Trade, Industry and Energy, Republic of Korea (No. 2018201010650A), and by the Daejin University Research Grants in 2021.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Baliga, B.J. *Power Semiconductor Devices*, 2nd ed.; PWS Publishing Company: Boston, MA, USA, 1996; p. 373.
2. Cha, K.-H.; Ju, C.-T.; Kim, R.-Y. Analysis and Evaluation of WBG Power Device in High Frequency Induction Heating Application. *Energies* **2020**, *13*, 5351. [[CrossRef](#)]
3. Ma, C.-T.; Gu, Z.-H. Review of GaN HEMT Applications in Power Converters over 500 W. *Electronics* **2019**, *8*, 1401. [[CrossRef](#)]
4. Hudgins, J.L. Power Electronic Devices in the Future. *IEEE J. Emerg. Sel. Top. Power Electron.* **2013**, *1*, 11–17. [[CrossRef](#)]
5. Huang, X.; Lee, F.C.; Li, Q.; Du, W. High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor. *IEEE Trans. Power Electron.* **2016**, *31*, 4343–4352. [[CrossRef](#)]
6. Zhong, X.; Wu, X.; Zhou, W.; Sheng, K. An All-SiC High-Frequency Boost DC–DC Converter Operating at 320 °C Junction Temperature. *IEEE Trans. Power Electron.* **2014**, *29*, 5091–5096. [[CrossRef](#)]
7. Huang, X.; Lee, F.C.; Li, Q.; Du, W. MHz GaN-based interleaved CRM bi-directional buck/boost converter with coupled inductor. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015.
8. Texas Instruments. IGBT & SiC Gate Driver Fundamentals. 2019. Available online: <https://www.ti.com/lit/slyy169> (accessed on 1 January 2019).
9. Lidow, A. *GaN Transistor for Efficient Power Conversion*, 2nd ed.; Wiley: New York, NJ, USA, 2015; ISBN 978-1-118-84478-6.
10. Jadli, U.; Mohd-Yasin, F.; Moghadam, H.A.; Pande, P.; Chaturvedi, M.; Dimitrijević, S. Modeling Power GaN-HEMTs Using Standard MOSFET Equations and Parameters in SPICE. *Electronics* **2021**, *10*, 130. [[CrossRef](#)]
11. Cha, H.-R.; Kim, K.-M.; Song, M.-S.; Kim, R.-Y. PCB-Embedded Spiral Pattern Pick-Up Coil Current Sensor for WBG Devices. *Energies* **2020**, *13*, 5747. [[CrossRef](#)]
12. Kim, U.-J.; Song, M.-S.; Kim, R.-Y. PCB-Based Current Sensor Design for Sensing Switch Current of a Nonmodular GaN Power Semiconductor. *Energies* **2020**, *13*, 5161. [[CrossRef](#)]
13. Martínez, P.J.; Maset, E.; Martín-Holgado, P.; Morilla, Y.; Gilabert, D.; Sanchis-Kilders, E. Impact of Gamma Radiation on Dynamic RDSON Characteristics in AlGaIn/GaN Power HEMTs. *Materials* **2019**, *12*, 2760. [[CrossRef](#)] [[PubMed](#)]
14. Ni, C.; Zhao, Z.; Cui, X. Inductance Calculation Method Based on Induced Voltage. *IEEE Trans. Magn.* **2017**, *53*, 1–4. [[CrossRef](#)]
15. Wang, J.; Chung, H.S.; Li, R.T. Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance. *IEEE Trans. Power Electron.* **2013**, *28*, 573–590. [[CrossRef](#)]
16. Letellier, A.; Dubois, M.R.; Trovão, J.P.F.; Maher, H. Calculation of Printed Circuit Board Power-Loop Stray Inductance in GaN or High di/dt Applications. *IEEE Trans. Power Electron.* **2019**, *34*, 612–623. [[CrossRef](#)]
17. Jørgensen, A.B.; Bęczkowski, S.; Uhrenfeldt, C.; Petersen, N.H.; Jørgensen, S.; Munk-Nielsen, S. A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices. *IEEE Trans. Power Electron.* **2019**, *34*, 2494–2504. [[CrossRef](#)]
18. Reusch, D.; Strydom, J. Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter. *IEEE Trans. Power Electron.* **2014**, *29*, 2008–2015. [[CrossRef](#)]
19. Yang, S.S.; Soh, J.H.; Kim, R.Y. Parasitic Inductance Reduction Design Method of Vertical Lattice Loop Structure for Stable Driving of GaN HEMT. In Proceedings of the IEEE 4th International Future Energy Electronics Conference (IFEEEC), Singapore, 25–28 November 2019.
20. Zhang, Y.; Oo, Z.Z.; Wei, X.; Liu, E.; Fan, J.; Li, E. Systematic Microwave Network Analysis for Multilayer Printed Circuit Boards with Vias and Decoupling Capacitors. *IEEE Trans. Electromagn. Compat.* **2010**, *52*, 401–409. [[CrossRef](#)]
21. Fu, R.; Grekov, A.; Peng, K.; Santi, E. Parasitic modeling for accurate inductive switching simulation of converters using SiC devices. In Proceedings of the IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013.
22. Wu, K.; Shiue, G.; Guo, W.; Lin, C.; Wu, R. Delaunay–Voronoi Modeling of Power-Ground Planes with Source Port Correction. *IEEE Trans. Adv. Packag.* **2008**, *31*, 303–310.