

## Article

# Gate All around with Back Gate NAND Flash Structure for Excellent Reliability Characteristics in Program Operation

Jae-Min Sim <sup>1</sup> , Bong-Seok Kim <sup>1</sup>, In-Ho Nam <sup>1</sup> and Yun-Heub Song <sup>1,2,\*</sup>

<sup>1</sup> Department of Electronics Engineering, Hanyang University, Seoul 04763, Korea; ustin24@hanyang.ac.kr (J.-M.S.); bongseok63@hanyang.ac.kr (B.-S.K.); ihnam@hanyang.ac.kr (I.-H.N.)

<sup>2</sup> PeDiSem Co., Ltd., Seoul 04763, Korea

\* Correspondence: yhsong2008@hanyang.ac.kr; Tel.: +82-2-2220-4136

**Abstract:** A gate all around with back-gate (GAAB) structure was proposed for 3D NAND Flash memory technology. We demonstrated the excellent characteristics of the GAAB NAND structure, especially in the self-boosting operation. Channel potential of GAAB shows a gradual slope compared with a conventional GAA NAND structure, which leads to excellent reliability characteristics in program disturbance, pass disturbance and oxide break down issue. As a result, the GAAB structure is expected to be appropriate for a high stacking structure of future memory structure.

**Keywords:** gate all around with back-gate (GAAB); NAND flash; self-boosting; hot carrier injection (HCI); program disturbance; pass disturbance



**Citation:** Sim, J.-M.; Kim, B.-S.; Nam, I.-H.; Song, Y.-H. Gate All around with Back Gate NAND Flash Structure for Excellent Reliability Characteristics in Program Operation. *Electronics* **2021**, *10*, 1828. <https://doi.org/10.3390/electronics10151828>

Academic Editor: Yahya M. Meziani

Received: 7 July 2021

Accepted: 27 July 2021

Published: 30 July 2021

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## 1. Introduction

In the memory market, 3D NAND flash memory is a mainstream technology that can achieve high bit density by increasing the mold stacking height [1]. Recently, 3D NAND flash has been implemented with approximately 170 stacks and is expected to increase by about 300 layers [2–4].

To continuously increase stacking layers, vertical scaling is inevitable to reduce mold staking height. However, the scaling technology has many problems which must be confronted to solve reliability issues [5–7]. Among them, conventional gate all around (GAA) type 3D NAND structures have insufficient self-boosting efficiency, because hot carrier injection (HCI) is generated by high electric field in the channel region [8]. Additionally, the number of cells suffering from pass disturbance increases as the string length increases [9].

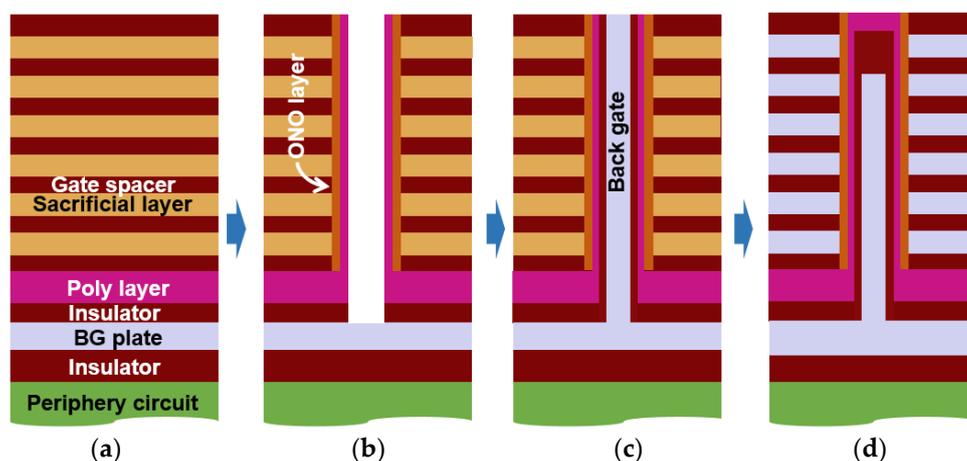
In this situation, most industries try to achieve periphery under circuit architecture to reduce the chip area [3,4]. This structure experienced severe leakage current characteristics during a self-boosting operation [10,11]. As a result, after the periphery circuit process, it is impossible to form single crystalline silicon through selective epitaxial growth (SEG) of the source line for the cell array; therefore, the channel in the ground select line (GSL) area is replaced with poly silicon type, leading to more severe program and pass disturbance. In addition, as the distance between adjacent cells decreases, high electric field generated in the spacer has a significant impact on the reliability.

To solve these issues, we proposed a gate all around with back-gate (GAAB) NAND structure, and attempted to prove excellent reliability compared to the conventional GAA structure using a TCAD simulation.

## 2. GAAB NAND Structure

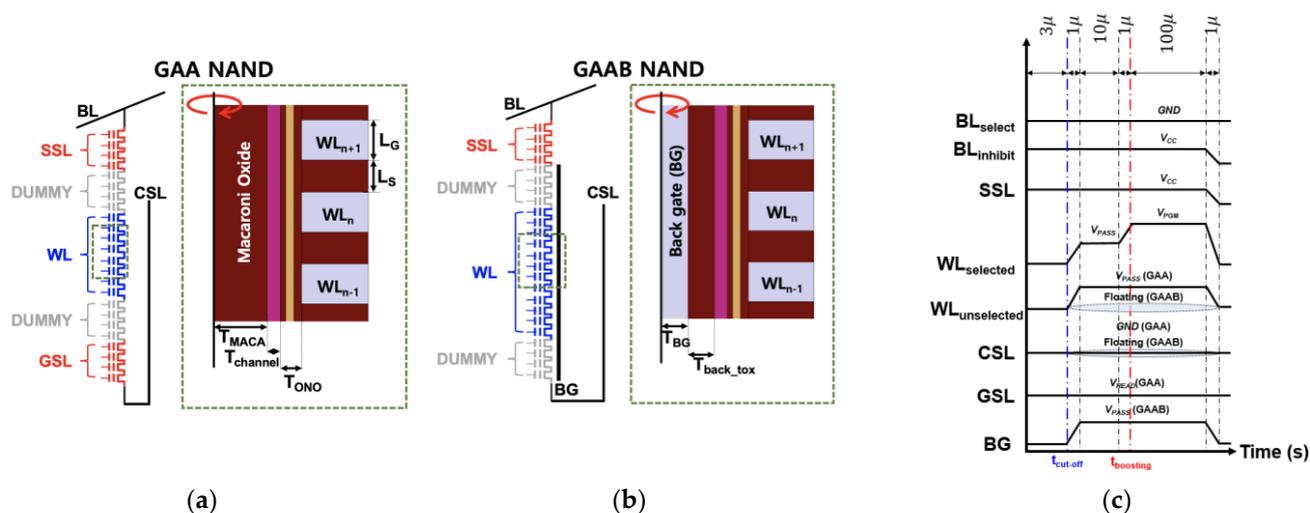
Figure 1 shows the manufacturing process flow of the GAAB structure, which can be realized by a periphery under circuit technology. In the GAA NAND type, a poly layer is formed after the formation of a periphery circuit. On the other hand, in the GAAB type, back-gate (BG) plate and insulator layer are stacked before forming the poly layer. The BG plates are formed in each block. Then, additional processes include etching

the poly layer after poly-silicon channel formation and filling the BG material inside a hole after BG dielectric film deposition. These processes are the most critical steps in manufacturing the GAAB structure. Therefore, advanced etching and filling technologies are required for better feasibility. Nevertheless, the GAAB structure shows advantages in program operation.



**Figure 1.** GAAB fabrication flow. (a) BG plate formation before substrate deposition; (b) channel-hole etching and ONO, poly-channel deposition; (c) BG dielectric and BG formation; (d) BG recess and channel capping.

Figure 2a,b show the schematic and cross-section of the GAA and GAAB NAND structures. Compared with the conventional GAA type, GAAB shares the BG across all memory cells. Moreover, GSL transistors are not included in the GAAB structure. The operation scheme was examined in comparison with a conventional GAA structure. Both structures have 32 word-lines (WLs), and GAA uses 4 String select line (SSL)/GSL transistors while GAAB only uses SSL. The design parameters of the gate length, space length, and O/N/O thickness are 25 nm, 20 nm, and 4/6/6 nm, respectively. The macaroni oxide thickness ( $T_{MACA}$ ) in the GAA structure is 40 nm, and both the back gate oxide thickness ( $T_{back\_tox}$ ) and back-gate thickness ( $T_{BG}$ ) are 20 nm in GAAB. The channel thickness is 10 nm for both structures. Lastly, the selected word-line is WL16, which is the center of the string.



**Figure 2.** Schematics and cross-sections of 3D NAND flash memory: (a) Conventional GAA NAND and (b) Proposed GAAB NAND. (c) Timing diagram of program scheme in the GAAB NAND flash memory ( $V_{CC}$ : 3 V,  $V_{PGM}$ : 20 V,  $V_{PASS}$ : 9 V (standard), 12 V, 15 V).

In the TCAD simulation-based study, we used the recombination model using the doping dependence of the SRH (Shockley–Read–Hall) lifetime model and band-to-band model. In addition, all simulation results are performed by cylindrical computation based on the cross-sections structure of Figure 2a,b.

### 3. Self-Boosting Scheme of GAAB NAND

Figure 2c shows the program operation in selected bit line (BL) and inhibited BL. In the program operation, NAND flash array is controlled by each BL and SSL bias condition [12]. Therefore, channel potential of the inhibited BL must be increased by a self-boosting scheme to prevent program disturbance. Alternatively, the channel potential of the selected BL must be grounded to maximize the electric field between WL and channel. In the case of a conventional self-boosting scheme, SSL and GSL channel regions must make the cut-off state by applying  $V_{CC}$  bias, which leads to a floating state in inhibited channel potential at  $t_{cut-off}$ . After this,  $V_{PASS}$  and  $V_{PGM}$  bias to the unselected and selected WLs can increase the floating state channel potential at  $t_{boosting}$ .

Compared with the conventional program scheme, program operation of the GAAB NAND structure uses BG bias to increase channel potential. Therefore, unselected WLs are in the floating state, and the pass voltage ( $V_{PASS}$ ) is applied to the back gate instead. Common source line (CSL) is also in a floating state as the unselected WL. In this scheme, we observed  $t_{boosting}$  when the selected WL is applied in the  $V_{PGM}$ .

Figure 3 shows the channel potential of GAA and GAAB NAND structures in the inhibited BL and electrostatic potential at each region at  $t_{boosting}$ . The channel potential characteristics of GAA NAND shows the general self-boosting effect [13]. Therefore, the potential difference between the selected WL and unselected WL is abruptly increased.

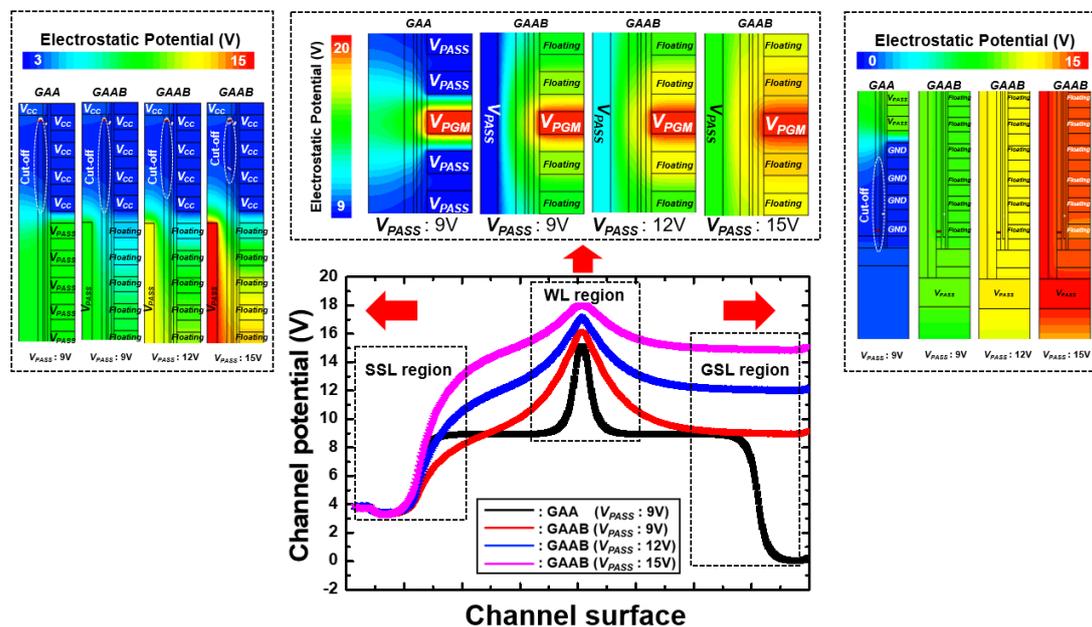


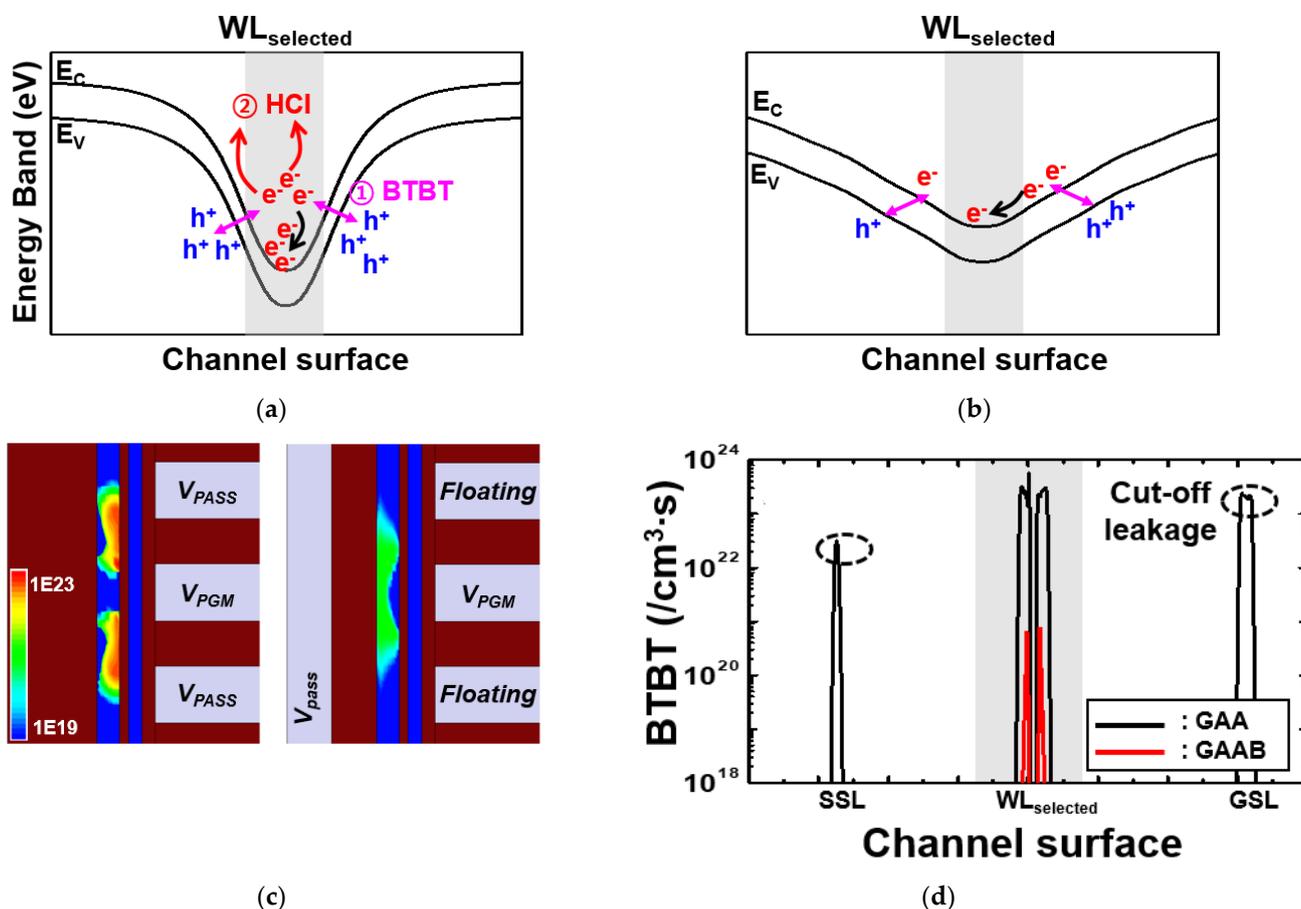
Figure 3. Inhibited channel potential in GAA and GAAB NAND structure at  $t_{Boosting}$  and electrostatic potential at each region.

However, the GAAB structure shows a gradual profile of channel potential since the unselected WLs are in a floating state. Additionally, the channel potential can be easily increased by increasing the  $V_{PASS}$  without considering the pass disturbance. Therefore, the  $V_{PASS}$  of the unselected WL can be completely replaced by applying  $V_{PASS}$  to the back gate in the GAAB NAND. Furthermore, we also confirmed that GAAB NAND strings achieve self-boosting behavior without GSL transistors. Although both GAA and GAAB have the same cut-off operation in the SSL region, in the case of the GSL region, GAAB

does not need GSL—unlike GAA—because GSL is not required due to back gate bias under the poly layer. Since the 3D NAND flash technologies use the poly-silicon channel of SSL and GSL transistors, the leakage characteristics must be carefully considered. However, we confirmed that the GAAB structure can achieve program operation without a GSL transistor. It will be an advantage for reducing the burden on the manufacturing process and circuit operation.

#### 4. Reliability Characteristics

In this chapter, we investigated reliability characteristics of the GAAB NAND structure compared with GAA. We focused on program disturbance and pass disturbance. The program disturbance occurs in the inhibited BL. Figure 4a shows the energy band diagram of the GAA structure. Since the energy band near the selected WL is steep, band-to-band tunneling (BTBT) generation may occur. The generated electrons are likely to cause HCI due to a high electric field.



**Figure 4.** Simulation result of the inhibited BL band diagram at  $t_{boosting}$ . (a) GAA, (b) GAAB NAND structure and constant BTBT generation contours. (c) GAA and GAAB NAND structure. (d) BTBT generation in the inhibited BL from GSL to SSL.

Alternatively, Figure 4b shows that the GAAB band diagram is a very gradual slope, which is expected to have significantly less BTBT generation compared with the GAA structure. As a result, Figure 4c,d show a simulated result of BTBT generation. The GAAB structure has significantly lower BTBT generation than that of the GAA structure. In addition, Figure 4e shows BTBT generation occurring in the inhibited BL channel. In the GAA structure, BTBT generation is also high in the SSL and GSL transistor areas, which is caused by the potential difference between unselected WL and cut-off region in SSL and GSL as shown in Figure 3b. On the other hand, BTBT generation hardly occurs on SSL

and GSL in the GAAB structure due to the gradual channel potential slope with the cut-off region of the SSL channel area.

Figure 5a shows the electric field in the nitride trap layer. Even if  $V_{PASS}$  increases, the electric field in the selected WL, SSL, and GSL region is lower in the GAAB structure than in the GAA structure. The high electric field in the trap layer can also affect the retention characteristic of trapped charge. Therefore, we confirmed that the GAAB structure has significant immunity to program disturbance.

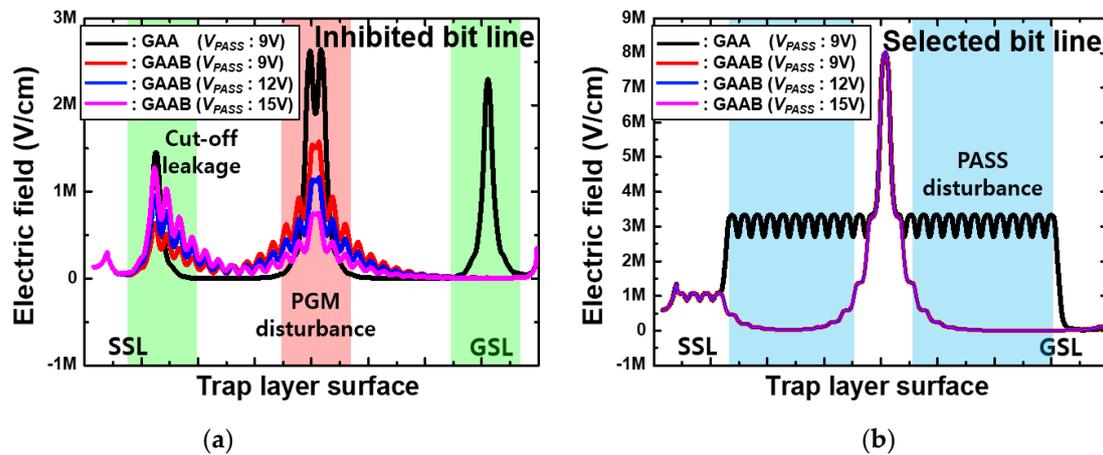


Figure 5. Electric field at  $t_{boosting}$  in the nitride trap layer surface region of the NAND structure. (a) Inhibited BL and (b) selected BL.

Figure 6 shows the electric field contour in inhibited BL. During program operation, the potential difference between selected WL ( $V_{PGM} = 20$  V) and unselected WLs ( $V_{PASS} = 9$  V) is critical for the break down issue, as shown in Figure 6a. However, the GAAB structure provides more immunity to breakdown because the floating state of unselected WL can be maintained at a relatively lower electric field than the GAA structure due to the gradual potential distribution between WLs, as shown in Figure 6b.

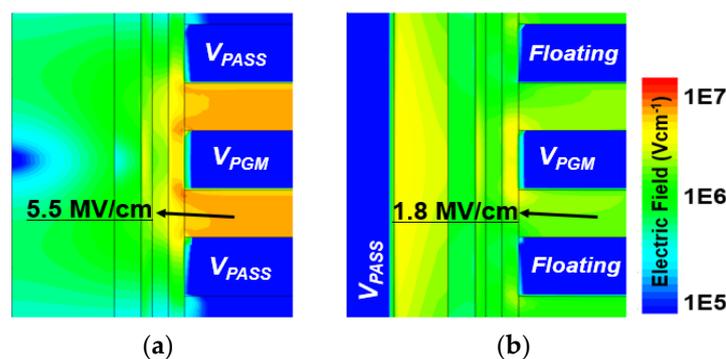


Figure 6. Electric field contour at  $t_{boosting}$  in inhibited BL. (a) GAA and (b) GAAB NAND structure.

Considering all the advantages investigated above, the GAAB NAND has a number of advantages for high stacking and vertical shrinkage structures.

### 5. Conclusions

A gate all around with back-gate (GAAB) structure was proposed for 3D NAND flash memory technology. Excellent characteristics of the proposed structure were demonstrated by a self-boosting scheme using back gate bias. It provides a highly gradual channel profile, which leads to high immunity of program disturbance, pass disturbance and overcoming of the field breakdown between WLs. These advantages of the GAAB structure can lead

to a significant increase in the number of cells by scaling down and better reliability characteristics.

**Author Contributions:** Methodology, paper writing, investigation, conceptualization, Validation, writing, investigation, J.-M.S. Review, B.-S.K. and I.-H.N. Funding acquisition, supervision, editing, Y.-H.S. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was supported by PeDiSem Co., Ltd.

**Conflicts of Interest:** The authors declare no conflict of interest.

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