An Enhanced H-Bridge Multilevel Inverter with Reduced THD, Conduction, and Switching Losses Using Sinusoidal Tracking Algorithm

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Abstract: In this paper, an enhanced H-Bridge multilevel inverter is proposed with the sinusoidal tracking algorithm. The proposed multilevel inverter (MLI) consists of two half H-Bridges cascaded with two unidirectional switches, n direct current (DC) sources, and (n-2) number of bi-directional switches together to form an enhanced H-Bridge (EHB) multilevel inverter. The output voltage levels of an EHB MLI depends on the number of DC sources, the number of bi-directional switches, and the relationship between the magnitude of left-side and right-side DC sources. With the addition of DC sources, bidirectional switches, and employing the sinusoidal tracking algorithm, the performance of the inverter is enhanced with features like an increased number of levels and a reduction in the total harmonic distortion and switching losses. In all the modes of operation of the proposed inverter, only three switches are “ON”, so that conduction losses are less. The proposed enhanced H-Bridge MLI is simulated using MATLAB/Simulink R2017a, and is verified with the experimental result.

Keywords: power electronics; conduction and switching losses; THD (total harmonic distortion); multilevel Inverter; sinusoidal tracking algorithm

1. Introduction

In recent years, multilevel inverters have become popular because of their competence for carrying high power, high voltage, good power quality, lower order harmonics, lower switching losses, and lower electromagnetic interference, due to the absence of an inductor and a capacitor [1–3]. Multilevel inverters generate close to sinusoidal voltages, as in the form of a stepped voltage waveform, using many direct current (DC) voltage sources. In a multilevel inverter, increasing the number of output voltage levels results in lower THD at the output voltage. There are three kinds of multilevel inverter structures: diode-clamped, flying capacitor, and cascaded H-Bridge (CHB). To produce higher levels, the flying capacitor and diode-clamped topologies use many capacitors and diodes, respectively. Also, both of the structures suffer from voltage inequality of capacitors [4–8]. The CHB topology can be suitable to generate higher voltage levels, because it requires fewer components compared to the conventional topologies [1,2]. CHB inverters can increase the number of output voltage levels by increasing the number of H-Bridges used, which increases the number of switching devices used; this makes a multilevel inverter more complicated. Modifications to the H-Bridge inverter topology reduces the number of components. A bi-directional switch is added in the conventional H-Bridge to get two additional voltage levels via a capacitor from a single DC voltage source, and final output is a stepped five-level output voltage [9–14]. A series and parallel connection of DC voltage...
sources cascaded with a conventional H-Bridge gives a stepped output with the reduced harmonics content in the output voltage [15,16]. Series connections of sub-multilevel, half-bridge symmetrical and asymmetrical inverters generate 13 and 31 levels, respectively, when cascaded to an H-Bridge inverter, in this topology six switches are “ON” in all the modes of operation [17,18]. Two half-bridges are cascaded by adding two unidirectional switches, and this forms the seven-level inverter [19]. The cascading of two units of developed H-Bridges produces 49 output voltage levels, but in all the modes of operation, six switches are in the “ON” state [20]. Two cascaded half H-Bridges are nested to form a single unit. One half-bridge inverter and two units of the nested cascaded half H-Bridges are connected in series with the H-Bridge inverter to generate 15 levels, and comprised of 16 switches and seven DC sources. In this topology, a minimum of five switches and a maximum of nine switches are in the “ON” state [21]. Most of the inverters use pulse width modulation method to generate the switching pulses; due to this, the switching losses are very high, especially in high-voltage and high-power multilevel inverters. Frequent high-voltage switching generates more heat, due to power losses in the switches, so reference frequency switching is best to minimize the switching losses [22]. A new multilevel inverter based on modified H-Bridge topology generates a 13-level stepped output, and uses the capacitor to generate the in-between levels, but voltage balancing of the capacitor is difficult and bulky under various loaded conditions [23]. The proposed topology consists of a left-side half H-Bridge inverter with q number of DC sources, (q − 1) number of bidirectional switches, and similarly the right-side half H-Bridge inverter with r number of DC sources, (r − 1) number of bidirectional switches. Finally, these two half H-Bridges cascaded with two unidirectional (S_X, S_Y) switches, as shown in Figure 1. In the proposed enhanced H-Bridge (EHB) multilevel inverter (MLI), in all the modes of operation, only three switches are “ON”, and a reference frequency switching method is used so that the conduction losses and switching losses are minimal. In this proposed topology, there is no storage element like an inductor, and hence the losses are minimized. In this paper, to enhance the performance of the base unit and to reduce the THD, a choice of bidirectional switches and DC sources on both sides with two different methods and a sinusoidal tracking algorithm is proposed, with simulated and experimental results. This EHB MLI is suitable for medium-voltage applications and also used in v/f control drives.

2. Proposed Enhanced H-Bridge Multilevel Inverter

A single-phase, general enhanced H-Bridge multilevel inverter is shown in Figure 1. This general enhanced H-Bridge multilevel inverter consists of (q − 1) and (r − 1) number of bi-directional switches, q number of voltage sources on the left side, and r number of voltage sources on the right side are embedded to form a developed H-Bridge multilevel inverter. The developed H-Bridge consists of six unidirectional power switches (S_1, S_2, S_3, S_4, S_X, and S_Y). The number of output voltage levels of an enhanced H-Bridge multilevel inverter depends on the number of DC voltage sources, bi-directional switches, and the relation between left- and right-side voltage sources.

If the enhanced H-Bridge inverter has two voltage sources (V_P1, V_P2) in the left side and two voltage sources (V_N1, V_N2) on the right side, and the number of bi-directional switches on the left side is one (2 − 1), and the number on the right side is one (2 − 1; q = 2 and r = 2), along with the regular six unidirectional switches. Since the number of bidirectional switches is the same on both sides, it is a symmetrical structure enhanced H-Bridge (SSEHB) multilevel inverter, as shown in Figure 2.

Suppose the enhanced H-Bridge inverter has two voltage sources (V_P1, V_P2) in the left side and three voltage sources (V_N1, V_N2, V_N3) on the right side and hence the number of bi-directional switches on the left side is one (2 − 1), and on right side is two (3 − 1; q = 2 and r = 3), along with the regular six unidirectional switches. Since the number of bidirectional switches is not equal on both sides, it is an asymmetrical structure enhanced H-Bridge (ASEHB) multilevel inverter, as shown in Figure 3.
3. DC Voltage Source Selection Methods

The general enhanced H-Bridge consists of \((q - 1)\) bi-directional switches \((S_{p1}, S_{p2}, S_{p3} \ldots S_{p(q-1)})\) on the left side, \((r - 1)\) bi-directional switches \((S_{n1}, S_{n2}, S_{n3} \ldots S_{n(r-1)})\) on the right side, and six unidirectional power switches, \((S_1, S_2, S_3, S_4, S_X, \text{ and } S_Y)\) are available in the developed H-Bridge.
inverter. The proposed topology as shown in Figure 1 contains q number of voltage sources (V_{P1}, V_{P2}, V_{P3} ... V_{Pq}) and r number of voltage sources (V_{N1}, V_{N2}, V_{N3} ... V_{Nr}) in the left and right side, respectively. Based on the relationship between left- and right-side voltage sources, two methods are proposed here.

**Method I**

There are q number of voltage sources (V_{P1}, V_{P2}, V_{P3} ... V_{Pq}) in the left side, and are equal in magnitude.

V_{P1} = V_{P2} = V_{P3} = ... = V_{Pq}  \quad (1)

where q = 1, 2, 3 ... C

There are r number of voltage sources (V_{N1}, V_{N2}, V_{N3} ... V_{Nr}) in the right side, and are equal in magnitude.

V_{N1} = V_{N2} = V_{N3} = ... = V_{Nr}  \quad (2)

where r = 1, 2, 3 ... D

Equations (3) and (4) specify the difference in magnitude between the left and right side voltage sources when Method I is applied.

V_{P1} = V_{P2} = V_{P3} = ... = V_{Pq} = V_{DC}  \quad (3)

V_{N1} = V_{N2} = V_{N3} = ... = V_{Nr} = (q) \cdot V_{DC}  \quad (4)

**Method II**

V_{P1} = V_{P2} = V_{P3} = ... = V_{Pq}  \quad (5)

V_{N1} = V_{N2} = V_{N3} = ... = V_{Nr}  \quad (6)

Equations (7) and (8) specify the difference in magnitude between the left and right side voltage sources when Method II is applied.

V_{P1} = V_{P2} = V_{P3} = ... = V_{Pq} = V_{DC}  \quad (7)

V_{N1} = V_{N2} = V_{N3} = ... = V_{Nr} = (q + 1) \cdot V_{DC}  \quad (8)

**Method I Example**

In SSEHB, the equal number of bidirectional switches on both sides is

(q - 1) = (r - 1) = n  \quad (9)

In the SSEHB topology, the number of output voltage levels (N_{Level}) is

N_{Level} = (n + 1)^2 + (n + 2)^2  \quad (10)

If n = 1, N_{Level} = (1 + 1)^2 + (1 + 2)^2 = 13.

If n = 2, N_{Level} = (2 + 1)^2 + (2 + 2)^2 = 25.

The number of uni-directional switches is

N_{Uni} = 6  \quad (11)

The number of bi-directional switches is

N_{Bi} = 2n  \quad (12)
The number of dc voltage sources

\[ N_{DC} = 2(n + 1) \]  

(13)

The maximum and minimum magnitude of the generated output voltage is

\[ V_{O,\text{Max}} = \sum_{q = 1,2,3}^{C} V_{Pq} + \sum_{r = 1,2,3}^{D} V_{Nr} \]  

(14)

\[ V_{O,\text{Min}} = V_{P1} \]  

(15)

if the number of bidirectional switches are not equal on both side, then

\[ (q - 1) \neq (r - 1) \]  

(16)

If \((q - 1) > (r - 1)\), \(n = (r - 1)\)

Else if \((q - 1) < (r - 1)\)

\[ n = (q - 1) \]

(17)

\[ x = ((q - 1) \sim (r - 1)) \]

(18)

In the ASEHB topology, the number of output voltage levels \(N_{\text{Level}}\) is

\[ N_{\text{Level}} = (n + 1)^2 + (n + 2)^2 + (2 + 2n)x \]  

(19)

If \(n = 1\) and \(x = 0\), then \(N_{\text{Level}} = (1 + 1)^2 + (1 + 2)^2 + (2 + 2(1))0 = 13.\)

If \(n = 1\) and \(x = 1\), then \(N_{\text{Level}} = (1 + 1)^2 + (1 + 2)^2 + (2 + 2(1))1 = 17.\)

If \(n = 1\) and \(x = 2\), then \(N_{\text{Level}} = (1 + 1)^2 + (1 + 2)^2 + (2 + 2(1))2 = 21.\)

\[ N_{\text{Uni}} = 6 \]  

(20)

\[ N_{\text{Bi}} = 2n + x \]  

(21)

\[ N_{DC} = 2(n + 1) + x \]  

(22)

\[ V_{O,\text{Max}} = \sum_{q = 1,2,3}^{C} V_{Pq} + \sum_{r = 1,2,3}^{D} V_{Nr} \]  

(23)

\[ V_{O,\text{Min}} = V_{P1} \]  

(24)

Method II Example

Where \(n\) is an equal number of bidirectional switches on both sides (SSEHB). The value of \(n\) can be found by using Equation (9).

The number of levels in the inverter output voltage is given below:

\[ N_{\text{Level}} = 2(n + 1) + (n + 1)^2 + (n + 2)^2 \]  

(25)

If \(n = 1\), then \(N_{\text{Level}} = 2(1 + 1) + (1 + 1)^2 + (1 + 2)^2 = 17.\)

If \(n = 2\), then \(N_{\text{Level}} = 2(2 + 1) + (2 + 1)^2 + (2 + 2)^2 = 31.\)

If \(n = 3\), then \(N_{\text{Level}} = 2(3 + 1) + (3 + 1)^2 + (3 + 2)^2 = 49.\)

The equations for the number of uni-directional switches \(N_{\text{Uni}}\), number of bi-directional switches \(N_{\text{Bi}}\), number of dc voltage sources \(N_{DC}\), maximum magnitude of the generated output voltage \(V_{O,\text{Max}}\), and the minimum magnitude of the generated output voltage \(V_{O,\text{Min}}\) are the same for the SSEHB topology represented in Equations (11)–(15), respectively.
If the topology contains unequal bidirectional switches (ASEHB) i.e., \((q - 1)\) bi-directional switches at the left side and \((r - 1)\) bi-directional switches at the right side. The value of \(n\) and \(x\) can be found by using Equations (17) and (18), respectively.

\[
N_{\text{Level}} = 2(n + 1) + (n + 1)^2 + (n + 2)^2 + (4 + 2n)x
\]  

(26)

If \(n = 1\), \(x = 0\), then \(N_{\text{Level}} = 2(1 + 1) + (1 + 1)^2 + (1 + 2)^2 + (4 + 2(1)) = 17\).

If \(n = 1\), \(x = 1\), then \(N_{\text{Level}} = 2(1 + 1) + (1 + 1)^2 + (1 + 2)^2 + (4 + 2(1)) = 23\).

If \(n = 3\), \(x = 5\), then \(N_{\text{Level}} = 2(3 + 1) + (3 + 1)^2 + (3 + 2)^2 + (4 + 2(3)) = 99\).

The equations for the number of uni-directional switches \(N_{\text{Uni}}\), number of bi-directional switches \(N_{\text{Bi}}\), number of DC voltage sources \(N_{\text{DC}}\), maximum magnitude of the generated output voltage \(V_{O,\text{Max}}\), and the minimum magnitude of the generated output voltage \(V_{O,\text{Min}}\) are the same for the ASEHB topology represented in Equations (20)–(24) respectively.

In this section, a various number of bidirectional switches are associated with the developed H-Bridge to enhance the performance of the base unit SSEHB and ASEHB inverter, and for further enhancement, the various methods are applied to the proposed inverters, as shown in Figure 1.

The number of output voltage levels for the different number of bidirectional switches and the two methods are tabulated in Table 1.

**Table 1.** Choice of the number of bidirectional switches with respect to the number of output voltage levels.

<table>
<thead>
<tr>
<th>Number of Bidirectional Switches in the Left Side (N_{\text{BL}}) ((q - 1))</th>
<th>Number of Bidirectional Switches in the Right Side (N_{\text{BL}}) ((r - 1))</th>
<th>Difference between the Number of Bidirectional Switches (x = (q - 1) - (r - 1))</th>
<th>(N_{\text{Level}}) ((\text{Method I}))</th>
<th>(N_{\text{Level}}) ((\text{Method II}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>13</td>
<td>17</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>17</td>
<td>23</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>21</td>
<td>29</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>3</td>
<td>25</td>
<td>35</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>4</td>
<td>29</td>
<td>41</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>5</td>
<td>33</td>
<td>47</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>0</td>
<td>17</td>
<td>23</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>21</td>
<td>29</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>2</td>
<td>25</td>
<td>35</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>3</td>
<td>29</td>
<td>41</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>4</td>
<td>33</td>
<td>47</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>5</td>
<td>37</td>
<td>53</td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>0</td>
<td>21</td>
<td>29</td>
</tr>
<tr>
<td>9</td>
<td>3</td>
<td>1</td>
<td>25</td>
<td>35</td>
</tr>
<tr>
<td>10</td>
<td>3</td>
<td>2</td>
<td>29</td>
<td>41</td>
</tr>
<tr>
<td>11</td>
<td>3</td>
<td>3</td>
<td>33</td>
<td>47</td>
</tr>
<tr>
<td>12</td>
<td>3</td>
<td>4</td>
<td>37</td>
<td>53</td>
</tr>
<tr>
<td>13</td>
<td>3</td>
<td>5</td>
<td>41</td>
<td>59</td>
</tr>
</tbody>
</table>

From Table 1, one can choose the number of bidirectional switches needed for the required level of output voltage. Comparing Methods I and II, Method II gives more output voltage levels for the same number of bidirectional switches.

### 3.1. Modes of Operation

As shown in Table 2, the SSEHB multilevel inverter shown in Figure 2 can generate 13 voltage levels—\((\pm V_{P2}), (+V_{P1} + V_{P2}), (+V_{N2} + V_{P2}), (+V_{N2} + V_{P2} + V_{P1}), (+V_{N2} + V_{N1} + V_{P2}), (+V_{N2} + V_{N1} + V_{P2} + V_{P1})\), and \((0)\) at the output, by selecting different magnitudes of the DC voltage sources as per the proposed Method I. As per the proposed Method II, the same SSEHB inverter is able to generate 17 levels by selecting different magnitudes of the DC voltage sources.

The ASEHB multilevel inverter shown in Figure 3 is able to generate 17 voltage levels at the output by selecting different magnitudes of the DC voltage sources, as per the proposed method I. As per the proposed method II, the same ASEHB inverter is able to generate 23 levels by selecting...
different magnitudes of the DC voltage sources, as shown in Table 3. The output voltage levels are \( \pm (V_{P2}), \pm (V_{P1} + V_{P2}), \pm (V_{N3}), \pm (V_{N3} + V_{P2}), \pm (V_{N3} + V_{P2} + V_{P1}), \pm (V_{N3} + V_{P2} + V_{P1}), \pm (V_{N3} + V_{N2} + V_{P1}), \pm (V_{N3} + V_{N2} + V_{P1}), \pm (V_{N3} + V_{N2} + V_{P1}), \pm (V_{N3} + V_{N2} + V_{P1}), \pm (V_{N3} + V_{N2} + V_{P1}), \) and (0).

### Table 2. Switching states of the proposed SSEHB inverter based on Method I.

<table>
<thead>
<tr>
<th>Level</th>
<th>Output Level Voltage</th>
<th>On Switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>S0, S1, S4</td>
</tr>
<tr>
<td>2</td>
<td>V_{P2}</td>
<td>S_{P1}, S_{P2}, S_{P3}</td>
</tr>
<tr>
<td>3</td>
<td>V_{P1} + V_{P2}</td>
<td>S1, S2, S4</td>
</tr>
<tr>
<td>4</td>
<td>V_{N2} + V_{P2}</td>
<td>S_{N1}, S_{P1}, S_{N2}</td>
</tr>
<tr>
<td>5</td>
<td>V_{N2} + V_{P2} + V_{P1}</td>
<td>S1, S_{N2}, S_{P1}</td>
</tr>
<tr>
<td>6</td>
<td>V_{N2} + V_{P1} + V_{P2}</td>
<td>S_{P1}, S_{N2}, S_{P1}</td>
</tr>
<tr>
<td>7</td>
<td>V_{N2} + V_{N1} + V_{P2}</td>
<td>S_{N1}, S_{P1}, S_{N2}</td>
</tr>
<tr>
<td>8</td>
<td>(-V_{P1})</td>
<td>S_{P1}, S_{P2}, S_{P3}</td>
</tr>
<tr>
<td>9</td>
<td>(-V_{P1})</td>
<td>S_{N1}, S_{P1}, S_{P2}</td>
</tr>
<tr>
<td>10</td>
<td>(-V_{N1} + V_{P1})</td>
<td>S_{N1}, S_{P1}, S_{N2}</td>
</tr>
<tr>
<td>11</td>
<td>(-V_{N1} + V_{P2} + V_{P1})</td>
<td>S_{N1}, S_{P1}, S_{N2}</td>
</tr>
<tr>
<td>12</td>
<td>(-V_{N1} + V_{N1} + V_{P1})</td>
<td>S_{N1}, S_{P1}, S_{N2}</td>
</tr>
<tr>
<td>13</td>
<td>(-V_{N2} + V_{P1})</td>
<td>S_{P1}, S_{P2}, S_{P3}</td>
</tr>
</tbody>
</table>

The 23 levels of the output voltage give 23 modes of operation. In any mode of operation, three switches are “ON”, and the remaining switches are “OFF”, as shown in Table 3. In all the modes of operation, one switch from the left side inverter circuit (S_{1}, S_{4}, or S_{P1(q − 1)}) and one switch from the right side inverter circuit (S_{2}, S_{3}, or S_{N1(f − 1)}), and one switch from the cascade connection (S_{X}, S_{Y}) are always in the “ON” state.

### Table 3. Switching states of the proposed asymmetrical structure enhanced H-Bridge (ASEHB) inverter based on Method II.

<table>
<thead>
<tr>
<th>Level</th>
<th>Output Level Voltage</th>
<th>On switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>S_{3}, S_{Y}, S_{4}</td>
</tr>
<tr>
<td>2</td>
<td>V_{P2}</td>
<td>S_{P1}, S_{P2}, S_{P3}</td>
</tr>
<tr>
<td>3</td>
<td>V_{P1} + V_{P2}</td>
<td>S1, S2, S4</td>
</tr>
<tr>
<td>4</td>
<td>V_{N3}</td>
<td>S_{N2}, S_{N4}, S_{Y}</td>
</tr>
<tr>
<td>5</td>
<td>V_{N3} + V_{P2}</td>
<td>S_{N1}, S_{N2}, S_{P1}</td>
</tr>
<tr>
<td>6</td>
<td>V_{N3} + V_{P2} + V_{P1}</td>
<td>S1, S_{N2}, S_{P1}</td>
</tr>
<tr>
<td>7</td>
<td>V_{N3} + V_{N2} + V_{P1}</td>
<td>S_{N1}, S_{P1}, S_{N2}</td>
</tr>
<tr>
<td>8</td>
<td>V_{N3} + V_{N2} + V_{P2}</td>
<td>S_{N1}, S_{P1}, S_{N2}</td>
</tr>
<tr>
<td>9</td>
<td>V_{N3} + V_{N2} + V_{N1}</td>
<td>S_{P1}, S_{N1}, S_{S}</td>
</tr>
<tr>
<td>10</td>
<td>V_{N3} + V_{N2} + V_{N1}</td>
<td>S_{P1}, S_{N1}, S_{S}</td>
</tr>
<tr>
<td>11</td>
<td>V_{N3} + V_{N2} + V_{N1}</td>
<td>S_{P1}, S_{N1}, S_{S}</td>
</tr>
<tr>
<td>12</td>
<td>V_{N3} + V_{N2} + V_{N1}</td>
<td>S_{P1}, S_{N1}, S_{S}</td>
</tr>
<tr>
<td>13</td>
<td>(-V_{P1})</td>
<td>S_{P1}, S_{P2}, S_{P3}</td>
</tr>
<tr>
<td>14</td>
<td>(-V_{P1})</td>
<td>S_{P1}, S_{P2}, S_{P3}</td>
</tr>
<tr>
<td>15</td>
<td>(-V_{N1})</td>
<td>S_{N1}, S_{N2}, S_{S}</td>
</tr>
<tr>
<td>16</td>
<td>(-V_{N1} + V_{P1})</td>
<td>S_{N1}, S_{P1}, S_{S}</td>
</tr>
<tr>
<td>17</td>
<td>(-V_{N1} + V_{P2})</td>
<td>S_{N1}, S_{P1}, S_{S}</td>
</tr>
<tr>
<td>18</td>
<td>(-V_{N1} + V_{N2})</td>
<td>S_{N2}, S_{N3}, S_{S}</td>
</tr>
<tr>
<td>19</td>
<td>(-V_{N1} + V_{N2} + V_{P1})</td>
<td>S_{N2}, S_{N3}, S_{S}</td>
</tr>
<tr>
<td>20</td>
<td>(-V_{N1} + V_{N2} + V_{N2})</td>
<td>S_{N2}, S_{N3}, S_{S}</td>
</tr>
<tr>
<td>21</td>
<td>(-V_{N1} + V_{N2} + V_{N3})</td>
<td>S_{N2}, S_{N3}, S_{S}</td>
</tr>
<tr>
<td>22</td>
<td>(-V_{N1} + V_{N2} + V_{N3})</td>
<td>S_{N2}, S_{N3}, S_{S}</td>
</tr>
<tr>
<td>23</td>
<td>(-V_{N1} + V_{N2} + V_{N3} + V_{P1} + V_{P2})</td>
<td>S_{N2}, S_{N3}, S_{S}</td>
</tr>
</tbody>
</table>

### 3.2. Voltage Stress across Switches

An important parameter that determines the cost of a multilevel inverter is the blocking voltage of the power switches, as well as the DC voltage sources. If the proposed inverter requires a variety of blocking voltage switches, then the cost of the inverter is too high. The voltage blocking mainly
depends on the topology of the inverter. In this section, voltage stress across various switches are derived for SSEHB and ASEHB inverters when methods I and II are applied. The equation to find the voltage stress across the switches is the same for both the SSEHB and ASEHB inverter.

The relation between $V_{Pq}$ and $V_{Nr}$ for Method I employing SSEHB and ASEHB inverters is shown in Equation (4). Similarly, the relationship between $V_{Pq}$ and $V_{Nr}$ for Method II employs SSEHB, and an ASEHB inverter is shown in Equation (8). For finding the blocking voltage across a switch substitute, the value of $V_{Nr}$ in terms of $V_{Pq}$ can be determined by Equations (27)–(31).

The blocking voltage across various power switches are given below:

$$V_{S1} = V_{S4} = \left( \sum_{q=1}^{C} V_{Pq} \right)$$  \hspace{1cm} (27)

$$V_{S2} = V_{S3} = \left( \sum_{r=1}^{D} V_{Nr} \right)$$  \hspace{1cm} (28)

$$V_{SP1} = V_{SP2} \cdots V_{SP(q-1)} = \left( \sum_{q=1}^{C-1} V_{Pq} \right)$$  \hspace{1cm} (29)

$$V_{SN1} = V_{SN2} \cdots V_{SN(r-1)} = \left( \sum_{r=1}^{D-1} V_{Nr} \right)$$  \hspace{1cm} (30)

$$V_{SX} = V_{SY} = \left( \sum_{q=1}^{C} V_{Pq} + \sum_{r=1}^{D} V_{Nr} \right)$$  \hspace{1cm} (31)

### 3.3. Conduction and Switching Losses

In this proposed ASEHB MLI, in all the modes of operation, only three switches are “ON”, and corresponding driver circuits are only “ON”, and so the power loss in the inverter during conduction is less compared to cascaded conventional H-Bridge inverter—hence, the efficiency of the inverter is improved. Here $P_C$ is the conduction loss of the power switches.

$$P_C = 3I^2R_{on}$$  \hspace{1cm} (32)

where $I$ is the current following through the switch, and $R_{on}$ is the on-state resistance of the switch during conduction period.

The switching losses mainly depend on the carrier frequency in pulse width modulation inverter, whereas here the switching is done based on the reference frequency compared with the input DC voltage levels, so the switching losses depend on the number of levels of the inverter. Here the switching losses are calculated in three group of switches.

The left side group is comprised of the switches $S_1, S_4$, and $S_{P1}$ to $S_{P(q-1)}$, and the total left-side group switch losses is equal to $P_{SL}$. Similarly, the right-side group is comprised of the following switches $S_2, S_3$, and $S_{N1}$ to $S_{N(r-1)}$, and the total right-side group switch losses is equal to $P_{SR}$. Finally, the cascaded group comprises the following switches $S_X$ and $S_Y$, and the total cascaded switching losses are equal to $P_{Scas}$.

$$P_{SL} = (2N_{Level} - 1) f_{ref}C_{ce} \left( \sum_{q=1}^{q} V_{Pq}^2 \right)$$  \hspace{1cm} (33)

$$P_{SR} = \left\{ \text{integer of} \left[ \frac{(2N_{Level} - 1)}{(q + 1)} \right] \right\} f_{ref}C_{ce} \left( \sum_{r=1}^{r} V_{Nr}^2 \right)$$  \hspace{1cm} (34)

$$P_{Scas} = 2f_{ref}C_{ce} V_{o,max}^2$$  \hspace{1cm} (35)
Here the \( f_{\text{ref}} \) is the reference frequency, and \( C_{ce} \) is the capacitance across the collector and emitter of IGBT.

### 3.4. Sinusoidal Tracking Algorithm for an Enhanced H-Bridge Multilevel Inverter

This algorithm tracks the fundamental sinusoidal function to calculate the time at which to turn on the switches. The \( V_m \) and \( f \) is calculated with the help of sinusoidal reference. With the help of \( f \) and \( V_m = V_{\text{ref.p}} \), fundamental reference \( V_{\text{ref}} \) is generated as given in Equation (36). A rectangle with area \( A_i \) is formed between successive voltage levels \( (\Delta V) \), and the time interval between these voltage levels \( (\Delta t) \). To find the equal area between two successive voltage levels, increment time by \( j \), where the sampling time \( j \) is given in Equation (38). Increment the time by \( j \) and find \( V_{ij} \), then calculate the area \( A_{ij} \) until the area of the rectangle is exactly 25% of the total area \( A_i \). At that resultant time \( (t_{\text{opt}}) \) or angle \( (\alpha) \) and voltage, the corresponding switches for \( i \) mode are turned on. Similarly, calculate for all the voltage levels from zero to \( V_{\text{max}} \). The best switching times to get the minimum THD using this sinusoidal tracking method is the time when the areas of the upper and the lower triangle of the fundamental sinusoidal wave are equal, as shown in Figure 4. Figure 5 details the switching states and timing calculation of the sinusoidal tracking algorithm for various input sinusoidal reference using a flowchart. This sinusoidal tracking algorithm is implemented with the help of a high-level language. The switching time is calculated offline and stored in the local PROM (programmable read only memory) of the PIC (peripheral interface controller) for various inputs of sinusoidal reference. Consider that the input DC voltages are stable and ripple-free to get a perfect enhanced performance for the proposed EHB MLI.

\[
V_{\text{ref}} = V_{\text{ref.p}} \sin \omega t 
\]

\[
X = 2 \left( \text{integer of} \left( \frac{V_{\text{ref.p}}}{V_{\text{p1}}} + 0.99 \right) \right) 
\]

\[
j = \frac{1}{f \times 10,000} 
\]

\[
V_i = i \times V_{\text{p1}} 
\]

\[
t_i = \frac{\sin^{-1} \left( \frac{V_i}{V_m} \right)}{\omega} 
\]

---

**Figure 4.** Fundamental sinusoidal tracking method for the switching techniques to find optimum switching time \( t_{\text{opt}} \).
3.5. Comparison with Other Multilevel Inverters

Table 4 compares the advantages of the proposed enhanced H-Bridge MLI with the various other H-Bridge multilevel inverters. \( N_{ON} \) is the number of switches that are “ON” in a particular state.
Table 4. Comparison of the basic cell used in the various topologies.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$N_{DC}$</th>
<th>$N_{Uni}$</th>
<th>$N_{Bi}$</th>
<th>$N_{level}$</th>
<th>$N_{ON}$</th>
<th>$N_{Variety}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>H-Bridge</td>
<td>1</td>
<td>4</td>
<td>–</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Modified H-Bridge [7–12]</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>5</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Developed H-Bridge [19]</td>
<td>2</td>
<td>6</td>
<td>–</td>
<td>7</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Cascaded developed H-Bridge [19]</td>
<td>4</td>
<td>10</td>
<td>–</td>
<td>31</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Series connection of sub-MLI [17]: symmetric</td>
<td>6</td>
<td>14</td>
<td>–</td>
<td>13</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>Series connection of sub-MLI [17]: asymmetric</td>
<td>4</td>
<td>12</td>
<td>–</td>
<td>31</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>Proposed SSEHB (Method I)</td>
<td>4</td>
<td>6</td>
<td>2</td>
<td>13</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Proposed SSEHB (Method II)</td>
<td>4</td>
<td>6</td>
<td>2</td>
<td>17</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Proposed ASEHB (Method I)</td>
<td>5</td>
<td>6</td>
<td>3</td>
<td>17</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Proposed ASEHB (Method II)</td>
<td>5</td>
<td>6</td>
<td>3</td>
<td>23</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Proposed ASEHB (Method II)</td>
<td>5</td>
<td>6</td>
<td>4</td>
<td>31</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>ASEHB (Method II)</td>
<td>6</td>
<td>6</td>
<td>4</td>
<td>31</td>
<td>3</td>
<td>5</td>
</tr>
</tbody>
</table>

The modified H-Bridge inverter [7] requires 14 bidirectional switches and 15 symmetrical value DC voltage sources to get a 31-level output voltage. The cascaded developed H-Bridge inverter [19] needs 10 unidirectional switches and four DC voltage sources to get a 31-level output voltage. With the proposed base unit EHB 31 level inverter, or even a 99-level inverter, in all the modes of operation only three switches are “ON”, whereas with the cascaded developed H-Bridge [19], five switches are on in all the modes of operation for 31 levels. Hence, the switching conduction losses are minimized compared to the cascaded developed H-Bridge [19], but there is an increase in the number of DC sources. The proposed enhanced H-Bridge is the most suitable for a higher number of levels, a lower THD with reduced switching conduction losses, and the lesser number of a variety of blocking voltage power switches.

4. Simulation Results

To study and verify the performance of a single-phase SSEHB 13-level inverter with optimum components, a 13-level output based on the Method I has been simulated. Table 2 shows the switching states of the 13-level inverter. Simulation has been done by using MATLAB/SIMULINK R2017a software, and Table 5 lists the simulation parameters. For the proposed SSEHB 13-level inverter, the output voltage is obtained by comparing various ($\pm 55, \pm 110, 165, \pm 220, \pm 275, \pm 330, 0$) DC levels with the fundamental sinusoidal function (335 V), as per the switching pattern, is given in Table 2. Similarly, to study and verify the performance of a single-phase ASEHB 23-level inverter with optimum components, a 23-level output voltage based on Method II has been simulated. Table 3 shows the switching states of the 23-level inverter. The output voltage of the proposed ASEHB 23-level inverter is obtained by comparing the various ($\pm 30, \pm 60, \pm 90, \pm 120, \pm 150, \pm 180, \pm 210, \pm 240, \pm 270, \pm 300, \pm 330, 0$) DC levels with the fundamental sinusoidal function (335 V) as per the switching pattern given in the Table 5.

Table 5. Simulation parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SSEHB Inverter (Method I)</th>
<th>ASEHB Inverter (Method II)</th>
<th>ASEHB Inverter (Method II)-Medium Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{P1}$</td>
<td>55</td>
<td>30</td>
<td>300</td>
</tr>
<tr>
<td>$V_{P2}$</td>
<td>55</td>
<td>30</td>
<td>300</td>
</tr>
<tr>
<td>$V_{N1}$</td>
<td>110</td>
<td>90</td>
<td>900</td>
</tr>
<tr>
<td>$V_{N2}$</td>
<td>110</td>
<td>90</td>
<td>900</td>
</tr>
<tr>
<td>$V_{N3}$</td>
<td>–</td>
<td>90</td>
<td>900</td>
</tr>
<tr>
<td>$N_{Uni}$</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>$N_{Bi}$</td>
<td>2</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Load resistor in ohm</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>RL load</td>
<td>$50 + 0.055 , \Omega$</td>
<td>$50 + 0.055 , \Omega$</td>
<td>–</td>
</tr>
<tr>
<td>Output frequency</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>$N_{Level}$</td>
<td>13</td>
<td>23</td>
<td>23</td>
</tr>
<tr>
<td>$V_{M}$ (Peak)</td>
<td>330</td>
<td>330</td>
<td>3300</td>
</tr>
</tbody>
</table>
The MATLAB/SIMULINK model for the proposed ASEHB 23-level inverter 300 V peak is as shown in Figure 6.

![MATLAB/SIMULINK model of 23-level ASEHB inverter.](image)

Figure 6. MATLAB/SIMULINK model of 23-level ASEHB inverter.

The pulse generator of switch S3 is shown in Figure 7. The optimum time \( t_{\text{opt}} \) to turn on a switch is obtained from the sinusoidal tracking algorithm. The amplitude of the reference sinusoidal at the optimum time \( t_{\text{opt}} \) and the previous state of a switch is compared to generate the pulse. Similarly, for all the transitions of switch S3, switching pulses are generated and logically ‘OR’ed to give the complete pulse of S3. The switching pulses for all other switches are generated using the same procedure.

![Pulse generator of switch S3 of a 23-level ASEHB inverter.](image)

Figure 7. Pulse generator of switch S3 of a 23-level ASEHB inverter.

Figure 8 shows the simulated output voltage and current waveforms of a proposed single-phase SSEHB 13-level inverter connected to a standalone R load. From observation, the SSEHB inverter generates the desired 13-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

![Simulated output voltage and current waveforms of a proposed single-phase SSEHB 13-level inverter.](image)

Figure 8. Simulation result of an SSEHB 13-level inverter with R load. (a) Output voltage waveform; (b) output current waveform.
for all the transitions of switch S3, switching pulses are generated and logically ‘OR’ed to give the complete pulse of S3. The switching pulses for all other switches are generated using the same procedure.

Figure 7. Pulse generator of switch S3 of a 23-level ASEHB inverter.

Figure 8 shows the simulated output voltage and current waveforms of a proposed single-phase SSEHB 13-level inverter connected to a standalone R load. From observation, the SSEHB inverter generates the desired 13-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

(a) (b)

Figure 8. Simulation result of an SSEHB 13-level inverter with R load. (a) Output voltage waveform; (b) output current waveform.

Figure 9 Shows the frequency spectrum of the SSEHB 13-level inverter’s output voltage and current waveform when connected to a purely resistive load. The total harmonic distortion of voltage and current is found to be 5.45% and 5.45%, respectively.

(a) (b)

Figure 9. Simulation result of an SSEHB 13-level inverter with R load. (a) FFT (Fast Fourier Transform) analysis of the output voltage; (b) FFT analysis of the output current.

Figure 10 shows the simulated output voltage and current waveforms of a proposed single phase SSEHB 13-level inverter connected to a standalone RL load. From the observation, the SSEHB inverter generates the desired 13-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

(a) (b)

Figure 10. Simulation result of an SSEHB 13-level inverter with an RL load. (a) Output voltage waveform; (b) output current waveform.

Figure 11 shows the frequency spectrum of the SSEHB 13-level inverter’s output voltage and current waveform when connected to an RL load. The total harmonic distortion of the current is found to be 3.51%.

(a) (b)

Figure 11. Simulation result of an SSEHB 13-level inverter with an RL load. (a) FFT (Fast Fourier Transform) analysis of the output voltage; (b) FFT analysis of the output current.
Figure 9. Simulation result of an SSEHB 13-level inverter with R load. (a) FFT (Fast Fourier Transform) analysis of the output voltage; (b) FFT analysis of the output current.

Figure 10 shows the simulated output voltage and current waveforms of a proposed single phase SSEHB 13-level inverter connected to a standalone RL load. From the observation, the SSEHB inverter generates the desired 13-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

Figure 11 shows the frequency spectrum of the SSEHB 13-level inverter’s output voltage and current waveform when connected to an RL load. The total harmonic distortion of the current is found to be 3.51%.

Figure 12 shows the simulated output voltage and current waveforms of a proposed single-phase ASEHB 23-level inverter connected to a standalone R load. From observation, the ASEHB inverter generates the desired 23-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

Figure 11. Output current frequency spectrum of an SSEHB 13-level inverter with an RL load. The total harmonic distortion of voltage and current is found to be 1.09%.

Figure 12. Simulation result of an ASEHB 23-level inverter with an R load. (a) Output voltage waveform; (b) output current waveform.
Figure 11. Output current frequency spectrum of an SSEHB 13-level inverter with an RL load.

Figure 12 shows the simulated output voltage and current waveforms of a proposed single-phase ASEHB 23-level inverter connected to a standalone R load. From observation, the ASEHB inverter generates the desired 23-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

Figure 13 shows the frequency spectrum of the ASEHB 23-level inverter’s output voltage and current waveform when connected to a purely resistive load. The total harmonic distortion of voltage and current is found to be 1.09% and 1.09%, respectively.

Figure 12. Simulation result of an ASEHB 23-level inverter with an R load. (a) Output voltage waveform; (b) output current waveform.

Figure 13. Simulation result of an ASEHB 23-level inverter with R load. (a) FFT analysis of output voltage; (b) FFT analysis of output current.

Figure 14 shows the simulated output voltage and current waveforms of a proposed single-phase ASEHB 23-level inverter connected to a standalone RL load. From the observation, the ASEHB inverter generates the desired 23-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

Figure 14. Simulation result of an ASEHB twenty-three level inverter with an RL load. (a) Output voltage waveform; (b) output current waveform.
Figure 13. Simulation result of an ASEHB 23-level inverter with R load. (a) FFT analysis of output voltage; (b) FFT analysis of output current.

Figure 14 shows the simulated output voltage and current waveforms of a proposed single-phase ASEHB 23-level inverter connected to a standalone RL load. From the observation, the ASEHB inverter generates the desired 23-level, 50 Hz stepped output voltage (sinusoidal fundamental) and the current waveform.

Figure 15. Output current frequency spectrum of an ASEHB 23-level inverter with an RL load. The total harmonic distortion of current is found to be 0.45%.

Figure 15. Simulation result of an ASEHB twenty-three level inverter with an RL load. (a) Output voltage waveform; (b) output current waveform.

The voltage stress across the various switches of an ASEHB 23-level 330 V peak inverter with the help of MATLAB simulation is shown in Figure 16. Analyzing Figure 16, the maximum voltage stress across the switches is $S_1 = 60\, \text{V}$, $S_2 = 270\, \text{V}$, $S_{P1} = 30$, $S_{N1} = 180$, and $S_X = 330$, which is validated with Equations (27)–(31), respectively.
The voltage stress across the various switches of an ASEHB 23-level 330 V peak inverter with the help of MATLAB simulation is shown in Figure 16. Analyzing Figure 16, the maximum voltage stress across the switches is $S_1 = 60$ V, $S_2 = 270$ V, $S_{P1} = 30$, $S_{N1} = 180$, and $S_X = 330$, which is validated with Equations (27)–(31), respectively.

Figure 16. Voltage stress across the switches of an ASEHB 23-level inverter. (a) Voltage stress across switch $S_1$; (b) voltage stress across switch $S_2$; (c) voltage stress across switch $S_{P1}$; (d) voltage stress across switch $S_{N1}$; (e) voltage stress across switch $S_X$.

Figure 17 shows the simulated medium output voltage and current waveforms of a proposed single-phase ASEHB 23-level inverter connected to a standalone R load. From the observation, the ASEHB inverter generates the desired 23-level, 50 Hz stepped peak 3300 V output voltage (sinusoidal fundamental) and the current waveform.
Figure 17 shows the simulated medium output voltage and current waveforms of a proposed single-phase ASEHB 23-level inverter connected to a standalone R load. From the observation, the ASEHB inverter generates the desired 23-level, 50 Hz stepped peak 3300 V output voltage (sinusoidal fundamental) and the current waveform.

Figure 17. Simulation result of an ASEHB 23-level medium voltage (3300 V peak) inverter with an R load. (a) Output voltage waveform; (b) output current waveform.

Figure 18 shows the frequency spectrum of the ASEHB 23-level inverter’s output 3300 V peak waveform when connected to an R load. The total harmonic distortion of the voltage was found to be 1.09%.

Figure 18. Output medium voltage (3300 V peak) frequency spectrum of an ASEHB 23-level inverter with an R load.
Experimental Results

From Table 3, an ASEHB inverter employed with Method II produces a higher number of output voltage levels compared to Method I for the same number of switching devices. The complete comparison is also tabulated in Table 1. This comparison, along with the simulation results shown in Figure 12a, has been the motivating factor in developing an ASEHB 23-level inverter working model. Table 6 lists the hardware specifications. In this, the PIC 16F887 series is used to generate the switching states, with the help of a comparison of various DC voltage levels with the reference signal, and stores the switching state’s timing in it.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of DC input voltage sources</td>
<td>5</td>
<td>-</td>
</tr>
<tr>
<td>$V_{P1}$</td>
<td>30 V</td>
<td>-</td>
</tr>
<tr>
<td>$V_{P2}$</td>
<td>30 V</td>
<td>-</td>
</tr>
<tr>
<td>$V_{N1}$</td>
<td>90 V</td>
<td>-</td>
</tr>
<tr>
<td>$V_{N2}$</td>
<td>90 V</td>
<td>-</td>
</tr>
<tr>
<td>$V_{N3}$</td>
<td>90 V</td>
<td>-</td>
</tr>
<tr>
<td>Number of unidirectional switches</td>
<td>6</td>
<td>KGT25N120NDA</td>
</tr>
<tr>
<td>Number of bidirectional switches</td>
<td>3</td>
<td>KGT25N120NDA</td>
</tr>
<tr>
<td>Number of gate drive circuits</td>
<td>9</td>
<td>TLP250</td>
</tr>
<tr>
<td>Microcontroller</td>
<td>1</td>
<td>PIC16F887</td>
</tr>
<tr>
<td>Load resistor (in ohm)</td>
<td>50</td>
<td>-</td>
</tr>
<tr>
<td>Number of output voltage levels</td>
<td>23</td>
<td>-</td>
</tr>
</tbody>
</table>

The switching frequency is very low, as per the comparison of various DC voltage levels with the reference signal; hence, IGBT was chosen for power inverter circuits. This switching pulse triggers the IGBT switches present in the inverter through isolated gate driver circuits. Figure 19 shows the hardware layout, and the ASEHB 23-level 660 V peak-to-peak and 233 V RMS (root mean square) hardware output voltage is shown in Figure 20. The THD value of an ASEHB 23 level inverter working model is 4.17%, as shown in Figure 21, measured with the help of utility software, TDSPCS1 v2.6-enabled Tektronix digital storage oscilloscope.

![ASEHB 23-level inverter hardware layout](image)
5. Conclusions

In this paper, a single-phase EHB multilevel inverter employed with a sinusoidal tracking algorithm has been proposed to generate 13-, 17-, and 23-level output voltages, respectively. From Tables 2 and 3, Method II gives an enhanced performance to the proposed ASEHB inverter. The most important advantages of this topology are (1) less conduction loss, due to the reason that only three switches are “ON” in all the modes of operation; (2) fewer switching losses; and (3) a reduction in the variety of the blocking voltage and driver circuit used, compared with conventional H-Bridge inverters. In the proposed inverter, only three switches are “ON” in all the modes, hence the conduction losses are minimized compared with other MLIs, as shown in Table 4. The output voltage waveform of the ASEHB 23-level inverter contains 4.17% THD, as shown in Figure 18. In the proposed inverter, the switching devices are designed for high-voltage and low-frequency operation. Therefore, the EHB multilevel inverter can be applied to medium power applications. This basic cell is suitable up to 99 levels—beyond that, the cascading of two basic units with a suitable number of bidirectional switches gives the required number of voltage levels.

The future scope of this paper is that the proposed enhanced H-Bridge multilevel inverter can be cascaded to generate a higher number of levels.
Author Contributions: In this research activity, A.T. proposed the core idea and developed the algorithm and simulation models; A.T. developed the hardware design, and measurement. He also conducted the simulation and the writing of this manuscript. U.K. validated the simulation results and provided guidance and supervision.

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References


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