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Luminaire Digital Design Flow with Multi-Domain Digital Twins of LEDs †

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Abstract: At present, when designing a Light Emitting Diode (LED) luminaire, different strategies of development are followed depending on the size of the company. Since on LED datasheets there is only limited information provided, companies designing LED luminaires spend a lot of effort gathering the required input of LED details to be able to design reliable products. Small and medium size enterprises (SMEs) do not have the bandwidth to gather such input and solely rely on empirical approaches leading to approximated luminaire designs, while larger companies use advanced hardware and software tools to characterize parts, design versions, and finally optimize all design steps. In both cases, considerable time and money is spent on prototyping, sampling, and laboratory testing. Digitalization of the complete product development (also known as Industry 4.0 approach) at all integration levels of the solid state lighting (SSL) supply chain would provide the remedy for these pains. The Delphi4LED European project aimed at developing multi-domain compact models of LED (for a consistent, combined description of electronic, thermal, and optical properties of LEDs) as digital twins of the physical products to support virtual prototyping during the design of luminaires. This paper provides an overview of the Delphi4LED approach aimed at supporting new, completely digital workflows both for SMEs and larger companies (Majors) along with some comparison with the traditional luminaire design. Two demonstration experiments are described: One to show the achievable benefits of the approach and another one to demonstrate the ease of use and ability to be accommodated in a larger scale product design for assessing design choices like e.g., number and type of LEDs versus electrical/thermal conditions and constraints, in a tool agnostic manner.

Keywords: LED digital twin; design flow; multi-domain compact model; tool agnostic; multi-LED

1. Introduction

The past two decades have seen growing adoption of light emitting diodes (LEDs) thanks to their improved efficacy and decreasing cost. According to the Strategies in Light conference in 2019, the trend is to move towards LED components commoditization, and the lighting industry is entering

another era with more demanding customers, market acceleration, and integration that extends beyond lighting (e.g., sensors). Industry 4.0, the fourth industrial revolution that exploits automation and data exchange, further facilitates acceleration and customization. To stay competitive, the lighting industry should embrace the digitalized early phase of development, which is currently in its infancy, to create space for new innovation beyond lighting (e.g. LiFi). A primary challenge to this approach is establishing ways for system integrators to have sufficiently detailed information on components without requiring LED suppliers to disclose proprietary information. The Delphi4LED H2020 ECSEL R&D project [1,2] of the EU proposes means to accelerate the transition to this new paradigm by creating the very first multi-domain LED "digital twin" from measurements and characterisations, and by suggesting new workflows using such digital twins [3]. One of the project's main objectives was to develop testing and modelling methodologies aimed at multi-domain characterisation of LED-based products at different levels of integration along the solid state lighting (SSL) supply chain, starting from modelling LED chips up to creating complete system level models of LED luminaires.

1.1. Digital Twins, Virtual Prototyping, and Digitalized Design Flow

Schluse provides a definition of digital twins [3]. In "Industry 4.0" context, a "digital twin" is a virtual representation of a real world subject (person, software system, ...) or a real world object (machine, component, part of the environment, ...). A digital twin contains models of its "data" (geometry, structure, ...), its functionality (data processing, behaviour, ...) and its communication interfaces. Figure 1 represents the digital twin components.

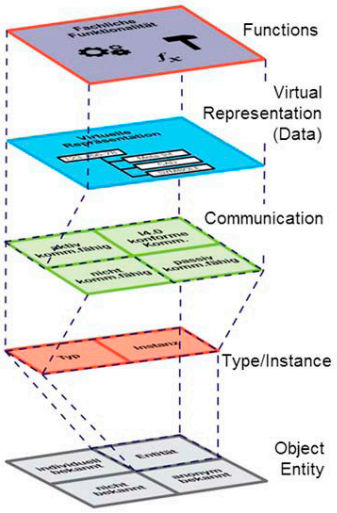


Figure 1. The "Industry 4.0 component" [4].

Research on all levels is required to allow for building full-blown digital twins of the product development cycle, the resulting products or the production environments.

When applied to LEDs and solid-state lighting product design, the LED digital twin is the multi-domain model of the packaged LED chips, including the physical structure of the package. In the context of the work presented in this paper virtual prototyping means testing of different versions of complete luminaire designs with the help of the luminaires' digital twins in different application scenarios by means of computer simulation. In a wider design flow context product optimization is also performed with the help of such digital twins. Development workflows relying completely on digital twins are called fully digitalized development workflows. Figure 2 represents the different dimensions involved in the creation of the LED digital twin (after [3]).

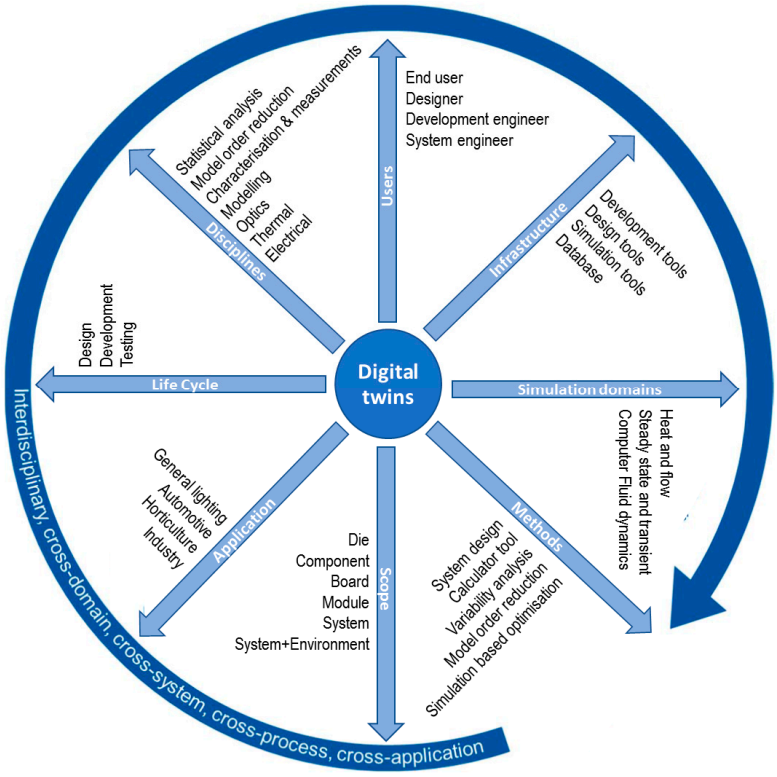


Figure 2. Different dimensions considered for the creation of the light emitting diode (LED) digital twin [3].

In other words, in the context of the lighting industry, major properties (such as the total emitted luminous flux) of a foreseen new luminaire can by identified under different combinations of application conditions through computer simulation and the effects of different design choices can be assessed, therefore design parameters can be optimized.

1.2. Objectives

The main purpose and novelty of the Delphi4LED project was the development of a comprehensive methodology to create a multi-domain LED digital twins (capturing LED behaviour regarding the electrical, thermal, and optical properties consistently in its entire operating domain) and provide a systematic, bottom-up hierarchical modelling approach that matches the computerized design environments, design, and simulation tools forming a complete design and simulation workflow that brings Industry 4.0 to the design of solid-state lighting products. To the best of the authors' knowledge, such a comprehensive approach is still missing. In view of this, the present paper proposes a generic methodology applicable to situations ranging from LED packages up to complete luminaires by creating a "digital twin" that properly represents its real, physical counterpart for simulation based experiments and optimization.

In this paper, we demonstrate the new "Industry 4.0"-like approach developed within the Delphi4LED project through the examples of LED-based luminaires. This paper extends earlier work [5], to validate with more LEDs, making it tool-agnostic and addressing the impact on the company digital footprint. In this study, the digital flow, its approach, and impacts are further presented, analysed, and discussed. The paper highlights the three key pillars for ensuring the sustainability of the approach in the lighting industry: Modelling of the LED packages to create their "digital twins" for the proposed design flow and the actual implementation of these models; the workflow together with involved personas at the different stages of workflow and the impact of the LED digital twins; and the proposed new product design workflows on the company digital footprint.

2. Materials and Methods

To protect their intellectual property, LED suppliers do not share sensitive and proprietary product details such as material properties or the architecture of their LED components. To develop LED-based products that are both reliable and cost-effective, detailed modelling is required early in the design process to predict performance so that appropriate design choices can be made as early as possible during the product development process. In the early product design phase, to properly represent the behaviour of an LED, a full LED model has to be built. Currently, this is done using reverse engineering to identify the LED build-up, dimensions, and material properties prior to modelling. This step adds cost, time, and uncertainty to the product design phase. The vision of the Delphi4LED consortium was to reduce time to market while increasing the accuracy of predictions by "digitizing" the early design phase: Replacing characterisation of physical product samples by their digital twins aimed for computer simulation. One key to a future with fully digitalized LED product development is the availability of compact, multi-domain (thermal-optical-electrical) models of LED components. The goal of the proposed approach is to create a multi-domain digital twin of LED packages directly from measurements [2]. (The term "LED package" is used by different professional organizations in the lighting world to refer to an LED chip fully encapsulated in a mechanical enclosure, the "package", complete with electrical connections and optical parts to form a fully functional LED device that can be used further on in product integration, as the basic component.)

Figure 3 illustrates the hierarchical, bottom-up modelling approach from LED chip level to LED module level. The multi-domain operation is captured on LED chip level. Such a chip level model combined with the compact thermal model of the mechanical structure of the package forms the package level LED model, also called LED digital twin. At the module level, we create the compact thermal model of the module substrate as a multi heat-source model, where the heat-sources are the pads of the LED packages through which the power dissipated by the LEDs of the populated module enter the substrate. The luminaire's digital twin (virtual prototype) includes the luminaire's thermal model, considering also the LED driver and luminaire optics and their losses. As it will be shown later in this paper, the level of detail in the luminaire digital twin depends on the actual application and on the available CAD tools with which the proposed workflow is implemented.

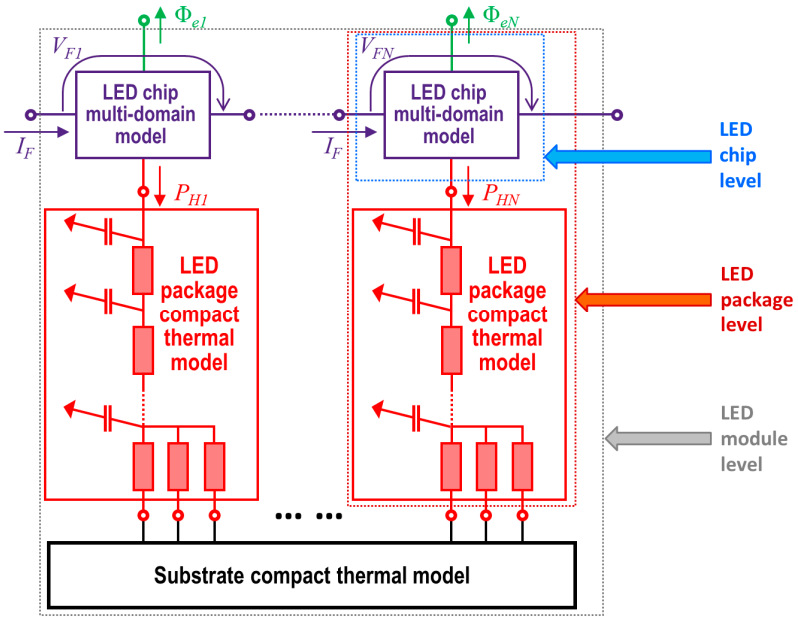


Figure 3. Bottom-up, hierarchical approach of modelling from LED chip to LED module level, with multi-domain operation captured on the chip.

Figure 4 illustrates through what steps the physical LED devices are linked to the module or luminaire level of product design and simulation tools in a fully Industry 4.0-like solid-state lighting eco-system. As illustrated here, the interface between the physical devices and their digital twins is represented by future electronic LED datasheets. The first step towards achieving widespread use of such datasheets is the LED suppliers' and LED users' consensus on LED test data reporting, both in terms of the type and number of tests data included and in terms of machine readable file formats such as XML. Work regarding recommendations on LED test data reporting is in progress at the International Commission on Illumination (CIE) [6].

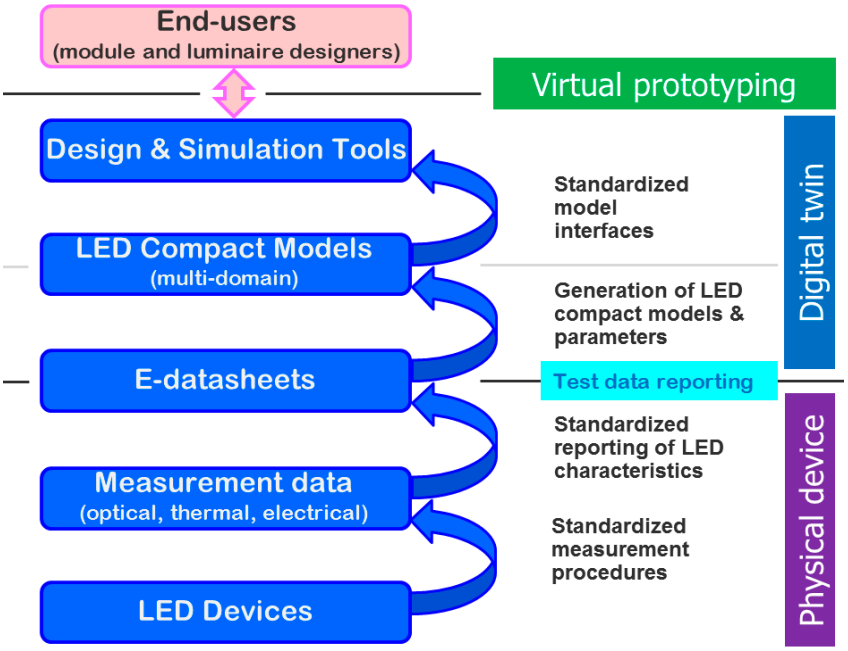


Figure 4. The Delphi4LED approach to digitalization of LED application design by creating digital twins of physical samples of packaged LEDs. The interface between the physical LEDs and their digital twins is represented by the electronic LED datasheets. The interface between LED vendors and end-users is represented by multi-domain LED compact models: the LED digital twins.

Figure 5 provides the major steps of creating the multi-domain compact models of LED packages. The LED package (multi-domain) compact model is comprised of; (1) a boundary condition-independent compact thermal model of the physical LED package and (2) a multi-domain, so called Spice-like, model that describes the LED operation at the chip level [7]. The former can be created with the help of the measured real thermal impedance, $Z_{th}(t)$ of the LED package in question while the parameters of a chip level LED model can be identified from the so called isothermal current-voltage-flux characteristics of the LED device (see later).

Temperature is the most important operating parameter that defines the operation of LEDs. Thermal modelling of LED packages, modules, and luminaires is a cornerstone at all integration levels from LED chips to LED luminaires. We treat the multi-domain operation basically at the LED chip level/LED package level, as shown in Figure 3 and in Figure 5.

At the chip level, a physics-based model is created by using characteristics derived from measurements while at the package level a dynamic thermal compact model is created in two steps. First a detailed thermal model of the LED package structure is set up and "calibrated" with the help of structure functions derived from the measured thermal impedance, $Z_{th}(t)$ of the package and then, in a subsequent step, thermal capacitance and thermal resistance values of a thermal RC network model of the package are optimized to best represent the thermal properties of the LED package under any boundary conditions at the package footprints and the LED's dome (lens) [8].

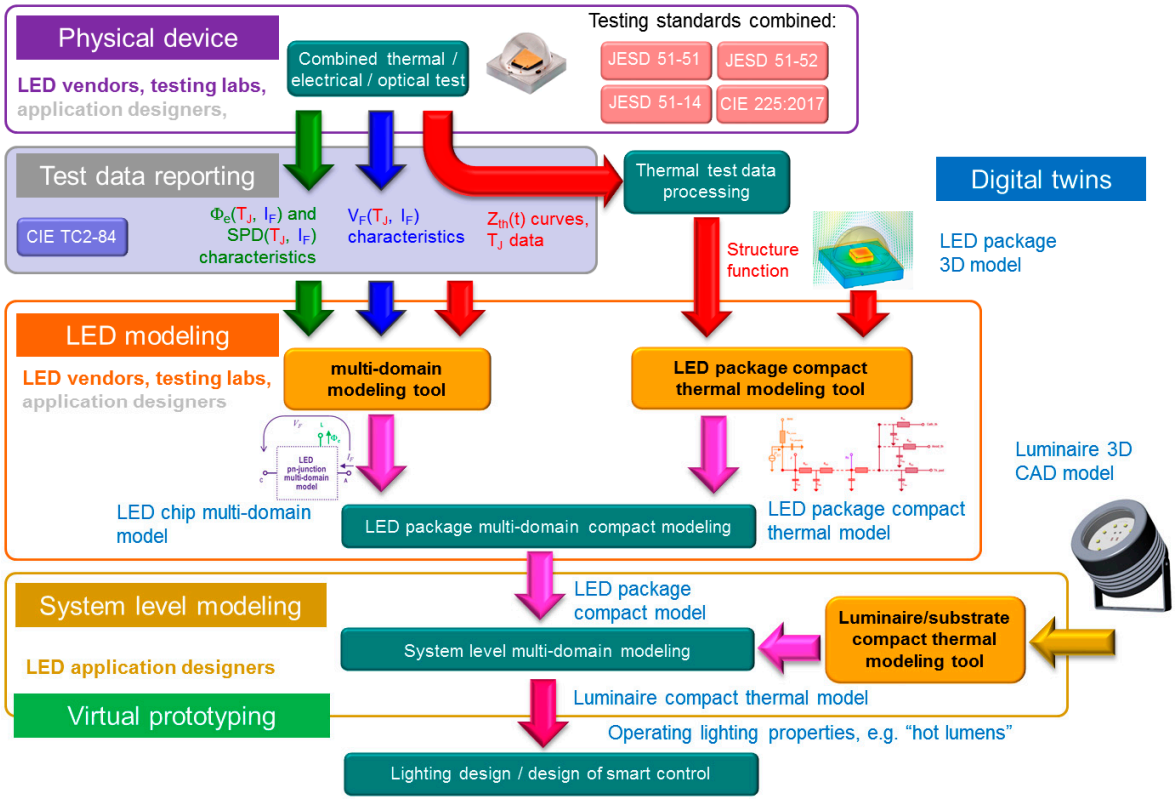


Figure 5. Delphi4LED workflow for generation and application of digital twins of LED packages, modules, and luminaires.

From LED to luminaire (Figure 5), the Delphi4LED approach consists of the following key steps:

1. Standardized measurements and characterisation of LEDs combining the testing standards JEDEC JESD51-14, JESD 51-51, JESD 51-52, and CIE 225-2017 [9–12]; for a summary on LED testing see [13].
2. Characteristics are reported in a standard way through an electronic datasheet (e-datasheet); work towards recommendations on such LED test data reporting is in progress at the CIE TC2-84 technical committee [6].
3. A LED digital twin, also called multi-domain compact model [7,14–17], is created. This includes a dynamic compact thermal model of the mechanical structure of the LED package [8].
4. The LED digital twin is implemented in a calculation tool or simulation tool together with the light engine and luminaire twins [5] through a standardized interface.

Step one through three are executed typically by LED vendors or testing labs, as indicated also in Figure 5. Step four is performed together with the luminaire design by luminaire makers. As will be discussed later, we categorize these luminaire manufacturers into two groups: Small and medium size companies (SMEs) and large international companies (Majors).

In the following subsections we detail these four major steps in greater detail, from a product design perspective, supported also by a case study.

2.1. Measurements and Characterisation of LEDs, Test Data Reporting

To describe the multi-domain feature of LED operation, parameters including light output, thermal, and electrical characteristics are measured in a consistent way.

New testing protocols and modelling methodologies were developed to allow easy creation of compact models based on measurement data [16–19].

Measurements take into account the latest LED testing methods, such as JEDEC's thermal testing standards for power semiconductors [9] and power LEDs [10,11] as well as CIE's LED optical testing recommendations for high power LEDs [12]. Applying these recommendations, so called isothermal current-voltage-flux characteristics (IVL characteristics) are measured in combination with the real thermal impedance, $Z_{th}(t)$ of the package. For thermal modelling purposes, the equivalent representation, so called structure functions, of the impedance curves are used [13].

The basis of the Delphi4LED approach of LED application design is that LED vendors provide the necessary data on packaged LED chips (LED packages) in a standard way; e.g., an electronic format that can be further processed by software tools for extracting the right LED digital twins from these. Currently, the TC2-84 technical committee of Division 2 of CIE deals with establishing recommendations on test data reporting of LED packages [6].

2.2. Creation of the LED Digital Twin

Poppe et al. described die level modelling and integration with package modelling, up to a system level compact model of a complete luminaire [20,21]. In the subsequent subsection, following the bottom-up hierarchy shown in Figure 3, we present, how this earlier concept was implemented in the Delphi4LED design flow.

As mentioned earlier, the multi-domain model of an LED package combines the digital twin at chip level and the dynamic thermal compact model of the LED package.

2.2.1. Digital Twin of LED Chip

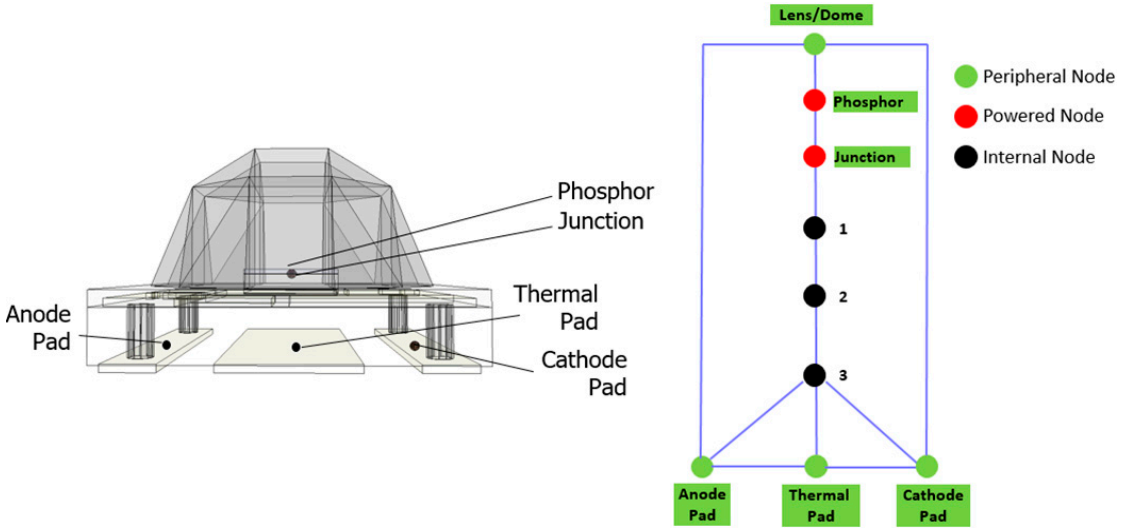
In the Delphi4LED project two methods for chip level multi-domain modelling and simulation were developed: A quasi black-box model of LEDs was proposed through appropriate extension of the built-in diode model of generic Spice solvers, on the one hand; while on the other hand, a new Spice-like LED model has also been proposed that is more closely based on the physics of today's heterojunction based multiple quantum well structures of high power LEDs [7]. Both models have been implemented as LTspice circuit macros and the model equations were also implemented in form of Visual Basic macros aimed at the implementation in an Excel spreadsheet based luminaire design calculation too [7]. Both implementations share the same set of model parameters that can be extracted straight from the measured LED characteristics as indicated in Figure 5. As a result, basic electrical, thermal, and optical behaviour of LEDs is described for the full working space in the LED application, which enables efficient simulation of LED applications on higher product integration levels.

These chip level multi-domain models have evolved from the previously published ones [14–16]. As hinted by both Figures 4 and 5, in the future, the required measurements and model parameter identification will be expected from LED vendors and the resulting LED characteristics/model parameter sets reported in a standardized format so that they can ultimately be used in a luminaire design tool or directly integrated in simulation tools in a way outlined in [5,7] and [8].

2.2.2. Digital Twin of the LED Package

In the Delphi4LED project, dynamic compact thermal models (DCTMs) of the LED packages are created (see Figure 6b).

The process of creating thermal digital twins of the LED packages starts with creating calibrated detailed 3D models of the LED packages (such as presented in Figure 6a) with the help of the structure functions [22]. These are dependent on, but do not explicitly require proprietary information of the LED: The detailed geometry and material properties.



(**a**) (**b**)

Figure 6. (**a**) Outlines of major shapes in a detailed 3D LED package model; (**b**) topology of the corresponding LED package dynamic compact thermal model (node J represents the LED junction; every internal node also represents a thermal capacitance which are omitted here) [8].

According to the original DELPHI methodology standardized in the electronics cooling simulation industry [23] and also in our present approach, compact thermal models are identified through an optimization process [8] using calibrated detailed thermal models [22].

These are later used in luminaire level analysis (following the hierarchical approach proposed in [20] and [21]) as the actual digital twins of the LED packages representing their true thermal behavior.

A package DCTM connected to a chip level multi-domain LED model is the ultimate digital twin of a packaged LED, provided e.g. as a Spice netlist (see Figure 3). For the detailed description of the methodology of creating LED package dynamic compact thermal models refer to the paper of R. Bornoff [6] published in this special Journal issue.

2.2.3. Secondary Heat Source: Phosphor

As hinted by Figure 6a, in case of phosphor converted white LEDs, the phosphor plays a significant role as secondary heat source which cannot be neglected [24]. Especially when the phosphor layer is thick and/or has low thermal conductivity, the energy loss and the corresponding temperature rise in the phosphor cannot be lumped with the dissipation and the temperature of the LED's pn-junction. Besides that, further optical losses also need to be accounted for and modelled. On the following we provide a brief summary of the results achieved within the Delphi4LED consortium.

The light trapped in the dome and light conversion losses in the phosphor create secondary heat sources P_{hC} and P_{hD} inside an LED package (Figure 7). The package level light extraction efficiency may be as low as 65% for LEDs with flat lenses. Thus, up to 35% of the light emitted by the pn-junction may be trapped in the package that is converted into heat. These additional, secondary heat sources have a significant impact on the structure functions [24–26] identified from the temperature transient measured at the LED's junction, thus, affect the accuracy of the calibration of the detailed 3D model of the LED package. Therefore, to properly calibrate the thermal parameters of the main heat-flow path, these secondary heat sources have to be accounted for.

The part of the junction temperature transient response associated with the smallest thermal time-constants is known to be dependent on the geometrical features and thermal parameters of the die. As a consequence, any heat generation in the phosphor has negligible effect on the part of the structure function prior to the die attach [24–26]. To account for the thermal effect of the phosphor,

the following method is used to calibrate the 3D finite element model and separate the main and the secondary heat sources [24]:

1. Define the precise chip substrate geometry with x-ray measurements.
2. Assign arbitrary thermal properties of the chip substrate and of the dome materials (within an expected final range).
3. Calibrate the P_{hJ} power source by matching the initial junction temperature transient response of the model to the measured one.
4. Define the secondary heat source power as the difference between, P_{hJ} and the measured heat total dissipation, P_h.
5. Perform a calibration of the thermal properties of the rest of the model.
6. Both the heat generated in the phosphor and the lens must be calibrated by fitting the long time-constants part (0.01 s < t < 10 s) of the time-constant spectrum of the transient response, or, in other words, by fitting to the "tails" of the structure function.

This methodology prevents an unphysical calibration of the thermal parameters that might be due to the significant presence of the secondary heat sources within an LED package.

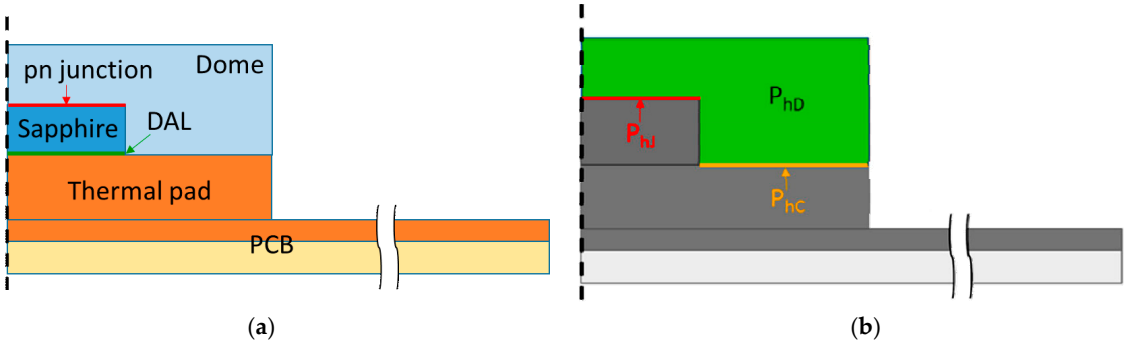


Figure 7. (**a**) Cross section of an LED package (DAL stays for die attach layer); (**b**) The different heat generating regions (heat sources) in the model.

2.2.4. Variability Assessment of the LED Digital Twin

In an industrial environment, LEDs do not have perfect characteristics; particularly at package level which manufacturing process is less well controlled than the semiconductor part chip level. Their variability might have a significant impact on the product performance. Variability among the different LED samples was also investigated [27–31]. In our actual study 11 royal blue LED samples and 11 samples of their phosphor converted white counterparts (LED having the blue peak at the same wavelength as the peak wavelength of the royal blue) have been measured and modelled. One sample with a die attach failure, as an obvious outlier was later omitted from the statistical analysis of the thermal test results.

Methods to assess the variability of the thermal properties of LED packages have been proposed. One approach uses a rough, step-wise approximation of the structure function (e.g., by means of a Cauer-type RC ladder with about a dozen stages) [28], see also Figure 8a. Based on this, a Monte Carlo simulation technique was developed to study the possible changes of the $Z_{th}(t)$ thermal impedance curves resulting from the local thermal resistance variations along the heat-flow path. The results are histograms about the distributions of the values of the local partial thermal resistances of the different heat-flow path sections (Figure 8b) and the transient temperature responses at the different locations of the heat-flow path, represented by the different nodes of the ladder model (Figure 8c).

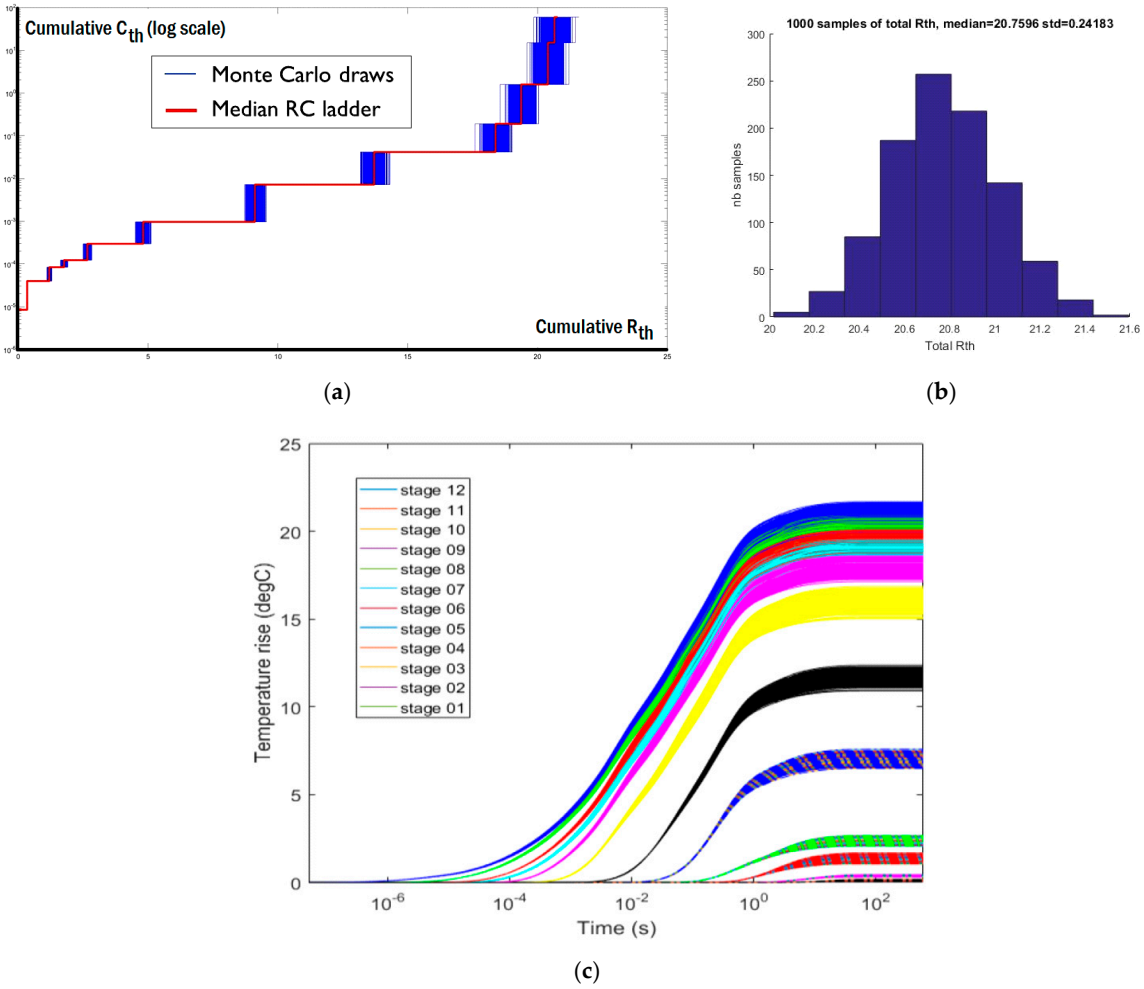


Figure 8. (**a**) Step-wise approximation of the structure function of the "median" sample of a population of 11 royal blue LEDs with Monte Carlo modelled scatter of the individual partial thermal resistances of the heat-flow path; (**b**) The histogram of the simulated value distribution of one of the stages RC ladder model of the structure function; (**c**) Simulated transient responses at the different nodes of the 12-stage RC ladder model of the heat-flow path, for all Monte-Carlo draws of local thermal resistance values of the heat-flow path sections [28].

Another method derives a new representation of the heat-flow path from the structure function which presents the changes of the local thermal resistance [29,30].

Variability of the isothermal IVL characteristics is also studied, see Figure 9. The statistical analysis of the measured isothermal IVL characteristics of the same 11 royal blue and 10 phosphor converted white LEDs that have been studied from thermal point of view is in progress, the first results are provided elsewhere [31].

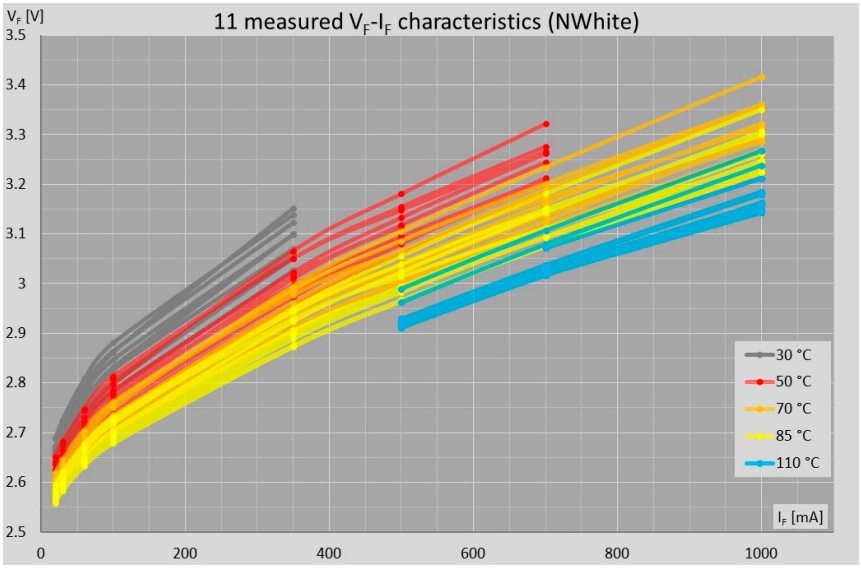


Figure 9. Isothermal forward voltage – forward current characteristics of 11 royal blue LED samples, measured at different junction temperatures between 30 °C and 110 °C.

2.3. Using the LED Digital Twin for Real Design Tasks

The advantage of the compact models is that they no longer carry proprietary information of the LED vendors, thus, LED vendors can share them with end-users without sharing their sensitive IP. A package DCTM connected to a chip level multi-domain LED model is the ultimate digital twin of a packaged LED, provided e.g., as a Spice netlist or implemented in a simple Excel spreadsheet based "luminaire design calculation tool" [5]. In our prior publication [5] we presented a simple application use-case, the design of a "10 W outdoor LED luminaire". In the following we briefly describe a design task where the LED digital twin embedded in a "calculation tool" was used to perform a more complex optimization task of a new light engine aimed as an LED based replacement of "70 W high-pressure sodium (HpS) lamps".

2.4. Modelling and Simulation of LED Modules

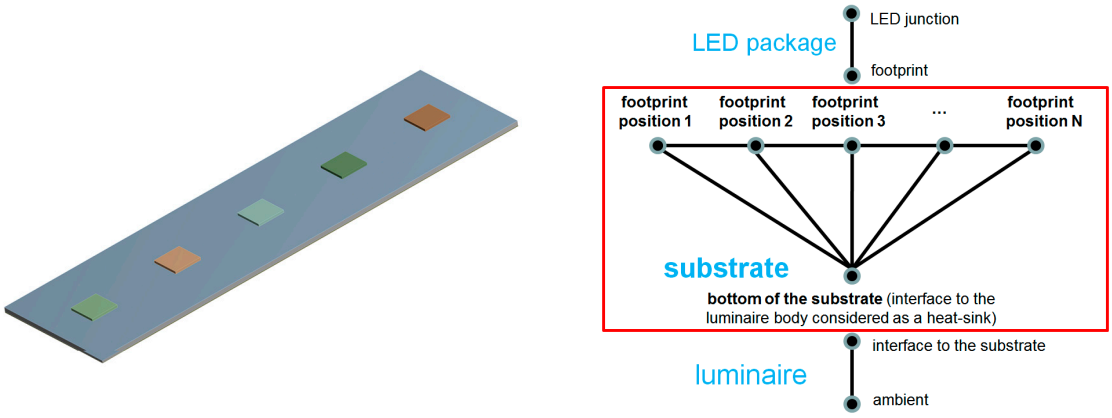
On the way towards multi-domain modelling and simulation of a complete LED based application, like a "70 W HpS lamp replacement" LED based solution, the next step level in the bottom-up hierarchy is an LED module realised on a substrate such as a printed circuit board (PCB). The quoted example, the "70 W HpS lamp replacement" LED light engine is quite a complex one, containing the LED driver electronics, the cap fitting into an Edison-type socket on one end, and proper cooling assembly on the other end. The middle part of this light engine is a complex LED assembly that mimics the light emission of the discharge tube of the sodium lamp, both in terms of the emitted total luminous flux and in terms of the spatial distribution of the emitted light. This LED assembly consists of several, identical PCB modules, carrying multiple LED packages. Thus, the corner stone of the design of this new light engine is the modelling such a PCB substrate populated with LED packages where the heat transfer from the packages towards the ambient takes place through the package footprints as thermal interfaces towards the PCB. The heat is dissipated by the LEDs then is transferred through the bottom side of the PCB substrates towards the light engine's cooling assembly from which the heat is finally transferred to the environment by convection. Now we restrict our discussion to the modelling and simulation of such a PCB module.

We set up a model in which we could easily vary the LED type, the number of LEDs used, and the properties of the substrate (e.g. different types of PCBs) during the product design optimisation phase. The properties of interest in such a system are the solder temperatures, the junction temperatures, and the "hot lumens" of each LED. "Hot lumens" is a sloppy expression widely used in the English

technical language of solid-state lighting, to refer to the emitted total luminous flux of an LED or LED based light source at the operating junction temperature of the device under application conditions.

A fully parametrized model with arbitrary dimensions was created including a 3-layer (or less) PCB substrate with arbitrary dimensions and thermal conductivity, dummy LED footprints placed on top to provide the interface area for the compact models of the LED packages, through which LEDs' heat dissipation is conducted towards the ambient. The number of dummy LEDs can vary, potentially filling both x- and y-directions. The 3D model of the physical structure of the PCB substrate is shown in Figure 10a. Figure 10b illustrates the compact thermal model of such a substrate that has been used in the "design calculator tool" implemented as an Excel based application already used with success for a simpler design [5].

In our present example, the PCB substrate is considered as a single thermal component (described by a multi heat source compact model) and the luminaire body as a heat-sink is considered as another component (modelled by a single, equivalent thermal resistance to the ambient), such as shown Figure 10b. This way, libraries of substrates made of different materials and with different designs (copper coverage, footprint layout, etc) and luminaires with different thermal features can be created for subsequent system level design and optimization.



(**a**) (**b**)

Figure 10. (**a**) an LED module with 5 LEDs; (**b**) the multi heat-source compact thermal model of the substrate (in red frame). The luminaire is represented in the overall system model as a single substrate-to-ambient thermal resistance, LED package thermal models are connected to the substrate model at the nodes corresponding to the LED footprint areas (coloured rectangles in Figure 6b).

For each LED module (a PCB populated with the chosen type and number of LED packages, considered as an elementary light source in the final light engine), following the method presented in [20] and [21] first the so called thermal characterisation matrix is created which is transformed into a Spice compatible thermal resistance network, as follows:

1. Run individual finite element model (FEM)-calculations for each LED-position assuming a unit heat dissipation at the footprint position and fixed temperature at PCB bottom interface towards the ambient (see Figure 10).
2. Generate a matrix of response temperatures at each footprint position for all cases. The resulting matrix is the so called $\mathbf{R}^*_{th}$ steady-state thermal characterisation matrix, that is specific to the given layout arrangement of the LED package footprints and represents the strength of the thermal coupling among the footprints and between each footprint and the ambient.
3. Using the algorithm described in [19] convert this $\mathbf{R}^*_{th}$ thermal characterisation matrix to a matrix of real thermal resistances that can also be exported as a real, Spice netlist of resistances. Complete this thermal resistance model with the junction to footprint thermal resistance of the chosen LED package type.

4. Convert the thermal resistance matrix corresponding to the above thermal resistance network to a solvable heat transfer coefficient (HTC) matrix. This matrix will represent the LED chips' 3D thermal environment.
5. This model is co-simulated with the chip level multi-domain LED model in a relaxation type scheme as follows:

    a. Matrix multiply the inverted HTC matrix with a power vector (containing all powers for each LED package footprint) to get the vector of temperature rises as a result.
    b. Execute the chip level multi-domain model for each LED instance, with the forward current and assumed ambient temperature. The model will calculate the LEDs' light output and heat dissipation.
    c. Take the new dissipation values as updates to the previous vector of dissipations and iterate until convergence is reached (i.e., the difference between the subsequent temperature/dissipation vectors shrinks below a given threshold).

6. When the convergence is reached, take the LEDs' calculated total radiant/luminous flux and junction temperature values and the footprint (solder joint) temperatures as final output.

2.5. The Overall Workflow

As seen in Figure 5, the entire workflow is divided into three major steps:

I. Characterisation/measurement (using a JEDEC JESD51-51/51-52 and CIE 127:2007/225:2017 compliant, combined thermal, and radiometric/photometric LED test system) in order to gain the right set of isothermal current-voltage-flux characteristics of LED packages. This step is ideally performed by the LED vendors and the obtained LED characteristics are published in an electronic LED datasheet, in a machine processable format (see also Figure 4).
II. Extract parameters for the chip level multi-domain LED model as well as identify the thermal boundary condition independent dynamic compact thermal model of the LED package. The chip and package models combined represent the multi-domain behaviour of the LED package by means of a compact model that should part of the model library of an LED application level simulation system. Ideally these model parameter identification steps are also performed by LED vendors but in cases when such models are not yet available, LED testing laboratories should also be able to provide such models.
III. Create the compact models of the LED modules by combining LED package models taken from the above libraries (ideally provided by LED vendors or LED testing laboratories) with the design specific compact thermal models of the module substrates or luminaires (or both). The inputs for such substrate/luminaire models are the electronics and mechanical CAD models (PCB electrical layout models/3D solid models) of the modules and luminaires. A substrate/luminaire compact thermal modelling tool can convert these models into the right compact thermal models. For smaller designs the thermal characterisation matrix based method outlined above is feasible and is relatively easy to implement. For larger designs however, using model order reduction techniques might be considered [30–33].

The Delphi4LED approach provides a good handshake between the semiconductor industry (represented by LED vendors) and the lighting industry (represented by the luminaire designers/manufacturers). Each have a role to play in achieving more reliable and faster product designs: The LED vendors by providing the LED characteristics in the form of electronic datasheets and eventually the LED digital twins, the luminaire designers/manufacturers being able to use these data in their own, Industry 4.0 like design workflows and if the LED compact models are not provided, being able to extract them from the e-datasheets provided by the LED vendors.

In the third phase pre-characterisation of different module substrates and different heat-sink designs are performed by the luminaire manufacturers. This way their compact thermal models

(thermal N-port models for the substrates, equivalent substrate-to-ambient thermal resistances for heat-sinks, see also Figure 10b) are also created and included in model libraries.

In the proof of concept implementation of the above workflow an Excel a spreadsheet application was created [5] into which both chip level multi-domain LED model parameter sets, LED package thermal resistances (as simplified LED package compact thermal models) as LED package model libraries and substrate/heatsink thermal models also as library items were included.

The user interface of this application allows setting major design goals (total luminous flux to achieve in this demo, see the blue field in Figure 11) and design constraints (foreseen ambient temperature, maximum allowed junction, and solder point temperatures; maximum allowed total forward voltage – the orange fields in Figure 11). The user (luminaire designer) can select the number of LEDs, substrate, and heat-sink types from pull-down menus and can set the efficiency of the luminaire optics and the total forward current provided the LED driver as input (light-green fields in Figure 11). (For the sake of simplicity it was assumed that all the LEDs of the module investigated were electrically connected in series, forming a string of LEDs.)

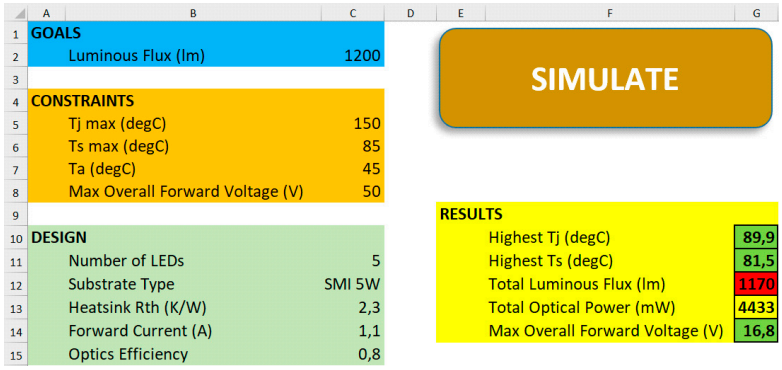


Figure 11. An Excel spreadsheet based application (a simple luminaire design tool) to support assessing basic luminaire design alternatives through virtual prototyping using Delphi4LED style compact models [3]. A "green" result means that the given target is met/constraint is not violated; "red" indicates failing a design target or violating a design constraint.

The complete digital twin of an LED luminaire is obtained by combining the luminaire (compact) thermal model with the digital twin of the LED package (chip level multi-domain model completed with the package DCTM). With such a digital twin of the complete luminaire as a virtual prototype, luminous flux calculations of different design versions can be performed under different environmental conditions that are close to the foreseen application conditions.

2.6. Implementation and Personas in the Overal Design Flow

Both within the Delphi4LED consortium and in real life, we identified two different company profiles where daily design practice significantly differs due to company cultures and available technical/financial resources. We distinguish between small and medium size companies (referred to as SMEs) and big, international companies (referred to as Majors).

2.6.1. From LED Physical Device to Multi-Domain Compact Model

LED vendors or certified expert labs play a key role in the characterisation and measurements of LEDs aimed as source of input for LED multi-domain modelling. The general vision is that these test date will be reported through electronic LED datasheets. Such e-datasheets, as vendor neutral ways of data exchange can be processed by appropriate software tools by these entities in order to extract the LED MDCM and store the models in a standard, LED vendor and software tool independent data exchange format (e.g., xml). Such LED models will be stored in a library of LED digital twins. Figure 12 shows the design process associating a set of libraries to a Luminaire Design Tool (LDT).

If a certain LED multi-domain digital twin cannot be obtained from an LED vendor or from an independent, certified/accredited LED testing laboratory, the luminaire designers/manufacturers will have to extract the necessary models themselves, taking the LED e-datasheet as input. This optional step is common to both SME and Majors.

2.6.2. From Luminaire Requirements to Final Application

In the overall Delphi4LED workflow of Figure 5 LED application designers (luminaire designers at luminaire manufacturers) are responsible for creating their own sets of libraries of heatsinks, optics, substrates and the matching (footprint) of the LED models (Figure 12).

The product designer will gather the luminaire requirements from the lighting designer matching the end application conditions (e.g. dimensions, emitted total luminous flux, light quality metrics such as correlated colour temperature, and/or colour rendering index, other optical requirements, such as light distribution pattern) and translates those requirements into critical to quality (CTQ) parameters.

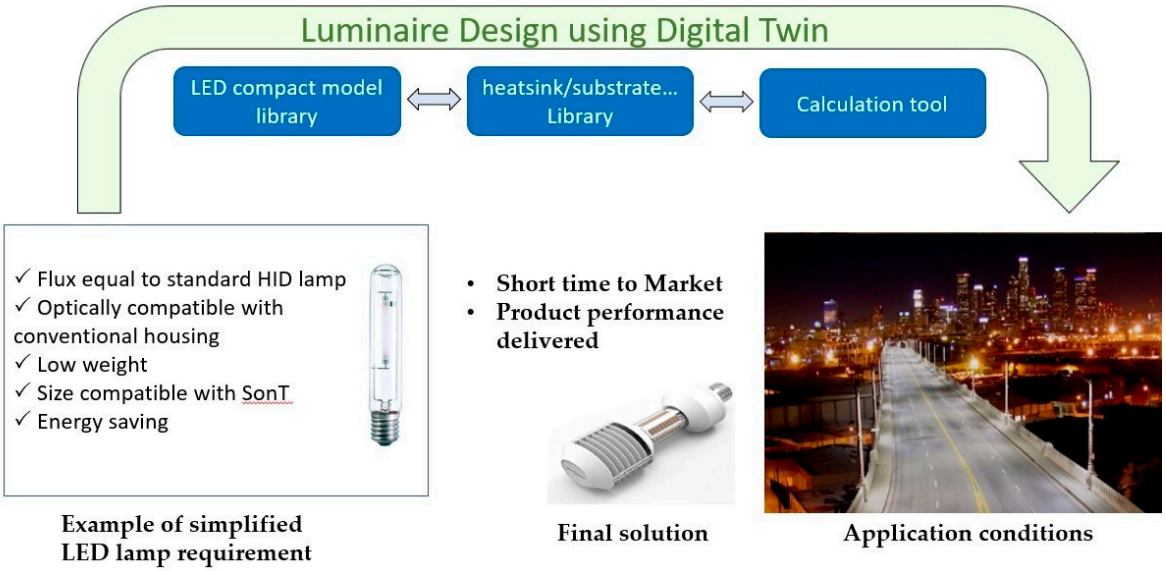
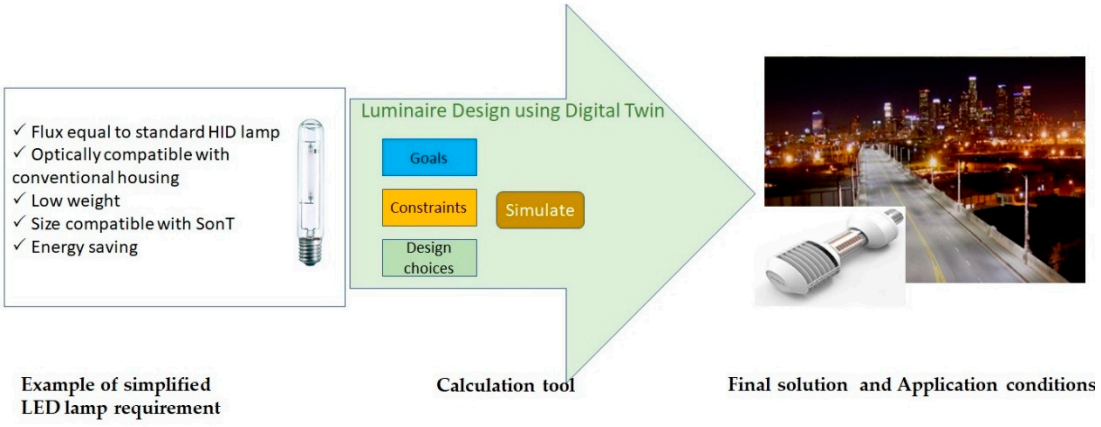


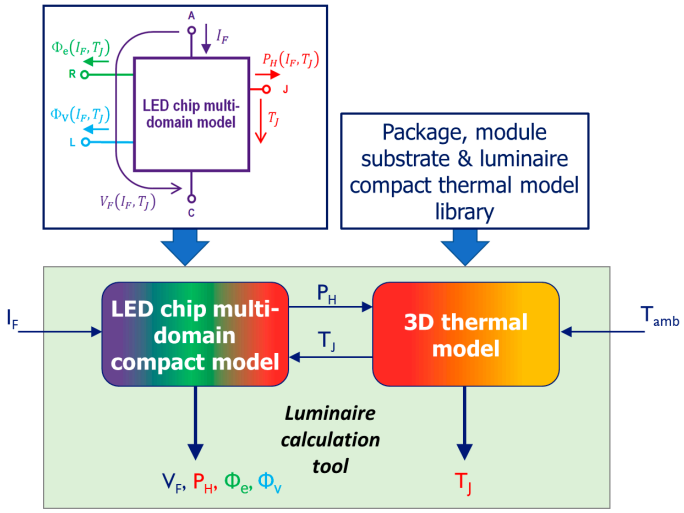
Figure 12. Computerized workflow: From luminaire requirement to final application with sets of model libraries.

Those parameters are split into three categories: Goals (equivalent to target performance), application constraints, and design choices (see Figure 13a). Goals set the target performance; such as luminous flux. Goals to achieve must fit the application constraints; which in turn are indicators for e.g., lifetime performance (maximum allowed temperature of the solder joints, junctions), limitations of the driver (maximum overall forward voltage), and ambient temperature. Design choices represent the degrees of freedom of the design. Parameters are typically LED type options (e.g., XPG3 and NF2L757DRT-V1) and corresponding forward current, substrates choices (e.g., FR4, MCPCB, and Cem3), optics efficiency, and cooling solution.

The luminaire calculation tools build up the system level model of a complete luminaire by mapping the design choices entered to items taken from the design libraries (Figure 12). The package and chip level model of the chosen LED is also taken from a library (ideally provided by LED manufacturers) and are combined with the other items, to create the internal, system level representation that is suitable for simulations (Figure 13b). This combined system model is executed when the "Simulate" button is pressed. If the user (LED application designer) changes a design choice, the luminaire calculation tools automatically updates the luminaire's system level model with the corresponding compact model taken from the model library.



(**a**)



(**b**)

Figure 13. Computerized workflow: (**a**) from luminaire requirement to final application, (**b**) representation of the system in the luminaire calculation tool.

2.7. Case Studies

Two test cases are considered for assessing ease of use, performance of the "digital twins", impact of a large number of LEDs and to demonstrate that the approach of the Delphi4LED project is tool agnostic. Figure 14 shows the demonstrators. Demonstrator a) is used to compare SME versus Majors approach, while demonstrator b) is used to assess applicability to a large number of LEDs and its tool agnosticism.

(**a**) (**b**)

Figure 14. Demonstration experiment proposed (not on scale): (**a**) "10 W outdoor LED spot" luminaire typology; (**b**) "70 W high-pressure sodium (HpS) replacement" LED lamp.

Experiment (A)

Based on this classification of foreseen users of the tools and methods developed within the Delphi4LED project, we set up two different demonstration experiments. One of the consortium members played the role of an SME and used the SME-type implementation of the overall workflow shown in Figure 5 (using the limited set of means usually available in small companies); another consortium member acted as a Major (i.e., large company) and used testing, modelling, and simulation tools typically available at a Major company. In this paper we present the SME style implementation of the proposed Delphi4LED workflow.

For the purpose of the study, two independent members of the consortium (Company A and B) played the role of developers and an independent industrial photometric test laboratory, respectively. Table 1 presents the four design styles assessed for SMEs and Majors. In this demonstration experiment, Company A executed the design and physical prototyping phase; and Company B executed the characterisation and final tests phase.

Table 1. Summary of design and development styles (workflows) followed during the project demonstration experiment of Delphi4LED.

Type of Design Flow	Concept/Development	Design and Prototyping	Characterisation and Final Tests
Majors	"Old process": tests/characterisation based optimization	Company A	Company B
Majors	"New process": compact model based optimization	Company A	Company B
SMEs	"Old process": prototyping and testing	Company A	Company B
SMEs	"New process": compact model based virtual prototyping	Company A	Company B

The assessment was done using Version 12.2 of the commercially available computer fluid dynamic (CFD) simulation tool Simcenter Flotherm software from *Mentor, a Siemens business* and a spreadsheet based luminaire calculation tool (realised in Visual Basic) and embedded in an Excel spreadsheet. The CFD tool was used to create the compact model library items corresponding to different substrate layouts and equivalent luminaire heatsink thermal resistances.

The design processes were monitored for each development style. The following performance indicators of the process were tracked: (1) Costs of development (time spent, incurred personal costs) for the realisation of virtual and physical prototypes samples, as well as (2) costs related to laboratory measurements and characterisation.

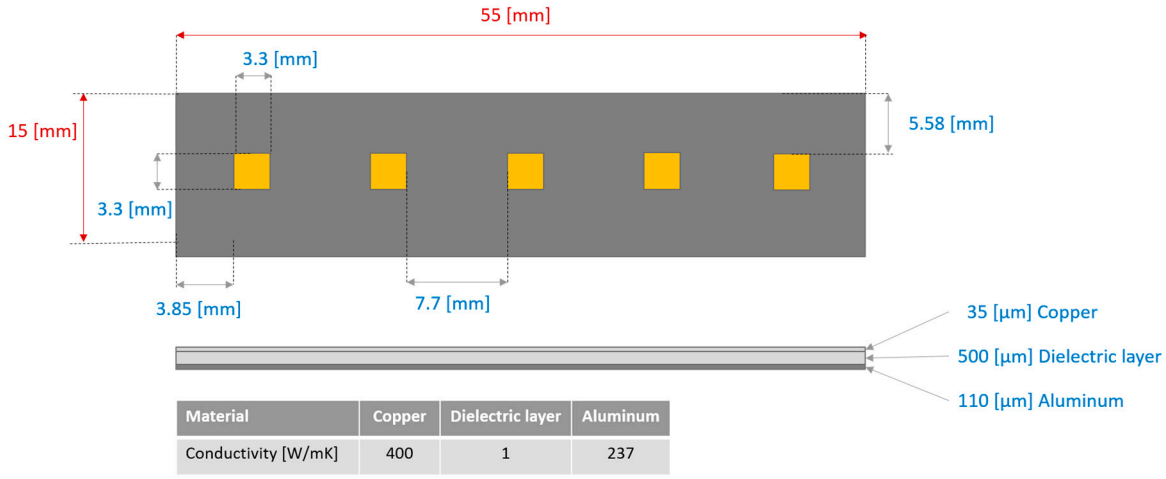
Experiment (B)

This experiment was performed to demonstrate how the Delphi4LED workflow is applicable to a real product development in a Major company. The chosen example was a high-intensity-discharge (HID) replacement lamp for street lighting application. The Delphi4LED virtual prototyping was used optimise the product by assessing different numbers and types of LEDs with which the total luminous flux target could be met. The purpose of this experiment was to demonstrate the ease of use when scaling the number of LEDs/applied forward current to meet the design specifications and to demonstrate the software tool independence of the proposed design flow.

In this experiment the models were created using the commercial finite element simulation tool ANSYS Version 17.2 (while in Experiment A the Simcenter Flotherm tool from Mentor was used).

The Ansys Parametric Design Language (ADPL) feature of ANSYS allowed the integration of both the LED package and the multi-domain chip level compact model to be solved in LTspice, in a similar relaxation type electro-thermal co-simulation scheme as depicted in Figure 13b. (Refer to [7] for details on the chip level multi-domain LED models aimed at different types of the implementation schemes of the electro-thermal co-simulation). This way the light output of the given LED configuration was obtained.

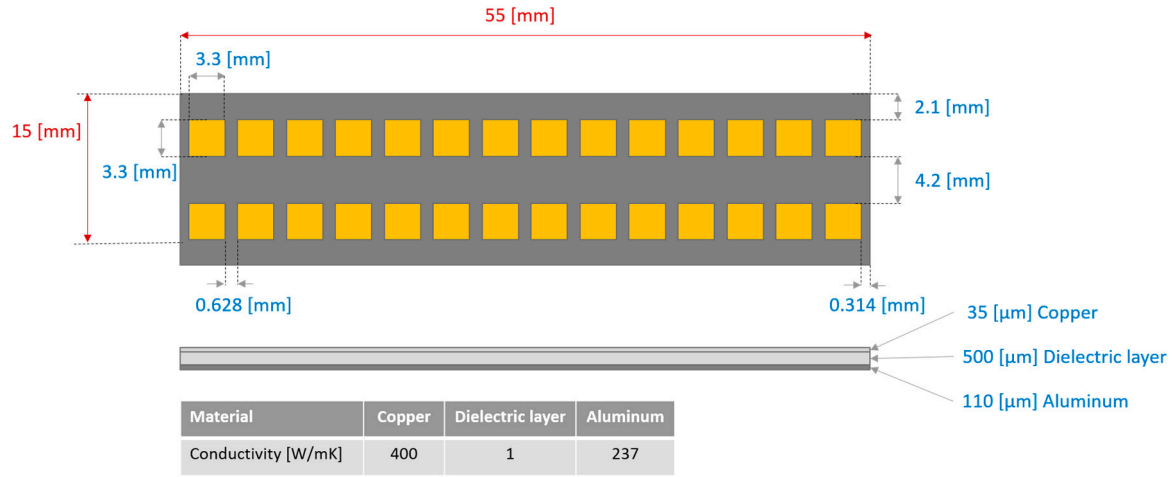
The middle part of the light engine of the HpS lamp replacement solution is composed of six symmetrically assembled LED modules. Due to the symmetry, it is enough to study only one single LED module. Figure 15 shows one of these six identical segments of the light engine of the lamp for two scenarios denoted by (x) and (y). The question was: Which combination of number of LEDs and forward currents for two different LED types meet the design goals and design constraints the best.



Material	Copper	Dielectric layer	Aluminum
Conductivity [W/mK]	400	1	237

(**a**)

Figure 15. *Cont.*



Material	Copper	Dielectric layer	Aluminum
Conductivity [W/mK]	400	1	237

(**b**)

Figure 15. One segment (not on scale) for Experiment b: (**a**) scenario (x) with details of the printed circuit board (PCB) for 5 LEDs powered by high forward current; (**b**) scenario (y) with details of the PCB for 22 LEDs powered by low forward current.

The designs were assessed with the following thermal boundary conditions:

1. Bottom temperature of the board at 85 °C.
2. Bottom temperature of the board at 45 °C.
3. Junction temperature of the board at 120 °C.

In scenario (y) with 22 LEDs is thermal coupling between adjacent LEDs was expected to be higher. For both scenario (x) and (y), the total luminous flux of the module and maximal power conversion efficiency were the design goals.

3. Results of Case Studies

This section presents the results of each key steps and related implementation in the overall Delphi4LED workflow of Figure 5.

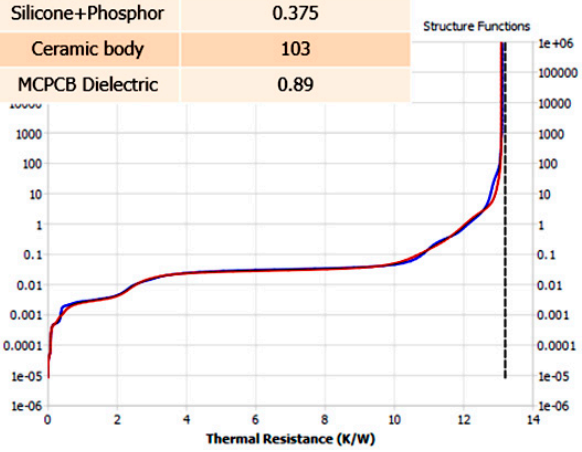
3.1. Results of the Measurements and Modelling of LEDs

In this initial step, which is identical for both SMEs and Majors, the designer gathers input from LED suppliers and makes a pre-selection of sub-set of LEDs. In both demonstration experiments XPG3 LEDs from Cree were selected and used; in Figure 16 we show a few results of the measurements and modelling, performed by consortium members specialized in LED testing and modelling, mimicking the role of an LED supplier. (Such data are preferably input from LED suppliers or certified independent characterisation laboratories.)

		XPG3_01	XPG3_02	XPG3_03	XPG3_04	XPG3_05
Sample:						
Max Vf error:		0%	1%	0%	0%	0%
Max Fi_e error:		1%	1%	1%	1%	1%
Max Fi_v error:		1%	1%	1%	1%	1%
UT	=	0,0296	0,0296	0,0296	0,0296	0,0296
I0	=	7,6395E-24	6,9812E-24	8,1736E-24	7,2375E-24	7,6335E-24
m	=	1,7354	1,7349	1,7359	1,7353	1,7358
R	=	0,1929	0,2141	0,197	0,2138	0,1973
I0_rad	=	4,0317E-23	3,4889E-23	3,4027E-23	3,3826E-23	3,1585E-23
m_rad	=	1,8150	1,8131	1,8075	1,8107	1,8089
R_rad	=	0,0190	0,021001	0,020001	0,021001	0,019001
a_el	=	-8,079E-06	-2,501E-06	-6,348E-06	1,973E-07	-3,155E-06
b_el	=	2,153E-05	1,209E-05	1,762E-05	7,854E-06	1,475E-05
c_el	=	-1,050E-06	2,362E-06	-5,003E-08	2,998E-06	-4,546E-07
d_el	=	1,326E-03	5,207E-04	1,085E-03	1,150E-04	4,845E-04
e_el	=	-4,104E-03	-2,919E-03	-3,586E-03	-2,243E-03	-2,982E-03
f_el	=	-8,353E-04	-1,348E-03	-9,861E-04	-1,462E-03	-9,515E-04
a_rad	=	-8,304E-06	-2,668E-06	-6,589E-06	2,394E-07	-3,053E-06
b_rad	=	2,209E-05	1,261E-05	1,824E-05	8,137E-06	1,492E-05
c_rad	=	-8,946E-07	2,563E-06	8,893E-08	3,154E-06	-1,960E-07
d_rad	=	1,364E-03	5,481E-04	1,127E-03	1,034E-04	4,618E-04
e_rad	=	-4,173E-03	-2,981E-03	-3,670E-03	-2,259E-03	-2,985E-03
f_rad	=	-8,187E-04	-1,338E-03	-9,643E-04	-1,449E-03	-9,417E-04
a_Kap	=	0,000	-0,002	-0,001	-0,002	-0,003
b_Kap	=	-0,057	0,320	0,123	0,326	0,463
c_Kap	=	2,306	-12,216	-5,028	-12,613	-17,489
d_Kap	=	0,000	0,002	0,000	0,002	0,002
e_Kap	=	0,081	-0,181	-0,028	-0,221	-0,324
f_Kap	=	-6,896	3,296	-0,971	5,542	8,955
g_Kap	=	0,000	0,000	0,000	0,000	0,000
h_Kap	=	-0,066	-0,082	-0,088	-0,055	-0,057
i_Kap	=	334,911	333,904	333,653	333,397	333,066

(**a**)

Thermal Conductivity	Calibrated value (W/mK)
Solder	36.7
Silicone+Phosphor	0.375
Ceramic body	103
MCPCB Dielectric	0.89



(**b**)

Figure 16. Model parameters and thermal test results for XPG3 type phosphor converted white LEDs from Cree: (**a**) Extracted sets of parameters used for a multi-domain LED chip level model [7]; (**b**) Typical representation of the junction-to-ambient thermal impedance through structure functions, used for package level modelling (model calibration based on test results).

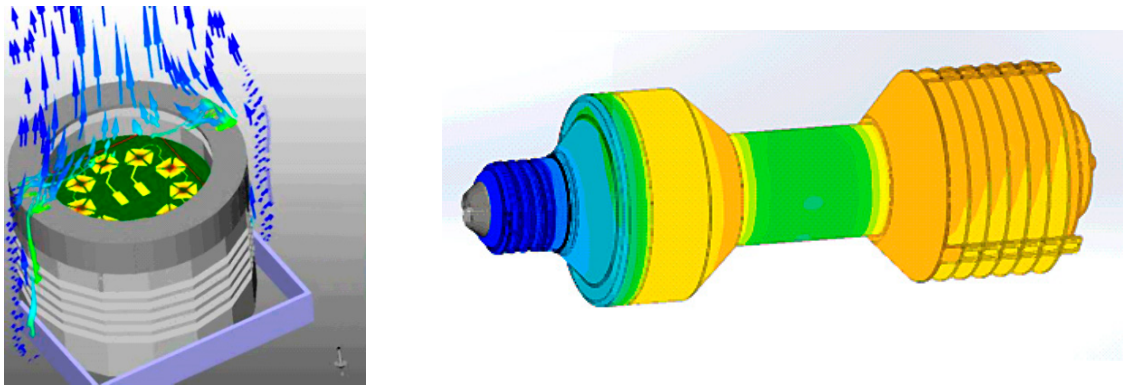
3.2. Digitial Twins of Luminaires

From the thermal point of view, a luminaire is a multi-heat-source system where the heat-sources are the LED packages with their footprints. An obvious digital twin of an LED luminaire is its MCAD model (such as shown in Figure 17). The thermal model, as a thermal only digital twin of the luminaire can be extracted from this MCAD model. A luminaire compact thermal modelling tool (as indicated in Figure 5) may use different approaches to provide the compact thermal model of the luminaire.

(**a**) (**b**)

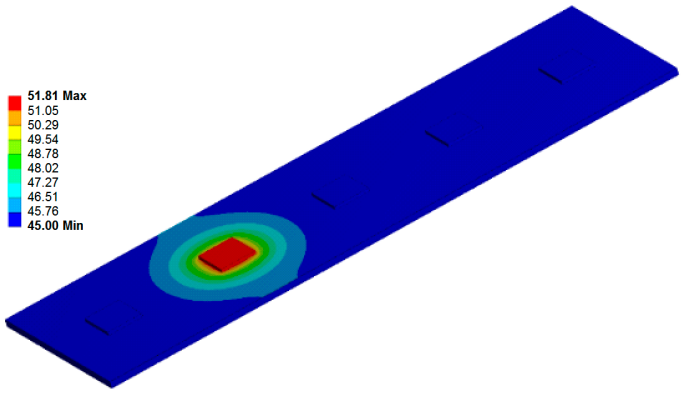
Figure 17. MCAD models of the demonstrator systems: (**a**) "10 W outdoor LED spot" luminaire typology; (**b**) "70 W HpS replacement" LED lamp.

One approach is to identify the thermal characterisation matrix of the luminaire and convert it into a Spice network model, through a series of CFD simulations, using the algorithm outlined in Section 2.4 (for details of the algorithm and for another application example refer to papers [20] and [21]). Figure 18 presents CFD simulation results of both demonstration examples. In Figure 19 CFD simulation result (temperature map) for a single run of the whole characterisation series is shown for the LED module according to scenario (x) of demonstrator b, together with the Spice netlist of the LED module. For creating the thermal compact model of the LED module substrates or complete luminaires, reduced order modelling techniques could also be used [32–35].



(**a**) (**b**)

Figure 18. Computer fluid dynamic (CFD) simulation of the luminaires shown in Figure 14. The detailed simulation models were created from the MCAD models shown in Figure 17: (**a**) "10 W outdoor LED spot" luminaire typology; (**b**) "70 W HpS replacement" LED lamp.




```
*XPG3board   Rjs
Rjc1 Junction1    Pos1   3.47
Rjc2 Junction2    Pos2   3.47
Rjc3 Junction3    Pos3   3.47
Rjc4 Junction4    Pos4   3.47
Rjc5 Junction5    Pos5   3.47

*Substrate
RPos1MCPCB_bot Pos1 MCPCB_bot 13.0789793
RPos2MCPCB_bot Pos2 MCPCB_bot 11.4229319
RPos3MCPCB_bot Pos3 MCPCB_bot 10.7096081
RPos4MCPCB_bot Pos4 MCPCB_bot 11.3707428
RPos5MCPCB_bot Pos5 MCPCB_bot 13.043822
RPos1Pos2 Pos1 Pos2 157.222636
RPos2Pos3 Pos2 Pos3 358.358111
RPos3Pos4 Pos3 Pos4 354.782076
RPos4Pos5 Pos4 Pos5 152.092579

*Luminaire to ambient
R_MCPCB_Bot_0    MCPCB_Bot   0   1.99062108
```

(**a**) (**b**)

Figure 19. Thermal characterisation and compact thermal modelling of the LED module of the light engine of demonstrator B, according to scenario (x): (**a**) temperature map obtained by a CFD simulation in the series of simulations run to obtain the thermal characterisation matrix, $\mathbf{R}^*_{th}$; (**b**) Spice netlist of the steady-state compact model of the LED module (Substrate section).

3.3. Luminaire Level Results

The first results of Experiment A were reported in [5] together with the description of a pilot implementation of the overall Delphi4LED workflow. In this demo implementation, a set of models has been created and combined into an Excel spreadsheet application, aimed as a simplified design/virtual prototyping tool for SMEs. Based on prior characterisation of LEDs foreseen for the project demonstrators consortium members specialised in LED testing and modelling created a Spice-like chip level multi-domain models [5] and extracted the model parameters (see Figure 16a). The DCTM of the package was also created. In both cases variability among the different LED samples was also considered in a simplified way: Instead of creating Monte Carlo models from parameter distributions identified for a larger population of LEDs (as suggested in [26–29]) the model parameter sets obtained for the actual measured LED samples (five different ones, see Figure 16a) were randomly used.

In the subsequent paragraphs of this subsection we focus Experiment B and the version of the Delphi4LED workflow used by a Major company.

Figure 19 illustrates the thermal characterisation and compact modelling of the LED module of demonstrator b, according to scenario (x) (five LEDs driven by high current). Figure 19a is a temperature snapshot from the series of CFD simulations performed as part of the thermal characterisation of the module substrate (as outlined in Section 2.4 and detailed in papers [20] and [21]). Figure 19b presents the complete luminaire level Spice netlist that corresponds to the simplified thermal modelling approach shown in Figure 10b. The substrate model shown corresponds to the thermal boundary condition of fixing the bottom surface of the PCB substrate at 45 °C. For the geometric dimensions of the LED module in this example, see Figure 15a.

The results both for scenario (x)—5 LEDs operated at a forward current of 500 mA—and for scenario (y)—22 LEDs operated at a forward current of 100 mA—were obtained for two different LED types and different temperatures of the bottom surface of the PCB substrate. Tables 2 and 3 provide the simulation results for the Cree XPG3 type LEDs at 45 °C and 85 °C, respectively, and Tables 4 and 5 provide the results of for the Nichia NF2L757DRT-V1 type LEDs, also for 45 °C and 85 °C, respectively.

In both scenarios (x) and (y), the target of the emitted total luminous flux of 6000 lm for the entire lamp can be achieved. Note, that LED efficacies and junction temperatures are different which potentially leads to different energy consumption and different lifetime of the lamp, if one or the other design variant is realized. (Red colour in the tables indicates that the design target is failed.)

Table 2. Results for XPG3 4000K CRI 70 high power LEDs on PCB—temperature at the bottom of the PCB: 45 °C. (Green colour indicates that the design target is met.)

Calculated Property	5 LEDs; I_F = 500 mA	22 LEDs; I_F = 100 mA
Solder point temperature [°C]	51.6	46.9
Junction temperature [°C]	54.3	47.3
Light output per PCB [lm]	1056	1049
Total Light output [lm]	6336	6294
Efficacy [lm/W]	150	180

Table 3. Results for XPG3 4000K CRI 70 high power LEDs on PCB—temperature at the bottom of the PCB: 85 °C. (Green colour indicates that the design target is met.)

Calculated Property	5 LEDs; I_F = 500 mA	22 LEDs; I_F = 100 mA
Solder point temperature [°C]	91.7	86.9
Junction temperature [°C]	94.4	87.3
Light output per PCB [lm]	1000	1004
Total Light output [lm]	6001	6024
Efficacy [lm/W]	144	174

Table 4. Results for Nichia NF2L757DRT-V1 4000K CRI 80 mid-power LEDs on PCB—temperature at the bottom of the PCB: 45 °C. (Green colour indicates that the design target is met, red colour means target failed.)

Calculated Property	5 LEDs; I_F = 200 mA	22 LEDs; I_F = 60 mA
Solder point temperature [°C]	51.8	47.6
Junction temperature [°C]	61.1	49.7
Light output per PCB [lm]	664	1008
Total Light output [lm]	3984	6050
Efficacy [lm/W]	105	136

Table 5. Results for Nichia NF2L757DRT-V1 4000K CRI 80 mid-power LEDs on PCB—temperature at the bottom of the PCB: 85 °C. (Green colour indicates that the design target is met, red colour means target failed.)

Calculated Property	5 LEDs; I_F = 200 mA	22 LEDs; I_F = 60 mA
Solder point temperature [°C]	91.6	87.6
Junction temperature [°C]	100.8	89.7
Light output per PCB [lm]	818	951
Total Light output [lm]	3708	5707
Efficacy [lm/W]	101	131

4. Discussion

Benefits of using LED/luminaire digital twins in an early development phase were assessed considering the different working styles of SMEs and Major companies. The proposed, tool agnostic approaches were tested with multiple LED types in different demonstration experiments.

4.1. Benefit Observed in Experiment A

Table 6 compares the four design processes (SME "old process"/"new process" and Major "old process"/"new process") with comparison of relative costs of the development at the given type of company. Note, that the absolute total costs at SMEs and Majors are different and is also country specific, therefore fair comparison of design efforts can only be given in terms of relative costs where the basis is the total cost of development using the "old process" of product design (without virtual prototyping with digital twins).

Table 6. Cost comparison between the old process and the new Delphi4LED processes to design and manufacture the first prototype of a luminaire. The final total (relative) gains are indicated by boldface.

Main Design Costs	Major "Old Process"	Major "New Process"	Gain
Personal costs [1]	0.819	0.502	39%
Material costs [1]	0.055	0.028	48%
Testing [1]	0.126	0.045	65%
Total [1]	1.000	0.575	**42%**
Main Design Costs	**SME "Old Process"**	**SME "New Process"**	**Gain**
Personal costs [2]	0.896	0.633	29%
Material costs [2]	0.049	0.028	43%
Testing [2]	0.056	0.056	0%
Total [2]	1.000	0.717	**28%**

[1] Relative values compared to total costs of development in the "old way" at a Major company. [2] Relative values compared to total costs of development in the "old way" at an SME.

Based on the data gathered during our demonstration experiment roughly 30–40% overall design cost savings (see the exact values in boldface in Table 6) can be achieved by avoiding building and testing physical product prototypes and through increased efficiency of designers, using multi-domain simulations with compact models of LEDs combined with luminaires digital twin. The simulation based optimization led to a faster "time to pre-industrial sample", with a time reduction of about 30%.

4.2. Benefit observed in Experiment B

Analysing Table 2, Table 3, Table 4, and Table 5, an immediate observation is that 5 Nichia LEDs will not provide sufficient light output. Indeed, the using Cree's XPG3 LEDs assures to achieve the target luminous flux output of 6000 lm while keeping the junction temperature below 100 °C.

When usng Nichia NF2L757DRT-V1 4000K CRI 80 mid-power LEDs (considered for this case study), it can be seen, that with five LEDs of this Nichia mid-power LED type the target 6000 lm cannot be reached even when the LEDs are driven at the maximum allowed forward current of 200 mA. While in case of the modules with 22 pieces of Nichia's mid-power LEDs the LEDs are not driven at the maximum forward current: with only 60 mA of forward current the total luminous flux of the entire lamp close to the target of 6000 lm is reached.

For this specific case study, the XPG3 LEDs deliver in both scenarios (x) and (y) the targeted luminous flux at feasible junction temperatures and providing the highest system efficacy of both scenarios. The final decision between LED types, number of LEDs per module (5 LEDs, 22 LEDs, or any number of LEDs in between) will depend on the trade-off between optical performance, thermal limits, and cost.

The approach proposed allows the user, in a very short time frame, to develop very valuable insights in design choices. The case study highlighted the relation between the number of necessary LEDs and type of LED combination with system efficacy.

Finally, comparing demonstrations carried out in Experiment A (using Flotherm) with Experiment B (using ANSYS), the approach proved to be fast and accurate, independently of the software tool used: In a nutshell, tool agnostic.

4.3. Implementation of the New Digital Workflow in An Industrial Environment

Constraints of the actual industrial environment depend on the type of companies (SME versus Major). In both cases, the Delphi4LED overall workflow can be implemented in a way that best fits the company profile in question, providing ease of use by LED application designers and assuring accurate and fast results.

Experiment A was a proof of concept of the Delphi4LED methodology from LED device to luminaire design, both for SME and Major companies' industrial environment.

Experiments A and B show that results are accurate and fast, independently of the simulation tool chosen (simple Excel spreadsheet application ANSYS, Flotherm) confirming that the approach is tool agnostic.

Experiment B pushed the limits for a larger number of LEDs in a system. With the help of a parametric study, the results were obtained in less than an hour. The tedious part was to create the parametric model. Compared to the "old process", the Delphi4LED modelling and simulation provides answers to design choices early in the product development (when degrees of freedom are still high). These choice may include type and amount of LEDs, driving current, substrates, and layout configurations. In the dynamic market of lighting, this truly is a competitive advantage.

4.4. Impact on the Company Digital Footprint

Key to the success of this new LED design workflow is the availability of sets of libraries interacting with each other. The LED package libraries eventually should be provided obviously by the LED vendors, while other libraries such as module substrate, and heat-sink. Thermal model libraries, as indicated in Figure 12, are the new digital assets of a luminaire designer/manufacturer. This forms the future company digital footprint.

Figure 20 shows the input to those libraries from LED suppliers (LED e-datasheets or directly the LED digital twins) and customers (luminaire requirements). In case of SMEs, those databases are input for a spreadsheet based luminaire calculator tool. In case of Major companies, the model libraries can be directly linked to commercially available simulation tools (e.g., Flotherm, ANSYS).

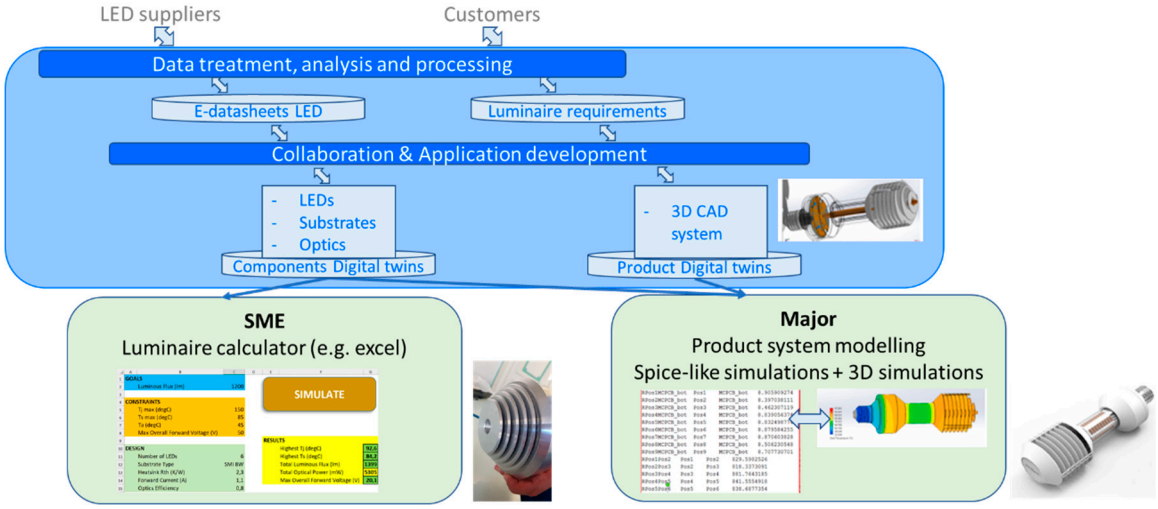


Figure 20. Digital footprint of an LED luminaire manufacturing company represented by the available design tools, libraries, and means of communications with LED suppliers and customers.

5. Conclusions

In the Delphi4LED project, new methodologies have been developed for compact modelling of LED products. The multi-domain nature of LED operation is treated on the chip level, using multi-domain LED models that can be implemented both in generic Spice circuit simulators and also as Visual Basic macros in a spreadsheet based luminaire calculation tool application. With an approach similar to the standard DELPHI methodology [25], boundary condition independent compact models of LED packages are created. These, combined with the chip level multi-domain model and the compact thermal models of module substrates and luminaires, allow a system level multi-domain simulation of an LED application. The combined chip + package + substrate + luminaire model is the "digital twin" or "virtual prototype" of a foreseen luminaire. This virtual prototype allows computer simulation assisted or computer simulation based optimization of an LED application. The methodology has been proven to be tool agnostic, tested with multiple LED systems.

Larger scale demonstrators are currently under study to validate the findings presented in this paper. Variability analysis applied to a luminaire level will also be further investigated.

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Nomenclature

LED	Light Emitting Diode
PCB	Printed Circuit Board
DAL	Die Attach Layer
MDCM	Multi-domain compact model
LDT	Luminaire Design Tool
BCI	Boundary Condition Independent
DCTM	Dynamic Compact Thermal Model
HTC	Heat Transfer Coefficient
SME	Small and Medium Entreprise
MCAD	Mechanical Computer Aided Design
P_h	Total thermal power dissipated by an LED
P_{hJ}	Thermal power dissipated in a pn junction of an LED
P_{hC}	Thermal power dissipated on the cup reflector surface of an LED
P_{hD}	Thermal power dissipated in the dome (lens) volume of an LED
$\mathbf{R}^*_{th}$	thermal characterisation matrix

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