Article

Miniature DC-DC Boost Converter for Driving Display Panel of Notebook Computer

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Abstract: This paper proposes a miniature DC-DC boost converter to drive the display panel of a notebook computer. To reduce the size of the circuit, the converter was designed to operate at a switching frequency of 1 MHz. The power conversion efficiency improved using a passive snubber circuit that consisted of one inductor, two capacitors, and two diodes; it reduced the switching losses by lowering the voltage stress of the switch and increased the voltage gain using charge pumping operations. An experimental converter was fabricated at 2.5 cm × 1 cm size using small components, and tested at input voltage 5 V ≤ V_{IN} ≤ 17.5 V and output current 30 mA ≤ I_O ≤ 150 mA. Compared to existing boost converters, the proposed converter had ~7.8% higher power conversion efficiency over the entire range of V_{IN} and I_O, only ~50% as much voltage stress of the switch and diodes, and a much lower switch temperature T_{SW} = 49.5 °C. These results indicate that the proposed converter is a strong candidate for driving the display panel of a notebook computer.

Keywords: backlight; DC-DC converter; passive snubber; voltage stress

1. Introduction

Notebook or tablet computers are powered by a Li ion battery pack [1–4]. Typically, the battery pack is composed of 2–4 Li ion battery cells. Each Li ion cell has a terminal voltage of 2.6–4.2 V depending on the charging state, so the voltage of the battery pack changes in the range of 5–17 V [5–7]. To supply power to each part of the computer, the pack voltage is converted to several voltages by DC-DC converters.

Many computers use a light-emitting diode (LED) backlight unit (BLU) for the liquid crystal display (LCD) panel. For a 17 inch panel, the voltage required to drive the LED backlight can be as high as 40 V [8]. The DC-DC boost converter for the LED BLU in a notebook or tablet computer should have a circuit topology that can reduce the overall size and weight [9–16]. The conventional boost converter (Figure 1) has the simplest structure, and can be implemented in small sizes by operating at a high switching frequency f_S. However, the switching loss increases as f_S increases, and thereby decreases the power conversion efficiency \eta_e and can cause overheating of the switch. This problem has been solved using soft-switching converters [17–21].
Soft-switching converters [17–21] use active snubbers to reduce switching loss. These snubbers are implemented using an auxiliary switch, diodes, and energy storage elements. The auxiliary switch requires a separate gate drive circuit that is controlled by a sophisticated algorithm. The snubber of Reference [17] discharges the drain-source capacitor $C_{DS}$ of the main switch before the switch turns on, so zero-voltage (ZV) turn-on of the switch is possible. The snubbers of References [18,19] force the switch current to zero before the switch turns off, so zero-current (ZC) turn-off of the switch is possible. The snubber of Reference [20] achieves ZV turn-off of the switch by reducing the rate of voltage increase during the turn-off transient, and achieves ZC turn-on of the switch by reducing the rate of current increase during the turn-on transient. However, the converters of References [17–20] have some limitations when they operate at high $f_S$; they use a resonance between an inductor ($L$) and a capacitor ($C$) in the active snubber, the inductance $L$ of $L$ should be small enough to achieve ZV or ZC switching in a short time; the current peak of the switch or diodes increases as $L$ decreases, therefore, this change increases the conduction loss and reduces the maximum output power. In the converter of Reference [21], the capacitance $C_{DS}$ discharges through $L$ of the snubber when the auxiliary switch turns on. The ZV turning on of the main switch is achieved by discharging $C_{DS}$ completely. The $L$ required to achieve the ZV turning on of the switch decreases as $f_S$ increases; as a consequence, the switching loss in the auxiliary switch increases. Therefore, simultaneous reduction of switching losses in the main and auxiliary switches is very difficult at high $f_S$. The converter of Reference [9] uses a passive snubber to reduce the switching loss. The switching loss is reduced by lowering the turn-on slope of the switch current; the inductor $L_S$ that is connected in series with the switch controls the turn-on slope. However, the energy stored in $L_S$ is released as a voltage spike because the current path of $L_S$ is blocked when the switch is turned off. To ensure that this voltage spike does not exceed the maximum voltage limit of the switch, $L_S$ should be less than 50 nH at high switching frequencies; This value of $L_S$ was calculated using Equation (9) of the design guide in Reference [9]. The low value of the chip type inductor has a low maximum current limit. This low inductance also causes undesired resonance due to the parasitic inductance or capacitance of the circuit. Because of this, the converter of Reference [9] is difficult to use at high switching frequencies. Additionally, the switch current significantly increases the conduction loss in $L_S$ because the components of small size have non-negligible series resistance.

To improve upon the aforementioned drawbacks in the existing converters, this paper proposes a miniature DC-DC boost converter for the display panel of a notebook computer. The proposed converter (Figure 2) uses a passive snubber to reduce the switching loss; the capacitor $C_2$ is connected in parallel with the switch, and the inductor $L_1$ is connected in series with $C_2$, and the value of $L_1$ and $C_2$ are large enough to prevent resonance at high $f_S$. This lowers $V_{SW}$ to $V_O-V_{C1}$ and eliminates the switching loss. In addition, $L_1$ is placed apart from the main current path to reduce the conduction loss in the passive snubber. The switch operates under a hard-switching condition to achieve fast

![Figure 1. Schematic of conventional DC-DC boost converter.](image-url)
switching, but the switching loss is reduced by lowering $V_{SW}$ (Figure 3). The switching loss $P_{SW}$ is calculated using the waveforms of $i_{SW}$ and $V_{SW}$ as:

$$P_{SW} = \frac{1}{T_s} \int_{t_0}^{t_2} V_{SW}(t)i_{SW}(t)dt + \frac{1}{T_s} \int_{t_3}^{t_5} V_{SW}(t)i_{SW}(t)dt$$

Compared with the conventional converter, the proposed converter has a similar current peak, but has $V_{SW}(t_1)$ and $V_{SW}(t_4)$ lowered by ~1/2, so $P_{SW}$ is reduced.

The proposed converter has a higher voltage conversion ratio than the conventional boost converter, and therefore has a wide range of output voltage for a given range of input voltage. Section 2 describes the circuit structure and operating principle of the proposed converter, Section 3 gives the design guidelines, Section IV shows the experimental results, and Section V concludes the paper.

2. Circuit Structure and Operating Principles of the Proposed Converter

The proposed converter consists of two capacitors $C_1$ and $C_2$, two diodes $D_1$ and $D_2$, and an inductor $L_1$, in addition to the conventional boost components $L_b$, $D_O$, $C_O$, and a switch (SW). $C_1$ is located between boost inductor $L_b$ and output diode $D_O$, and acts as a charge pump capacitor to
increase the voltage gain. $L_1$ and $C_2$ reduce the voltage stress of SW by dividing the output voltage $V_O$. $D_1$ and $D_2$ provide a charging or discharging path for $C_2$. 

The operating modes (Figure 4) and key waveforms (Figure 5) of the proposed converter include three sequential modes of operation.

**Mode 1 ($t_0$-$t_1$):** The first operation (Figure 4a) starts at $t = t_0$ by turning ON SW. During this operation, $D_2$ turns ON, and $D_1$ and $D_O$ turn OFF. $v_{lb} = V_{IN}$ and $v_{l1} = V_{C2}-V_{C1}$, so

$$i_{lb}(t) = \frac{V_{IN}}{L_b}(t-t_0) + i_{lb}(t_0)$$

(1)

$$i_{l1}(t) = i_{C1}(t) = \frac{V_{C2}-V_{C1}}{L_1}(t-t_0)$$

(2)

$C_1$ is charged and $C_2$ is discharged when SW is turned ON. Mode 1 ends when SW is turned OFF.

**Mode 2 ($t_1$-$t_2$):** The second operation (Figure 4b) starts at $t = t_1$ when SW turns OFF. During mode 2, $D_2$ stays ON, and $D_1$ and $D_O$ are turned ON. When SW is turned OFF, the anode voltage of $D_1$ is $V_{C2}$ because $V_{lb} = V_{C2} - V_{IN}$ according to the voltage second valence law. The cathode voltage of $D_1$ is $V_{C2} - \Delta V_{C2}$ because $C_2$ was discharged in Mode 1, so $D_1$ is turned ON. After $D_1$ is turned ON, the anode voltage of $D_O$ is $V_{C1} + V_{C2}$ and cathode voltage is $V_O - \Delta V_O$ because $C_O$ was discharged in Mode 1. Therefore, $D_O$ is turned ON because $V_{C1} + V_{C2} = V_O$ in steady state. In the same manner, after $D_1$ and $D_O$ are turned ON, $D_2$ is turned ON because the anode voltage of $D_2$ is $V_{C1} + V_{C2}$ and the cathode voltage is $V_O - \Delta V_O$. $v_{lb} = V_{IN} - V_{C2}$ and $v_{l1} = -V_{C1}$, so

$$i_{lb}(t) = \frac{V_{IN} - V_{C2}}{L_b}(t-t_1) + i_{lb}(t_1), \quad i_{l1}(t) = \frac{V_{C1}}{L_1}(t-t_1) + i_{l1}(t_1).$$

Figure 4. Modes of operation: (a) Mode 1 ($t_0 < t < t_1$), (b) Mode 2 ($t_1 < t < t_2$), (c) Mode 3 ($t_2 < t < t_3$).
The voltage stress of SW is $V_{C2}$ because $D_1$ is turned ON when SW is turned OFF. The output voltage $V_O$ is divided into $V_{C1}$ and $V_{C2}$, so the voltage stress of SW is smaller than $V_O$, which is the voltage stress of the conventional boost converter.

Mode 3 ($t_2$~$t_3$): The last operation (Figure 4c) starts at $t = t_2$ when $D_2$ turns OFF. $D_1$ and $D_O$ stay ON during this mode.

$$v_{Lb} = V_{IN} - V_{C2}, \quad \text{so} \quad i_{Lb}(t) = \frac{V_{IN} - V_{C2}}{L_b}(t - t_1) + i_{Lb}(t_1)$$

In this mode, $v_{L1} = 0$ because $i_{L1} = 0$. Mode 3 ends when SW is turned ON for the next switching cycle.

The voltage-second balance law of inductances $L_b$ and $L_1$ yields

$$V_{IN}D + (V_{IN} - V_{C2})(1 - D) = 0 \quad \quad \quad (3)$$

$$V_{C2} - V_{C1}D - V_{C1}(1 - D - \alpha) = 0 \quad \quad \quad (4)$$

where $D$ is the duty of switching and $\alpha T_S$ is the duration of Mode 3. Solving Equations (3) and (4) for $V_{C1}$ and $V_{C2}$ yields

$$V_{C2} = \frac{V_{IN}}{1 - D}, \quad V_{C1} = \frac{D}{1 - \alpha} \frac{V_{IN}}{1 - D}. \quad \quad \quad (5)$$
Equation (5) and $V_O = V_{C1} + V_{C2}$ then give the voltage conversion ratio as

$$\frac{V_O}{V_{IN}} = \frac{1}{1-D} \frac{1 - \alpha + D}{1 - \alpha} \quad (6)$$

The average current of $L_1$, $I_{L1}$ for one switching period $T_S$ is equal to the average output current $I_O$, so

$$I_O = \frac{V_{C2} - V_{C1}}{2L_1} D^2 T_S + \frac{V_{C1}}{2L_1} (1 - D - \alpha)^2 T_S \quad (7)$$

Inserting Equation (5) into Equation (7) and solving for $\alpha$ yields

$$\alpha = \frac{(V_{IN}DT_S - 2I_O L_1)(1 - D)}{V_{IN} DT_S} \quad (8)$$

Combining Equations (6) and (8) yields the output voltage

$$V_O = \frac{2V_{IN}(V_{IN}D^2 T_S + I_O L_1 (1 - D))}{(1 - D)(V_{IN}D^2 T_S + 2I_O L_1 (1 - D))} \quad (9)$$

$V_O$ versus $D$ (Figure 6) for $L_1 = 10 \ \mu H$, $f_s = 1 \ \text{MHz}$, $I_O = 150 \ \text{mA}$, $V_{IN} = 5 \ \text{V}$, and $0.1 \leq D \leq 0.9$ was calculated using Equation (9) for the proposed converter, but the conventional boost converter was calculated using their voltage gain equations. To have $V_O = 40 \ \text{V}$ for given $V_{IN}$, $D = 0.775$ was applied to the proposed converter, whereas $D = 0.875$ was applied to the conventional boost converter. At given $V_{IN}$ and $D$, the proposed converter had higher $V_O$ than the conventional boost converters.

![Figure 6. $V_O$ versus duty $D$ for the experimental boost converters; $V_{IN} = 5 \ \text{V}$, $0.1 \leq D \leq 0.9$.](image)

3. Design Guideline

3.1. Boost Inductor $L_b$

The inductance $L_b$ of $L_b$ should be determined so that the proposed converter operates in a continuous conduction mode (CCM). The current through $L_b$ is minimum at $t_0$ and maximum at $t_1$. The following equation is obtained using the average of $i_{Lb}$ and Equation (1),

$$i_{Lb}(t_1) - i_{Lb}(t_0) = \frac{V_{IN} DT_S}{L_b}, \quad i_{Lb}(t_1) + i_{Lb}(t_0) = 2I_{IN}. \quad (10)$$

Solving Equation (10) for $i_{Lb}(t_0)$ yields

$$i_{Lb}(t_0) = I_{IN} - \frac{V_{IN} DT_S}{2L_b}$$
The condition \( i_{D2}(t_0) > 0 \) should be satisfied to operate the proposed converter in CCM. This condition yields

\[
L_b > \frac{V_{IN}DT_S}{2I_{IN}} \tag{11}
\]

For \( 5 \leq V_{IN} \leq 17.5 \) V, \( V_O = 40 \) V, \( f_S = 1 \) MHz, and \( 30 \leq I_O \leq 150 \) mA, \( L_b = 33 \) \( \mu \)H was determined using Equations (9) and (11).

3.2. Snubber Inductor \( L_1 \)

A small value of \( L_1 \) causes a drastic current decrease of \( D_2 \) in mode 2. Therefore, the limit of \( L_1 \) is calculated using the following condition for a soft turn-off of \( D_2 \).

\[
\frac{V_{C1}}{L_1} \ll \frac{I_{D2,max}}{t_{D2,fall}}
\]

where \( I_{D2,max} \) is the highest diode current and \( t_{fall} \) is the diode turn-off time; \( L_1 \gg 0.2 \) \( \mu \)H for \( I_{D2,max} = 1 \) A and \( t_{fall} = 10 \) ns. The diode turn-off loss increases as \( L_1 \) decreases, so \( L_1 = 10 \) \( \mu \)H was chosen to provide an operating margin and to reduce turn-off loss of \( D_2 \).

3.3. Snubber Capacitors \( C_1 \) and \( C_2 \)

The capacitance of \( C_1 \) is determined by the condition that \( \Delta V_{C1} \ll V_{C1} \) because \( V_{C1} \) should be almost constant for one switching period \( T_S \), where \( \Delta V_{C1} \) is the voltage ripple of \( C_1 \). During Mode 1, \( C_1 \) charges through \( L_1 \); this results in a voltage ripple \( \Delta V_{C1} \) of \( C_1 \); \( \Delta V_{C1} = (V_{C2} - V_{C1}) (DT_S)^2 / (2C_1L_1) \) because the current through \( C_1 \) decreases linearly from 0 A at \( t_0 \) to \( (V_{C2} - V_{C1})DT_S / L_1 \) at \( t_1 \).

Therefore,

\[
C_1 \gg \frac{V_{C2} - V_{C1}}{2V_{C1}L_1} (DT_S)^2. \tag{12}
\]

For \( V_{IN} = 5 \) V, \( V_O = 40 \) V, \( f_S = 1 \) MHz, and \( L_1 = 10 \) \( \mu \)H, \( C_1 = 1 \) \( \mu \)F was determined using Equations (5) and (12). \( C_2 \) has been chosen to be the same as \( C_1 \) because \( \Delta V_{C1} = \Delta V_{C2} \) and \( i_{C1} = -i_{C2} \) in Mode 1.

4. Experimental Results

The proposed boost converter (Figure 7) was designed to operate at \( V_{IN} = 5 \) V, \( V_O = 40 \) V, \( 30 \leq I_O \leq 150 \) mA, and \( f_S = 1 \) MHz. The inductances were set at \( L_b = 33 \) \( \mu \)H and \( L_1 = 10 \) \( \mu \)H. Capacitances \( C_1 \) and \( C_2 \) were both set at 1 \( \mu \)F. The experimental circuit was implemented using the following miniature components (Table 1): TPS55340 DC-DC controller (Texas Instruments Inc., Dallas, TX, USA), which has an internal \( n \)-MOS switch (40 V, 5A), RB160M-60TR diodes (Rohm Co.), IFSC-1515AH-01 (Vishay Inc.) and SSMC25008R47SC (SST Inc.) chip inductors, and multilayer ceramic chip capacitors of a size 3.2 mm \times 1.6 mm. The chip inductors and capacitors have series resistances given in the parentheses. To ensure a fair comparison, the conventional boost converter used the same components.

![Figure 7. Photograph of the proposed DC-DC boost converter.](image_url)
The TPS55340 regulates the output voltage with current mode PWM control, and has an internal oscillator. The pulse width modulation of the gate pulse $V_g$ is achieved in the control circuit for the proposed converter (Figure 8) as follows; each clock pulse resets the flip-flop and the ramp generator, which sets $V_g$ to the ‘high’ state; the output $V_c$ of the error amplifier increases as $V_O$ increases; the comparator output changes from ‘low’ to ‘high’ when the output voltage of the ramp generator exceeds $V_c$, which changes the inverter output $V_g$ to the ‘low’ state. When the output current $I_O$ increases/decreases abruptly, $V_O$ decreases/increases instantly, which increases/decreases $V_c$. Thus, the pulse width of $V_g$ increases/decreases to keep $V_O$ constant.

The voltage and current waveforms of SW (Figure 9) were measured at $V_{IN} = 5$ V, $V_O = 40$ V, $I_O = 150$ mA, and $f_S = 1$ MHz. The voltage stress of the proposed converter (Figure 9a) was lower than that of the conventional boost converter (Figure 9b) because the voltage stress was $V_O - V_C1$ in the proposed converter but $V_O$ in the conventional boost converter. The current stresses of the proposed converter and the conventional boost converter were similar. The current waveforms of the diodes are shown in Figure 10. The diodes current stresses of the proposed converter was lower than the conventional boost converter. The time-averaged values $<i_{D1}>, <i_{D2}>, and <i_{D0}> were all equal to $I_O$.

The curves of $\eta_e$ on $I_O$ (Figure 11a) were measured at $30 \leq I_O \leq 150$ mA, $V_{IN} = 5$ V, $V_O = 40$ V, $f_S = 1$ MHz. At $I_O = 30$ mA, $\eta_e$ was 84.0% for the proposed converter and 76.9% for the conventional boost converter. At $I_O = 150$ mA, $\eta_e$ was 80.4% for the proposed converter and 72.6% for the conventional boost converter. The curves of $\eta_e$ on $V_{IN}$ (Figure 11b) were measured at $5 \leq V_{IN} \leq 17.5$ V, $I_O = 150$ mA, $V_O = 40$ V, $f_S = 1$ MHz; $\eta_e$ at $V_{IN} = 17.5$ V was 89.1% for the proposed converter and 88.6% for the conventional boost converter. The $\eta_e$ of the proposed converter was up to 7.8% higher than the conventional boost converter at $V_{IN} = 5$ V. The proposed converter had a high $\eta_e$ over the entire input voltage and output current ranges.

### Table 1. Component values for the experimental boost converters.

<table>
<thead>
<tr>
<th>Components</th>
<th>Conventional Boost Converter</th>
<th>Proposed Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_b$</td>
<td>33 μH (450 mΩ)</td>
<td>33 μH (450 mΩ)</td>
</tr>
<tr>
<td>$L_1$</td>
<td>-</td>
<td>10 μH (150 mΩ)</td>
</tr>
<tr>
<td>$C_1$</td>
<td>-</td>
<td>1 μH (12.5 mΩ)</td>
</tr>
<tr>
<td>$C_2$</td>
<td>-</td>
<td>1 μH (12.5 mΩ)</td>
</tr>
<tr>
<td>$C_O$</td>
<td>4.7 µF (10 mΩ)</td>
<td>4.7 µF (10 mΩ)</td>
</tr>
<tr>
<td>$D_1$</td>
<td>-</td>
<td>RB160M-60TR</td>
</tr>
<tr>
<td>$D_2$</td>
<td>-</td>
<td>RB160M-60TR</td>
</tr>
<tr>
<td>$D_O$</td>
<td>RB160M-60TR</td>
<td>RB160M-60TR</td>
</tr>
<tr>
<td>Driver IC (SW)</td>
<td>TPS55340 ($R_{on} = 0.1$ Ω)</td>
<td>TPS55340 ($R_{on} = 0.1$ Ω)</td>
</tr>
</tbody>
</table>

Figure 8. Block diagram of the control circuit for the proposed converter.

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Figure 9. Voltage and current waveforms of switch measured at $V_{IN} = 5\, V$, $V_O = 40\, V$, $I_O = 150\, mA$, and $f_S = 1\, MHz$. (a) Proposed converter, (b) conventional boost converter.

Figure 10. Diode waveforms of the proposed converter. (a) $D_o$, (b) $D_1$, (c) $D_2$, and diode waveform of the conventional boost converter. (d) $D_o$ measured at $V_{IN} = 5\, V$, $V_O = 40\, V$, $I_O = 150\, mA$ and $f_S = 1\, MHz$. 
The proposed converter reduced the switching loss by decreasing the current in the snubber circuit. Additionally, the snubber loss of the proposed converter was 0.16 W at $V_{IN} = 5$ V, and it was 0.15 W at $V_{IN} = 15$ V. These data indicate that the proposed converter generated less heat loss than the conventional boost converter.

The temperatures of SW and inductors (Figure 12) were measured for 30 min using a digital temperature recorder (GL-220, GRAPHTEC), while the converters were operated at $V_{IN} = 5$ V, $V_O = 40$ V, $I_O = 150$ mA, $V_{IN} = 5$ V, and $I_O = 150$ mA. In the conventional boost converter the switch stabilized at 86.6 °C and the inductor stabilized at 91.7 °C, but in the proposed converter, the switch stabilized at 49.5 °C and the inductor stabilized at 62.9 °C. These data indicate that the proposed converter generated less heat loss than the conventional boost converter.

The circuit losses were calculated using a circuit simulator at $V_{IN} = 5$ V, $V_O = 40$ V, $I_O = 150$ mA, and $f_S = 1$ MHz. The total power losses were 1.59 W (proposed) and 2.31 W (conventional) at $V_{IN} = 5$ V, and they were 0.68 W (proposed) and 0.78 W (conventional) at $V_{IN} = 15$ V. These results show that the proposed converter had lower power loss than the conventional boost converter at both $V_{IN} = 5$ V and 15 V. The losses in the switch were 0.65 W (proposed) and 1.41 W (conventional) at $V_{IN} = 5$ V, and they were 0.38 W (proposed) and 0.63 W (conventional) at $V_{IN} = 15$ V. The proposed converter reduced the switching loss by decreasing $V_{SW}$. Additionally, the snubber loss of the proposed converter was 0.16 W at $V_{IN} = 5$ V, and it was 0.15 W at $V_{IN} = 15$ V. The proposed converter reduced the snubber losses by placing $L_1$ at the output stage and eliminating the resonant current in the snubber circuit.
The voltage and current stress (Table 2) of the proposed and conventional boost converter were measured at $V_{IN} = 5$ V, $V_O = 40$ V, $I_O = 150$ mA, and $f_S = 1$ MHz. Without parasitic components, the voltage stress of SW and diodes were as follows: (1) in the conventional boost converter, $V_{SW} = V_O$ because $D_O$ was turned ON when $SW$ was turned OFF, and $V_{D0} = V_O$ because SW was turned ON when $D_O$ was turned OFF; (2) in the proposed converter, $V_{SW} = V_O - V_{C1}$ because $D_O$, $D_1$, and $D_2$ were turned ON when SW was turned OFF, $V_{D0} = V_{D1} = V_O - V_{C1}$ because SW was turned ON when $D_O$ and $D_1$ are turned OFF, and $V_{D2} = V_O - V_{C2}$ because $D_1$ and $D_0$ were turned ON, and SW was turned OFF when $D_2$ was turned OFF. The proposed converter had lower voltage stress of SW and diodes than the conventional boost converter because $V_O = V_{C1} + V_{C2}$. The current stress of SW was similar in the conventional boost converter and the proposed converter. The current stresses of diodes were lower by half in the proposed converter than in the conventional boost converter.

**Table 2. Voltage and current stresses of components in the experimental boost converters.**

<table>
<thead>
<tr>
<th>Components</th>
<th>Conventional Boost Converter</th>
<th>Proposed Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Peak voltage stress (V)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW</td>
<td>45.1</td>
<td>24.9</td>
</tr>
<tr>
<td>$D_O$</td>
<td>53.5</td>
<td>27.7</td>
</tr>
<tr>
<td>$D_1$</td>
<td>-</td>
<td>27.3</td>
</tr>
<tr>
<td>$D_2$</td>
<td>-</td>
<td>26.0</td>
</tr>
<tr>
<td><strong>Peak voltage stress (A)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW</td>
<td>1.72</td>
<td>1.87</td>
</tr>
<tr>
<td>$D_O$</td>
<td>1.78</td>
<td>0.90</td>
</tr>
<tr>
<td>$D_1$</td>
<td>-</td>
<td>0.96</td>
</tr>
<tr>
<td>$D_2$</td>
<td>-</td>
<td>0.32</td>
</tr>
</tbody>
</table>

The voltage stress, current stress, voltage gain, and efficiency of the existing boost converter were calculated using a circuit simulator at $V_{IN} = 5$ V, $V_O = 40$ V, $I_O = 150$ mA, and $f_s = 1$ MHz (Table 3). The efficiency $\eta_e$ was 72.6% for the conventional boost converter, 80.4% for the proposed converter, 75.1% for the converter of Reference [12], and 76.6% for the converter of Reference [21]. The proposed converter had the highest $\eta_e$ for given input and output conditions. The converters of References [12,21] had a lower efficiency than that of the proposed converter due to a high current stress and the loss of auxiliary switch, respectively. The voltage stress of the proposed converter was lower than that of the other converters because the voltage stress is $V_O-V_{C1}$ in the proposed converter but $V_O$ in the other converters. The current stresses of the proposed converter and the conventional boost converter were similar, but the converter of Reference [12] had a high current stress because it used resonance to
reduce the switching loss at high frequency. At given $V_{IN}$ and $V_{O}$, the proposed converter had the smallest duty, so the proposed converter had the highest voltage gain.

### Table 3. Comparison with existing boost converters.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of Components</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Inductor</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Capacitor</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Diode</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td><strong>Switch Stress</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage stress (V)</td>
<td>45.1</td>
<td>24.9</td>
<td>45.2</td>
<td>SW$_1$ 42.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SW$_2$ 42.8</td>
</tr>
<tr>
<td>Current stress (A)</td>
<td>1.72</td>
<td>1.87</td>
<td>2.92</td>
<td>SW$_1$ 2.42</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SW$_2$ 2.64</td>
</tr>
<tr>
<td>Duty</td>
<td>0.875</td>
<td>0.775</td>
<td>0.831</td>
<td>0.82 (main SW)</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>72.6</td>
<td>80.4</td>
<td>75.1</td>
<td>76.6</td>
</tr>
</tbody>
</table>

### 5. Conclusions

A miniature DC-DC boost converter for driving a display panel of a notebook computer was proposed. This converter operates at a switching frequency of 1 MHz to miniaturize the circuit. The switching loss is reduced by using a passive snubber that lowers the voltage stresses of the switch. The conduction losses of the snubber and switch is also minimized by preventing high peak current due to the resonance at high $f_S$. The experimental converter was fabricated in 2.5 cm × 1 cm size and tested at $5 \leq V_{IN} \leq 17.5$ V, $30 \leq I_O \leq 150$ mA. Compared to previous boost converters, the proposed converter had a higher voltage conversion ratio, ~7.8% higher power conversion efficiency over the entire range of $V_{IN}$ and $I_O$, ~1/2 as much voltage stress of the switch and diodes, and a much lower switch temperature. The results indicate that the proposed converter is a strong candidate for driving the display panel of a notebook computer.

**Author Contributions:** S.-H.H. conceived the main idea for the proposed converter and performed overall analysis and experiment. H.-J.C. led the project and gave technical advice.

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**Conflicts of Interest:** The authors have no conflict of interest.

**References**


