Analysis and Design of High-Efficiency Bidirectional GaN-Based CLLC Resonant Converter

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Abstract: A bidirectional CLLC resonant converter (CLLC-BRC) based on GaN transistors is analyzed and designed in this paper. Similar resonant topologies are listed and commented on, with the CLLC topology showing competitiveness in bidirectional energy transmission. The analysis of the aforementioned converter has been provided, including the reveal of resonant frequencies of the CLLC topology and an improved zero-voltage switching (ZVS) condition with operation principles of the reverse mode and relevant parasitic parameters taken into account. The design methodology of the aforementioned converter based on pulse frequency modulation (PFM) is further discussed in detail. A prototype with a rated power of 400 W and a maximal operating frequency that is larger than 0.5 MHz was built to verify the proposed design methodology. The highest conversion efficiency of the prototype was 97.02% in the forward mode, and it was 95.96% in the reverse mode.

Keywords: GaN transistors; bidirectional CLLC resonant converter; high efficiency

1. Introduction

Bidirectional DC/DC converters (BDCs) play an important role in many fields, including new energy generation systems, electric vehicles, aerospace power supplies and uninterruptible power supplies. An isolated type of BDC is usually accepted instead of a non-isolated one, as shown in Figure 1, since the aforementioned fields have strict requirements for safety.

![Figure 1. Structure of isolated BDC.](image)

Many isolated BDCs focus on soft switching to reduce loss due to its high operating frequency aiming for high power density, which are mainly divided into the phase shift control type [1,2] and the resonant type [3,4]. The gain range of the phase shift control type is limited, and soft switching of the full load range is hard achieve. By contrast, the LLC resonant converter is a topology of three resonant components that can achieve zero-voltage switching (ZVS) in the inverter-side of the full...
load range without any auxiliary circuits. In order to achieve bidirectional energy transmission, the diodes of its rectifier bridge are replaced with fully controlled devices. In [5], all the topologies of three resonant components are listed, including Type-4 and Type-11, as shown in Figure 2a,b. However, similar bidirectional voltage gain characteristics cannot be obtained in the two types. For example, when the LLC resonant circuit operates in the reverse mode, it degenerates into a LC resonant circuit, with normalized dc gain below 1. In [6–12], a symmetric tank structure called CLLLC is proposed, as shown in Figure 2c. Although similar bidirectional voltage gain features are obtained, too many resonant components are used in CLLLC, which increases the volume of the converter and the error of analysis and design. What’s more, the procedures of designing parameters [6] and controllers [7] are complicated, with the potential for risky operations caused by parasitic capacitance [12], leading to deviations from the design intention. In [13,14], a resonant tank of four elements called CLLC is proposed, as shown in Figure 2d. In contrast to the CLLLC topology, one resonant inductor is omitted in the CLLC topology, and similar bidirectional voltage gain features are obtained. The CLLC-BRC can achieve ZVS in the inverter side of the full-load range, and zero-current switching (ZCS) in the rectifier side of a certain load range. Additionally, the range of bidirectional DC gains is expanded, leading to more flexible capacity of voltage regulation. In [14], the forward mode and the reverse mode are equivalent to Type-4 and Type-11 with additional capacitors respectively. However, different basic frequencies are used for the two modes, with some features in common ignored. The current research on CLLC-BRC still needs to be improved, such as calculation of resonant frequencies of the CLLC topology, more thorough soft switching condition and so on.

Moreover, with the continuous development of semiconductor technology, the third generation of wide-bandgap semiconductor devices, including gallium nitride (GaN) devices and silicon carbide (SiC) devices, have been developed to help BDCs achieve higher frequency, higher power density, and higher efficiency, replacing conventional devices like Si MOSFETs. A summary of the material characteristics of these devices is shown in [9]. GaN has higher energy gap and electron velocity in contrast to SiC and Si, and thus GaN transistors possess better performance of lower on-resistance, faster switching speed, lower parasitic parameters, lower reverse recovery loss and so on. GaN transistors are suitable for even MHz-level operating frequency occasions that are difficult for application of SiC devices with high efficiency. It is well expected that GaN transistors deserve to replace other devices in low or medium power occasions. However, GaN transistors have a lower driving voltage threshold than SiC devices and thus have a high requirement for designing driving circuits to prevent wrong conduction. Meanwhile, GaN transistors have a larger reverse conduction voltage drop than SiC devices when no driving voltage is supplied, and thus synchronous rectification (SR) must be applied in the rectifier-side of BDC, whose accuracy affects the quality of output voltage and efficiency. Due to these problems, it is meaningful to study the application of GaN transistors in different BDC topologies that have already been equipped with MOSFETs. In [15–20], GaN transistors are applied to the conventional LLC resonant converter. However, it is hard to meet the bidirectional application requirement with the limitation of the LLC topology in the reverse mode. In [9], GaN transistors were applied to the bidirectional CLLLC resonant converter with parameters based on the design methodology proposed.

![Figure 2. Structures of resonant tanks of different types. (a) Type-4, i.e., LLC; (b) Type-11; (c) CLLLC; (d) CLLC.](image-url)
in [6]. However, complicated principles and the high design requirements of the CLLLC converter disturb the successful application of GaN transistors. Current solutions of replacing all conventional switching devices with GaN transistors in BDCs are still unsatisfying.

Therefore, this paper focuses on CLLC-BRCs of high operating frequency and high efficiency based on GaN transistors. In Section 2, the characteristics of CLLC-BRC are discussed in detail based on its operation principles, including the solution of resonant frequencies, definitions of auxiliary parameters and an improved ZVS condition of the inverter-side switches. In Section 3, the design procedures of GaN-based CLLC-BRC based on PFM are presented with assistance of the previous analysis. Then, the structure of the prototype and experimental results are shown in Section 4. Finally, conclusions are made in Section 5.

2. Analysis of Bidirectional CLLC Resonant Converter

The structure of GaN-based CLLC-BRC is shown in Figure 3. In [14], the operation principles of both the forward mode (MT-4 mode) and the reverse mode (MT-11 mode) of CLLC-BRC have been illustrated in detail, which thus will not be restated in this paper. However, different reference frequencies were used in the normalized dc gain curves of the two modes in [14], which conceals some critical features of CLLC topology, like the same resonant frequencies possessed by the two modes. Based on the first harmonic approximation (FHA) method, the following analysis is given.

2.1. Resonant Frequencies of Bidirectional CLLC Resonant Converter

The equivalent circuit of the forward mode is shown in Figure 4a, where $C_{r2e} = \frac{C_2}{n^2}$ is the normalized capacitor of $C_r2$, and $R_{ef} = \frac{8}{\pi^2}n^2R_{1,1}$ is the normalized equivalent AC resistance of the forward-mode load $R_{1,1}$. It can be further converted into the topology in Figure 4b based on Thevenin’s theorem, where the equivalent tank voltage $V_{1\text{tank}}$ and the total tank impedance $Z_{1\text{tank}}$ can be derived as:

$$V_{1\text{tank}} = V_1 \frac{\omega_s L_m}{\omega_s L_m + \omega_s L_r - \frac{1}{\omega_s C_{r1}}}$$

$$Z_{1\text{tank}} = \frac{1}{j \omega_s C_{r2e}} + j \omega_s L_m \left( j \omega_s L_r + \frac{1}{j \omega_s C_{r1}} \right) = \frac{L_m L_r C_{r1} C_{r2e} \omega_s^4 - (L_m C_{r1} + L_m C_{r2e} + L_r C_{r1}) \omega_s^2 + 1}{\omega_s^2 C_{r1} C_{r2e} (\omega_s L_m + \omega_s L_r - \frac{1}{\omega_s C_{r1}})}$$

where $\omega_s = 2\pi f_s$ and $f_s$ is the operating frequency of CLLC-BRC.
2.2. Auxiliary Parameters

Figure 4. Equivalent circuits of the forward mode and the reverse mode. (a) FHA circuit of the forward mode; (b) Thevenin equivalent circuit of (a); (c) FHA circuit of the reverse mode; (d) Thevenin equivalent circuit of (c).

The total impedance is in the state of pure resistance when the CLLC-BRC operates at the resonant frequencies. That is to say, $Z_{tank} = 0$, i.e.:

$$L_m L_r C_{r1} C_{r2e} \omega_2^4 - (L_m C_{r1} + L_m C_{r2e} + L_r C_{r1}) \omega_2^2 + 1 = 0$$

(3)

Apparently, there exist two resonant frequencies in the forward mode, which can be defined as $f_{r1}$ and $f_{r2}$ ($f_{r1} < f_{r2}$). Meanwhile, the equivalent circuits of the reverse mode of CLLC-BRC are shown in Figure 4c,d, where $R_{er} = \frac{R_{L2}}{\pi}$ is the equivalent ac resistance of the reverse-mode load $R_{L2}$. Similarly, $V_{2tank}$ and $Z_{2tank}$ can be derived as:

$$V_{2tank} = n V_2 \frac{\omega s L_m}{\omega s L_m - \frac{1}{\omega s C_{r2e}}}$$

(4)

$$Z_{2tank} = \frac{L_m L_r C_{r1} C_{r2e} \omega_2^4 - (L_m C_{r1} + L_m C_{r2e} + L_r C_{r1}) \omega_2^2 + 1}{\omega_2^2 C_{r1} C_{r2e} \left( \omega_s L_m - \frac{1}{\omega_s C_{r2e}} \right)}$$

(5)

When the CLLC-BRC operates at the resonant frequencies, the same reason leads to $Z_{2tank} = 0$, i.e., condition (3). That is to say, the same resonant frequencies are possessed by both the forward mode and the reverse mode.

Defining $a = L_m L_r C_{r1} C_{r2e}$, $b = -(L_m C_{r1} + L_m C_{r2e} + L_r C_{r1})$ and $c = 1$, with permanent $b^2 - 4ac > 0$, resonant frequencies of the two modes, i.e., $f_{r1}$ and $f_{r2}$, can be derived from Equation (3) as:

$$f_{r1} = \sqrt{\frac{\omega_2^2}{2\pi}} = \sqrt{-\frac{b - \sqrt{b^2 - 4ac}}{2a}} / 2\pi, \quad f_{r2} = \sqrt{-\frac{b + \sqrt{b^2 - 4ac}}{2a}} / 2\pi$$

(6)

2.2. Auxiliary Parameters

To simplify the analysis, some critical auxiliary parameters deserve to be defined, with their expressions and meanings shown in Table 1.
Table 1. Auxiliary parameters’ definitions.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Expression</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1; Q_2$</td>
<td>$\sqrt{L_{r1}/C_{r1}}; \sqrt{L_{r2}/C_{r2}}$</td>
<td>Quality factor of the forward mode and the reverse mode, respectively</td>
</tr>
<tr>
<td>$C_n$</td>
<td>$\frac{C_{r2}}{L_{n}}$</td>
<td>Ratio of resonant capacitors</td>
</tr>
<tr>
<td>$L_n$</td>
<td>$\frac{L_{r1}}{L_{n}}$</td>
<td>Ratio of resonant inductors</td>
</tr>
<tr>
<td>$f_n$</td>
<td>$\frac{1}{2\pi \sqrt{L_{r1}C_{r1}}}$</td>
<td>Basic frequency</td>
</tr>
<tr>
<td>$f$</td>
<td>$\frac{1}{L_{n}}$</td>
<td>Normalized operating frequency</td>
</tr>
<tr>
<td>$f_{m1}; f_{m2}$</td>
<td>$\frac{1}{2\pi \sqrt{(L_{n}+L_{m})C_{r2}}}; \frac{1}{2\pi \sqrt{L_{n}C_{r2}}}$</td>
<td>Series inverter-side resonant frequencies of the forward mode and the reverse mode, respectively</td>
</tr>
</tbody>
</table>

Therefore, based on the FHA method, normalized dc gain $G_f$ of the forward mode and $G_r$ of the reverse mode can be expressed respectively as:

$$|G_f| = \left| \frac{nV_2}{V_1} \right| = \left| \frac{\sqrt{q^2-4p} + j\sqrt{q^2-4p}}{C_n L_{n} f_{m1}^2} \right|^\frac{1}{2} \left( Q_1 \left[ \frac{C_n L_{n} f_{m1}^2 - (C_n L_{n} + L_{m} + 1)^2 + 1}{C_n L_{n} f_{m1}^2} \right] \right)$$  \hspace{1cm} (7)

$$|G_r| = \left| \frac{V_1}{nV_2} \right| = \left| \frac{\sqrt{q^2-4p} + j\sqrt{q^2-4p}}{C_n L_{n} f_{m1}^2} \right|^\frac{1}{2} \left( Q_2 \left[ \frac{C_n L_{n} f_{m1}^2 - (C_n L_{n} + L_{m} + 1)^2 + 1}{C_n L_{n} f_{m1}^2} \right] \right)$$  \hspace{1cm} (8)

Meanwhile, Equation (3) can be simplified based on Table 1 as:

$$C_n L_{n} f_{m1}^4 - (C_n L_{n} + L_{m} + 1)^2 + 1 = 0$$  \hspace{1cm} (9)

Defining $p = C_n L_{n}$, $q = -(C_n L_{n} + L_{m} + 1)^2$, the normalized resonant frequencies $f_1$ and $f_2$ can be expressed as:

$$f_1 = \sqrt{-q - \sqrt{q^2 - 4p}} \quad 2p$$
$$f_2 = \sqrt{-q + \sqrt{q^2 - 4p}} \quad 2p$$  \hspace{1cm} (10)

With the help of auxiliary parameters, more simplified analysis results were obtained. In addition, normalized DC gain is only decided by $Q_1$, $Q_2$, $C_n$, $L_n$ and $f$, which will be discussed in the following design methodology in detail.

2.3. Improved Zero-Voltage Switching Condition for Bidirectional CLLC Resonant Converter

In order to realize ZVS of the inverter-side switches, their parasitic capacitors should be completely charged and discharged within the dead time. In contrast to ZVS conditions in [6,14], an improved condition of ZVS with relevant parasitic parameters and dead-time processes of both the forward mode and the reverse mode taken into account is provided in this paper. Based on the operation principles of CLLC-BRC, the following assumptions were made:

1. The operating frequency $f_s$ is very close to the resonant frequency $f_{r2}$ aiming for optimal operation, with continuous current in the inverter side;
2. The process of charging and discharging parasitic capacitance is extremely short with constant inverter-side current taken into account.

Figure 5a shows the critical waveforms about charging and discharging parasitic capacitance in the forward mode. Based on the FHA method, the initial inverter-side current in the dead time of the forward mode, i.e., the constant current in the dead time, can be expressed as:

$$I_{\text{dead}_f} = \frac{1}{2} \int_{0}^{t_f} n \frac{V_2 - uC_{r2}}{L_{m}} \, dt, \quad uC_{r2} = U_{C_{r2}} \cos(2\pi f_s t + \phi)$$  \hspace{1cm} (11)
where $U_{C_{r_2}}$ is the peak voltage on $C_{r_2}$.

As for the rectifier-side current $i_{C_{r_2}}$, it is clear that:

$$i_{C_{r_2}} = C_{r_2} \frac{dU_{C_{r_2}}}{dt}, \quad i_{C_{r_2}}(0) = 0$$  \hspace{1cm} (12)

Therefore, $I_{\text{dead,f}}$ can be estimated from (11~12) as:

$$I_{\text{dead,f}} = \frac{nV_2 t_1}{2L_m} \approx \frac{nV_2}{4f_s L_m}$$  \hspace{1cm} (13)

Figure 5c shows the equivalent circuit of charging and discharging parasitic capacitance in the forward mode, where $C_1 = C_2 = C_3 = C_4 = C_{\text{oss}1}$, that is the parasitic capacitance of the high-voltage side switches, and $C_5 = C_6 = C_7 = C_8 = C_{\text{oss}2}$, with $C_{\text{oss}2}$ that is the parasitic capacitance of the low-voltage side switches, and $C_T$ is the equivalent parasitic capacitance of the transformer. In order to guarantee ZVS, it is required that:

$$\frac{I_{\text{dead,f}} t_{\text{dead}}}{C_{\text{eff}}} > \Delta u_{AB} = 2V_1$$  \hspace{1cm} (14)

where $C_{\text{eff}} = C_{\text{oss}1} + C_T + C_{\text{oss}2}/n^2$ is the equivalent capacitance of the inverter-side in the forward mode.

![Analysis diagram of ZVS](image)

**Figure 5.** Analysis diagram of ZVS. (a) Critical waveforms of the forward mode; (b) critical waveforms of the reverse mode. (c) Charging and discharging circuit of the forward mode; (d) charging and discharging circuit of the reverse mode.

Similar analysis was done for the reverse mode. Figure 5b shows the critical waveforms about charging and discharging parasitic capacitance in the reverse mode. The constant inverter-side current in the dead time of the reverse mode can be expressed as:

$$I_{\text{dead,r}} = \frac{1}{2} \int_{0}^{t_1} \frac{V_1 - u_{C_{r_1}} - u_{L_r}}{L_m} dt, \quad u_{C_{r_1}} = U_{C_{r_1}} \cos(2\pi f_s t + \phi)$$  \hspace{1cm} (15)
where $U_{Cr1}$ is the peak voltage on $C_{r1}$.

As for the rectifier-side current $i_{Lr}$, it is clear that:

$$i_{Lr} = C_{r1} \frac{du_{Cr1}}{dt}, \quad u_{Lr} = L_{r} \frac{di_{Lr}}{dt}, \quad i_{Lr}(0) = 0$$

(16)

Therefore, $I_{\text{dead}_r}$ can be estimated from Equations (15) and (16) as:

$$I_{\text{dead}_r} = \frac{V_{1}t_{1}}{2L_{m}} \approx \frac{V_{1}}{4f_{s}L_{m}}$$

(17)

Figure 5d shows the equivalent circuit of charging and discharging parasitic capacitance in the reverse mode. In order to guarantee ZVS, it is required that:

$$\frac{I_{\text{dead}_r}t_{\text{dead}}}{C_{\text{eff}2}} > \Delta u_{CD} = 2nV_{2}$$

(18)

where $C_{\text{eff}2} = C_{\text{eff}}$ is the equivalent capacitance of the inverter-side in the reverse mode.

Therefore, the final ZVS condition of CLLC-BRC can be expressed as:

$$L_{m} < \min \left\{ \frac{nV_{2}I_{\text{dead}}}{8f_{s}V_{1}C_{\text{eff}}}, \frac{V_{1}I_{\text{dead}}}{8f_{s}nV_{2}C_{\text{eff}}} \right\}$$

(19)

Based on the requirements of Equation (19), $L_{m}$ should be set as large as possible, so as to reduce the peak of excitation current and dead-time loss. Apparently, lower parasitic capacitance benefits the realization of soft switching, which strengthens the demand for GaN transistors in CLLC-BRCs.

3. Design Methodology of GaN-Based Bidirectional CLLC Resonant Converter

3.1. Design Procedures

We take the procedures of designing the prototype as an example to illustrate the flow chart of designing GaN-based CLLC-BRC, as shown in Figure 6. Design requirements of the prototype are shown in Table 2.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Rated Power</th>
<th>High-Voltage Side/V$_1$</th>
<th>Low-Voltage Side/V$_2$</th>
<th>Output</th>
<th>Ripple</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward</td>
<td>400 W</td>
<td>[382 V, 408 V] V$_{1N}$ = 400 V</td>
<td>[48 V, 56 V] V$_{2N}$ = 50 V</td>
<td>$I_2 = 8$ A</td>
<td>$\Delta V_2 \leq 1%$</td>
</tr>
<tr>
<td>Reverse</td>
<td>400 W</td>
<td>$V_{1N} = 400$ V</td>
<td>[48 V, 56 V] V$_{2N}$ = 50 V</td>
<td>$V_1 = 400$ V</td>
<td>$\Delta V_1 \leq 1%$</td>
</tr>
</tbody>
</table>

The proposed design methodology was based on PFM control method for CLLC-BRC. The initial transformer ratio $n$ could be set as $V_{1N}/V_{2N}$, and then normalized DC gain ranges $[G_{f\text{min}}, G_{f\text{max}}]$ of the forward mode and $[G_{r\text{min}}, G_{r\text{max}}]$ of the reverse mode were obtained with ripples and voltage drop on GaN transistors taken into account. Then, we preset a minimal normalized operating frequency $f_{\text{min}}$.

Figure 7 shows the relation between normalized DC gain and normalized operating frequency $f$ (Table 1) in the bidirectional modes under parameter sweep of quality factor with $L_{n} = 2.6$ and $C_{n} = 1.5$. Apparently, the rise in quality factor leads to a drop in the whole level of dc gain, and the whole level of $G_{r}$ was higher than that of $G_{f}$. Therefore, it is important to guarantee that $G_{f\text{max}}$ is reached when $Q_{1}$ reaches its designed maximum $Q_{1\text{max}}$ and $f = f_{\text{min}}$. Assuming $Q_{1\text{max}} = 0.4$, it is clear that $G_{r\text{max}}$ should be slightly below $G_{r\text{max}}$, otherwise it cannot be reached when $Q_{1} = Q_{1\text{max}}$ and $f = f_{\text{min}}$, which leads to adjusting the ratio $n$ properly.
Obtain DC gain ranges when $Q = Q_{\text{max}}$. Decide $f_{\text{max}}$ to meet the requirement of DC gain range. Calculate $f_{\text{max}}$ and $f_{\text{min}}$, and $f_{\text{2}}-f_{\text{min}}$.

Proper $f_{\text{2}}-f_{\text{min}}$ and $f_{\text{max}}-f_{\text{2}}$?

Set $Q_{\text{max}}$

Yes

Set $L_{\text{n}}$

G_{\text{f} \text{max}} is reached when $Q = Q_{\text{max}}$ and $f = f_{\text{min}}$?

Yes

Preset $f_{\text{max}}$, $C_{\text{n}}$

Design parameters based on the forward mode

Set $Q_{\text{max}}$

No

DC gain range?

Proper operating frequency range?

Meet requirement of the reverse-mode DC gain range?

Verify and correct parameters through the reverse mode

Calculating resonant parameters

Final $L_{\text{n}}, L_{\text{r}}, C_{\text{r}}, C_{\text{2}}$

Check DC gain curves of both the two modes again

Yes

Proper operating frequency range?

No

Meet requirement of the reverse-mode DC gain range?

No

$L_{\text{n}} < L_{\text{m, max}}$

Set standard frequency $f_{\text{n}}$

Calculate $C_{\text{n}}, C_{\text{r, 2}}, L_{\text{r}}, L_{\text{n}}$ by $Q_{\text{max}}, L_{\text{n}}, C_{\text{n}}, f_{\text{n}}$

Set $Q_{\text{max}}$

No

Set $L_{\text{n}}$

Figure 6. Flow chart of designing GaN-based CLLC-BRC.

Figure 7. DC gain curves with parameter sweep of $Q_{1}$ and $Q_{2}$ to illustrate the requirement of $G_{\text{f max}} < G_{\text{r max}}$. (a) Forward mode; (b) reverse mode.

After ratio $n$ and $f_{\text{min}}$ was obtained, we preset a $C_{\text{n}}$. Then, $Q_{\text{1 max}}$ and $L_{\text{n}}$ needed setting. It was better to obtain the curves of relation between $Q_{\text{1 max}}$ and peak normalized DC gain $G_{\text{f peak}}$ of the forward mode with parameter sweep of $L_{\text{n}}$, as shown in Figure 8a. Setting $L_{\text{n}}$ was limited by $G_{\text{f peak}} > G_{\text{f max}}$, which shall be considered when setting $Q_{\text{1 max}}$. A proper $L_{\text{n}}$ can be further decided by Figure 8b after $Q_{\text{1 max}}$ is set. It needed to be guaranteed that the forward-mode dc gain range $[G_{\text{f min}}, G_{\text{f max}}]$ was met within $[f_{\text{min}}, f_{\text{max}}]$, where $f_{\text{max}}$ was the designed maximal normalized operating frequency.
frequency. In other words, $f_{\text{max}}$ was determined by $L_n$ and the requirement of DC gain range. It was well expected that $f_{\text{min}}$ and $f_{\text{max}}$ are not far away from the normalized resonant frequency $f_2$ decided by $L_n$ and $C_n$ to decrease loss. A drop in $L_n$ will lead to a rise in the steepness of the gain curve and thus decrease in $|f_{\text{max}} - f_{\text{min}}|$, but it will also lead to rise in excitation current and dead-time loss. If it is hard to get proper $Q_{1\text{max}}$ and $L_n$, the previous steps need to be redone. It was noted that $C_n$ needed to be further verified and adjusted in combination with the reverse mode due to its effect on $f_{m2}$.

![Figure 7](image-url)  

**Figure 7.** Gain curves used to determine $Q_{1\text{max}}$ and $L_n$. (a) Curve family of DC gain curves with various $Q_{1\text{max}}$ and $L_n$; (b) Curve family of DC gains with various $f$ and $L_n$.

In order to get the actual frequency range, basic frequency $f_n$ needed to be set. According to the ceiling of operating frequency $f_{\text{max}}$, $f_n$ is determined by:

$$f_n = \frac{1}{2\pi \sqrt{L_n C_{r1}}} = \frac{f_{\text{max}}}{f_{\text{max}}}$$

(20)

Therefore, values of $L_m$, $L_r$, $C_{r1}$ and $C_{r2}$ could be derived from $L_m$, $C_{r1}$, $Q_{1\text{max}}$, $f_n$ and relevant expressions. Then, it needed to be verified whether $L_m$ satisfied condition (19), and measure the gain curve of the reverse mode, which can be adjusted according to the above design rules. It should be pointed out that the adjustment of any parameter will affect the forward and reverse DC gains at the same time, and a better design result can only be obtained by continuous adjustment.

### 3.2. Parameters of the Prototype

According to the previous analysis, the ratio of the transformer could be set as $n = 7$, and the parameters of the resonant elements are shown in Table 3, where the voltage and current stress could be obtained by the FHA method. The working-frequency ranges were [298 kHz, 472 kHz] of the forward mode and [271 kHz, 548 kHz] of the reverse mode. The values of resonant frequencies were: $f_{m1} = 131.60$ kHz, $f_{m2} = 164.09$ kHz, $f_{r1} = 106.09$ kHz, and $f_{r2} = 407.08$ kHz.

<table>
<thead>
<tr>
<th>Element</th>
<th>Value</th>
<th>Voltage Stress</th>
<th>Current Stress/RMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{r1}$</td>
<td>8.0 nF</td>
<td>253 V</td>
<td>2.69 A</td>
</tr>
<tr>
<td>$C_{r2}$</td>
<td>812.6 nF</td>
<td>21 V</td>
<td>20.51 A</td>
</tr>
<tr>
<td>$L_r$</td>
<td>29.4 µH</td>
<td>210 V</td>
<td>2.69 A</td>
</tr>
<tr>
<td>$L_m$</td>
<td>88.2 µH</td>
<td>626 V</td>
<td>2.96 A</td>
</tr>
</tbody>
</table>
4. Experimental Verification

The structure of the prototype is shown in Figure 9, with its performance shown in Table 2, and its main components shown in Table 4. It used TI’s UCD138 as a digital controller of the converter on the control board. Compared with the DSP/MCU completely managed by software like TMS320F28335 used in [9], UCD138 has access to high-speed control circuit, multi-loop control and solution of SR, with its three modes switched automatically to meet the requirement of SR in variable frequencies. In the high-voltage side, the isolated driving chip Si8273 was accepted to drive GaN transistors. In the low-voltage side, the non-isolated chip TI’s LMG1205YFXR was used as a driver. The dead time was set as 100 ns based on the used GaN transistors.

One of the biggest obstacles for application of GaN transistors is to design the driving circuit properly, which is discussed in [21] in detail. Meanwhile, it was necessary to implement SR for the rectifier-side GaN transistors due to its comparatively large reverse voltage drop. On-time of rectifier-side GaN transistors can be set as $1/(2f_{r2})$ when the operating frequency $f_s$ is below $f_{r2}$ and as $1/(2f_s)$ when $f_s \geq f_{r2}$, derived from the principles of CLLC-BRC in [14].

The experimental results show that the operating frequency range was [312 kHz, 435 kHz] of the forward mode, and it was [303 kHz, 556 kHz] of the reverse mode. Main waveforms at the maximal and minimal operating frequencies of the two modes are shown in Figures 10 and 11, where $i_{lr}$ is the current of the high-voltage side and $i_{Tr2}$ is the current of the low-voltage side. ZVS of GaN transistors of the whole operating frequency range in the inverter side can be realized in both the two modes. ZCS of GaN transistors in the rectifier side can be realized when $f_s < f_{r2}$, but cannot be realized when $f_s > f_{r2}$, as shown in Figure 10c,d for the forward mode and in Figure 11c,d for the reverse mode. As shown in Figure 12, the converter achieved a maximal efficiency of 97.02% in the forward mode with the output power of 384 W, and achieved a maximal efficiency of 95.96% in the reverse mode with the output power of 408 W. Efficiency of more than 95% was achieved near the rated power of 400 W in the two modes.

![Figure 9. Structure of the prototype.](image-url)

<table>
<thead>
<tr>
<th>Components</th>
<th>Description</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN transistors</td>
<td>GS66502B, in the high-voltage side</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>GS61004B, in the low-voltage side</td>
<td>4</td>
</tr>
<tr>
<td>$C_{r1}$</td>
<td>1 nF, 630 V</td>
<td>8</td>
</tr>
<tr>
<td>$C_{r2}$</td>
<td>47 nF, 100 V</td>
<td>17</td>
</tr>
<tr>
<td>$C_{l1}$</td>
<td>6.8 nF, 100 V</td>
<td>2</td>
</tr>
<tr>
<td>$C_{l2}$</td>
<td>47 uF, 450 V, series</td>
<td>2</td>
</tr>
<tr>
<td>$C_{t2}$</td>
<td>47 uF, 100 V, parallel</td>
<td>3</td>
</tr>
<tr>
<td>HF Transformer</td>
<td>Wound-type; n = 7:1; Primary $L_m$ = 88.2 $\mu$H; Core material: DRM95</td>
<td>1</td>
</tr>
</tbody>
</table>
maximal and minimal operating frequencies of the two modes are shown in Figures 10 and 11, where the forward mode, and it was switching speed, low reverse recovery loss and so on. The application of GaN transistors can further
5. Conclusions
side GaN transistors can be set as \( 1/(2f_{r2}) \) when the operating frequency \( f_s \) is below \( f_{r2} \) and as
rectifier-side GaN transistors due to its comparatively large reverse voltage drop. On-time of rectifier-
GaN transistors have the advantages of low on-resistance and parasitic parameters, fast
realized within a certain load range. In contrast to [14], more thorough analysis of CLLC-BRC with
improve the frequency, efficiency and power density of the DC-DC converters. In contrast to GaN-
was realized under all load conditions, while zero-current switching of the rectifier-side switches was
bidirectional operating modes of CLLC-BRC, zero-voltage switching of the inverter-side switches
explicit and comprehensive design methodology based on PFM is displayed, with the whole level of
solution of resonant frequencies and improved ZVS condition is given in this paper. Also, more
main circuit
control board
Structure of the prototype.

**Figure 10.** Main experimental waveforms of the forward mode. (a) Waveform of \( i_{Lr} \) when \( f_s = 312 \) kHz; (b) waveform of \( i_{Lr} \) when \( f_s = 435 \) kHz; (c) waveform of \( i_{Tr2} \) when \( f_s = 312 \) kHz; (d) waveform of \( i_{Tr2} \) when \( f_s = 435 \) kHz.

**Figure 11.** Main experimental waveforms of the reverse mode. (a) Waveform of \( i_{Lr} \) when \( f_s = 303 \) kHz; (b) waveform of \( i_{Lr} \) when \( f_s = 556 \) kHz; (c) waveform of \( i_{Tr2} \) when \( f_s = 303 \) kHz; (d) waveform of \( i_{Tr2} \) when \( f_s = 556 \) kHz.

**Figure 12.** Efficiency curves of the converter. (a) Forward mode; (b) reverse mode.
5. Conclusions

GaN transistors have the advantages of low on-resistance and parasitic parameters, fast switching speed, low reverse recovery loss and so on. The application of GaN transistors can further improve the frequency, efficiency and power density of the DC-DC converters. In contrast to GaN-based bidirectional CLILLLC resonant converters, one resonant inductance was removed in CLILLLC-BRC, resulting in less loss of resonant components, less volume and more convenience for the design and control of the converter, with similar features of bidirectional conversion preserved. In the bidirectional operating modes of CLILLLC-BRC, zero-voltage switching of the inverter-side switches was realized under all load conditions, while zero-current switching of the rectifier-side switches was realized within a certain load range. In contrast to [14], more thorough analysis of CLILLLC-BRC with solution of resonant frequencies and improved ZVS condition is given in this paper. Also, more explicit and comprehensive design methodology based on PFM is displayed, with the whole level of operating frequency improved by GaN transistors. Experimental results of the prototype with a rated power of 400 W have proved the validity of proposed design methodology, with the whole level of operating frequency that is larger than 0.5 MHz.

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References


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