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A Novel Repetitive Control Enhanced Phase-Locked Loop for Synchronization of Three-Phase Grid-Connected Converters

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Abstract: This paper proposes the enhancement of a synchronous reference frame phase-locked loop in terms of its dynamic response and disturbance rejection capability. The improvements were undertaken in order to upgrade the converter grid support capability required by modern grid codes during grid faults. The proposed repetitive control-based filter is inserted in the loop filter structure of the phase-locked loop. For the initially proposed structure, the necessity of the phase angle error correction term was derived and added at the output of the loop filter. On a set of tests that included (i) phase jump; (ii) voltage sag; (iii) voltage harmonics; (iv) DC offset; (v) random noise and; (vi) frequency change, the synchronization algorithm with the proposed modification showed two desirable characteristics: (i) a high attenuation of oscillations on specific frequencies; and (ii) the instant compensation of the portion of the phase angle jump. Along with the benefits, drawbacks of the proposed synchronization method were noted, the most important being the high dependency of the oscillation attenuation capability on the fundamental frequency drift and susceptibility to high-frequency noise. With the proposed modification, the synchronization algorithm manages to achieve a phase angle settling time not longer than one fundamental frequency period in all of the conducted tests.

Keywords: repetitive control; synchronization; phase-locked loop (PLL); three-phase converter

1. Introduction

The impact of renewable energy sources (RESs) on overall power system stability will continue to increase as their share of generated power increases. Many countries are re-examining and updating existing grid standards in order to enforce advance requirements for integrated RESs that include reactive power support, frequency control, and dynamic grid support [1]. A possible large number of RESs with their inherited intermittency, unpredictability, and spatial variability supplying a vast number of different consumer types creates a difficult problem related to grid power quality and stability [2].

Integration of modern RESs in the grid usually cannot be done directly, but rather through a power electronic-based converter. The control of modern converters is done via digital logic, using devices like digital signal processors (DSPs) and field programmable gate arrays (FPGAs) [3]. It is up to the algorithm implemented in these devices to ensure robust stability, abrupt response, optimal tracking ability, error eradication, and low distortion of the converter's parameters of interest. The control algorithm usually consists of two cascaded control loops: the inner current loop that

plays a fundamental role in closed-loop performance, and the outer voltage loop intended for refining the tracking ability [4]. If the converter control is implemented in the synchronous reference frame, there is also a need for fundamental grid voltage vector phase angle (FGVVPA) estimation for signal conversion between the reference frames, and the fundamental grid voltage vector frequency (FGVVF) estimation for the control loops' decoupling.

The process of the converter's output voltage vector harmonization with the fundamental grid voltage vector is called converter synchronization with the grid. The most popular techniques for FGVVPA tracking today are based on phase-locked loops (PLLs). In the ideal case, synchronization with FGVVPA would be instant and not affected by grid dynamics, grid strength, and power quality problems at the point of common coupling (PCC). Under these conditions, synchronization would not have adverse effects on the quality of the exchanged energy between the converter and the grid. In the real case, synchronization is susceptible to all previously mentioned problems, while situations where FGVVPA are assessed poorly, are related to power quality problems, and even the potentially hazardous operation of the converter [5].

In power systems, synchronous reference frame phase-locked loop (SRF-PLL) is the most extended technique for synchronization with three-phase systems [6]. It has a straightforward tuning procedure and the ability to work effectively under a balanced grid voltage condition. The problem with the SRF-PLL is its inability to accurately estimate FGVVPA and FGVVF during unbalanced or harmonic polluted grid voltages. In the events of phase jumps or voltage sags, SRF-PLL can have a high overshoot of estimated frequency that can lead to the unexpected tripping operation of RES protection, thus disconnecting the RESs from the grid [6]. Reduction of overshoot and the amplitude of oscillations with unbalanced voltage sags can be achieved with the reduction of SRF-PLL bandwidth, resulting in precise but slow synchronization [7]. The problem of unbalanced voltage is overcome by a novel cross-feedback decoupling network used for positive and negative sequence fundamental component extraction in a synchronization structure called the decoupled double synchronous reference frame PLL (DDSRF-PLL) [7,8]. Use of the moving average filter as a harmonic filter in SRF-PLL (MAF-PLL) [9] proved effective in the elimination of periodic disturbances related to voltage imbalance and harmonics, while at the same time reducing the frequency overshoot of conventional SRF-PLL. Its drawback is a slower dynamic response compared to SRF-PLL, making it inadequate for fast change detection [10]. In an attempt to make MAF-PLL eligible to fulfil modern grid codes like German [11], which requires the time for estimation of grid voltage parameters of no more than 25 ms [6], several approaches have been suggested in the literature. Replacement of a conventional proportional-integral (PI) controller with a proportional-integral-derivative (PID) as a loop filter (LF), the incorporation of the lead compensator, narrowing the MAF window length, relocating the MAF in the pre-loop, and the removal of PI controller integral term are some of the suggested approaches [8]. MAF based PLL with the removed integral term and the addition of compensation structure, named the Quasi-Type 1 PLL (QT1-PLL) enables a settling time of less than two cycles of fundamental frequency [10], but that improvement still makes it incompatible with the above-mentioned grid code requirement. Along with synchronous reference frame filtering, another popular group of synchronization algorithms use a stationary reference frame for specific signal extraction. The second-order generalized integrator (SOGI) acts as a quadrature sinusoidal generator using the combination of low pass filter (LPF) for harmonic filtering and orthogonal signal generation, along with the band pass filter (BPF) for harmonic filtering [7,8]. SOGI based PLLs are also advantageous for specific harmonic extraction capability, but at the cost of higher computation burden compared to previously described PLLs [8].

The basic idea of repetitive control (RC) comes from the internal model principle and the fact that if the model that generates the reference is included in a stable closed-loop system, the controlled output tracks the input without the steady-state error. Repetitive controllers belong to the group of intelligent controllers along with neural network, fuzzy logic, and autonomous controllers due to their operation, which emulates biological intelligence [3,4]. For the tracking error eradication, repetitive control uses information from the past and periodic steps for the reference value approach. Applied

in converter control, it has proven to be effective in tracking or rejecting periodic current signals or disturbances of the known and fixed period [12–15], thus improving power quality and reducing tracking error, but showed susceptibility to frequency variation. Used for grid current control, the RC based controller showed excellent tracking and harmonic rejection performance with lower computation burden and higher robustness to grid-impedance variation compared to the proportional-resonant (PR) controller [14]. As the sampling delay presents a limiting factor in high-performance converter current control loops, multisampling methods have been utilized on modern digital control hardware to minimize the equivalent delay, and RC based filters presented in [16,17] were incorporated for single value extraction and periodic disturbance rejection. The self-learning ability of frequency adaptive RC is demonstrated in the synchronization of three-phase converters, where it aided in the harmonic rejection capability of regular SRF-PLL without added substantial computational burden [18].

In this paper, the proposed method for speeding up the dynamic response of SRF-PLL beyond the QT1-PLL designed according to [10], while maintaining disturbance rejection capability on frequencies where common disturbances are to be expected, was based on RC. The proposed method enables instantaneous partial compensation of the phase angle difference in the events of the grid phase-angle jump, and phase angle settling times not longer than one period in all conducted tests. It is reasonable to expect that this behavior would have a positive impact on the overall stability of the system with a high power generation share from RESs in the events of the grid transferring from connected to islanding operation. This transfer can be followed with a substantial phase angle jump that, through phase angle information loss, affects the active and reactive power exchange between RESs and the grid, and influences the voltage and frequency of the grid [19]. This paper provides mathematical proof of the proposed PLL stability, mathematical proof of its ability to track the grid phase angle when the frequency deviates from nominal, a MATLAB code that enables digital implementation of the proposed filter, and benchmarking results in the transient and steady state. In summary, the contributions of this paper are as follows:

- A novel filtering stage is proposed based on RC that enables faster settling times than that of the QT1-PLL designed according to [10], while maintaining the ability of complete disturbance rejection when the grid frequency is nominal.
- To the authors' knowledge, this proposed PLL is the first to offer instantaneous partial compensation of the phase angle difference in the events of grid phase jump.
- The proposed PLL has a higher phase margin than the MAF-PLL or QT1-PLL designed according to [9,10], respectively.
- Validation of the proposed PLL effectiveness was done on a group of comprehensive experiments, with a set of frequencies around and including the nominal.
- The filtering stage of the proposed PLL is provided in a MATLAB code fit for implementation in simulations or on a digital control device.

The rest of this paper is organized as follows. The first part of Section 2 links between the common voltage disturbances and the oscillations in the synchronous reference frame are derived. In the second part, a block representation of the SRF-PLL that will be used for improvement is shown along with its small-signal model. In Section 3, the proposed PLL is described along with its small-signal model, the effects of one freely selectable parameter variation on the system response is discussed, and proof of its stability and phase tracking ability are provided. In Section 4, details of all of the implemented PLLs are provided, followed by the set of tests designed to show the transient response and steady-state performances of the proposed approach compared to other popular PLLs.

2. Low Voltage Grid Disturbances and Their Influence on Phase Locked Loop Synchronization

In this section, the effects of common grid disturbances on SRF-PLL are examined. Mapping of common grid voltage disturbances to synchronous reference frame (dq) oscillations is undertaken in the first part. In the second part, the idea of fundamental grid voltage vector tracking with SRF-PLL is

shown along with the effects of previously described disturbances on the correct fundamental voltage vector estimation.

2.1. Grid Voltage Vector Tracking

In the real grid, voltage disturbances such as phase asymmetry, voltage harmonics, or DC offset are to be expected. DC offset and even harmonics are often neglected in practice, as their amplitude is much lower than other expected disturbances [10], while for the derivation purpose in this paper, the DC offset was considered. Derivation of disturbances will be conducted for a three-phase system without a neutral conductor, the most preferred power converter topology in the industry [4]. Voltages of this system, if voltage asymmetry is expected only in fundamental grid voltage frequency, can be written using symmetrical component analysis as:

$$\begin{aligned} V_a &= V_{a,dc} + \sum_{h=1,7,13\dots} V_h^+ \cos(\theta_h^+) + \sum_{h=-1,-5,-11,-17\dots} V_h^- \cos(\theta_h^-) \\ V_b &= V_{b,dc} + \sum_{h=1,7,13\dots} V_h^+ \cos(\theta_h^+ - \frac{2\pi}{3}) + \sum_{h=-1,-5,-11,-17\dots} V_h^- \cos(\theta_h^- + \frac{2\pi}{3}) \\ V_c &= \underbrace{V_{c,dc}}_{DC} + \underbrace{\sum_{h=1,7,13\dots} V_h^+ \cos(\theta_h^+ + \frac{2\pi}{3})}_{Positive} + \underbrace{\sum_{h=-1,-5,-11,-17\dots} V_h^- \cos(\theta_h^- - \frac{2\pi}{3})}_{Negative} \end{aligned} \quad (1)$$

where h represents the order of harmonic; V_h^\pm and $\theta_h^\pm = h\omega t + \phi_h^\pm$ are the amplitude and phase angle of the h -th positive (+) or negative (-) sequence harmonic; ω is the fundamental frequency; $V_{abc,dc}$ is the DC voltage in phases a , b , or c ; and ϕ_h^\pm is the initial phase angle of the h -th harmonic. Due to the three-wire converter system, zero-sequence voltages were not considered. Applying the Clarke transformation on Equation (1), the system of equations in the stationary reference frame ($\alpha\beta$) can be written as:

$$\begin{aligned} V_\alpha &= V_{\alpha,dc} + \sum_{h=1,7,13\dots} V_h^+ \cos(\theta_h^+) + \sum_{h=-1,-5,-11,-17\dots} V_h^- \cos(\theta_h^-) \\ V_\beta &= V_{\beta,dc} + \sum_{h=1,7,13\dots} V_h^+ \sin(\theta_h^+) + \sum_{h=-1,-5,-11,-17\dots} V_h^- \sin(\theta_h^-) \end{aligned} \quad (2)$$

$$\begin{aligned} V_{\alpha,dc} &= V_{a,dc} - 0.5V_{b,dc} - 0.5V_{c,dc} \\ V_{\beta,dc} &= 0V_{a,dc} + \frac{\sqrt{3}}{2}V_{b,dc} - \frac{\sqrt{3}}{2}V_{c,dc} \end{aligned} \quad (3)$$

Voltages from Equations (2) and (3) can be transferred in the synchronous reference frame (dq) using the Park transformation, after which the following equations are obtained:

$$\begin{aligned} V_d &= V_{d,osc}(\hat{\theta}) + \sum_{h=1,7,13\dots} V_h^+ \cos(\theta_h^+ - \hat{\theta}) + \sum_{h=-1,-5,-11,-17\dots} V_h^- \cos(\theta_h^- + \hat{\theta}) \\ V_q &= V_{q,osc}(\hat{\theta}) + \sum_{h=1,7,13\dots} V_h^+ \sin(\theta_h^+ - \hat{\theta}) + \sum_{h=-1,-5,-11,-17\dots} V_h^- \sin(\theta_h^- + \hat{\theta}) \end{aligned} \quad (4)$$

$$\begin{aligned} V_{d,osc}(\hat{\theta}) &= V_{\alpha,dc} \cos(\hat{\theta}) + V_{\beta,dc} \sin(\hat{\theta}) \\ V_{q,osc}(\hat{\theta}) &= -V_{\alpha,dc} \sin(\hat{\theta}) + V_{\beta,dc} \cos(\hat{\theta}) \end{aligned} \quad (5)$$

In the previous equations, $\hat{\theta}$ presents an instantaneous phase angle of the synchronous reference frame vector. Let positive fundamental grid voltage phase angle (θ_1^+) from Equation (4) be written as a separated term while all others are combined in residue function. Then, under the assumption that the fundamental grid voltage vector rotation speed matches the rotation speed of the synchronous reference frame vector (quasi-locked state), the form presented in Equation (6) can be obtained:

$$\begin{aligned} V_d &= V_1^+ \cos(\theta_1^+ - \hat{\theta}) + f(\omega, 2\omega, 6\omega, 12\omega \dots) \\ V_q &= V_1^+ \sin(\theta_1^+ - \hat{\theta}) + f(\omega, 2\omega, 6\omega, 12\omega \dots) \end{aligned} \quad (6)$$

The oscillating term in the previous equation that is a consequence of voltage disturbances is modeled as $f(\omega, 2\omega, 6\omega, 12\omega, \dots)$. The relationship between oscillations in the dq reference frame and considered disturbances under the quasi-locked state is presented in Table 1.

Table 1. Origin of oscillations in synchronous reference frame voltages in the quasi-locked state.

Oscillation Frequency (dq)	Origin (abc)
ω	DC offset
2ω	Fundamental voltage unbalance
6ω	5th and/or 7th harmonic
12ω	11th and/or 13th harmonic
...	...

The ratio of quadrature and direct voltage components from Equation (6) can be written as:

$$\frac{V_q}{V_d} = \frac{V_1^+ \sin(\theta_1^+ - \hat{\theta})}{V_1^+ \cos(\theta_1^+ - \hat{\theta}) + f(\omega, 2\omega, 6\omega, 12\omega \dots)} + \frac{f(\omega, 2\omega, 6\omega, 12\omega \dots)}{V_1^+ \cos(\theta_1^+ - \hat{\theta}) + f(\omega, 2\omega, 6\omega, 12\omega \dots)}. \quad (7)$$

Under the assumption of a small-angle difference between $(\theta_1^+ - \hat{\theta})$, and the surmise $V_1^+ \cos(\theta_1^+ - \hat{\theta}) \gg f(\omega, 2\omega, 6\omega, 12\omega \dots)$, Equation (7) can be simplified as:

$$\frac{V_q}{V_d} = \frac{\sin(\theta_1^+ - \hat{\theta})}{\cos(\theta_1^+ - \hat{\theta})} + \frac{f(\omega, 2\omega, 6\omega, 12\omega \dots)}{V_1^+ \cos(\theta_1^+ - \hat{\theta})}. \quad (8)$$

If the second term from the right side in Equation (8) is transferred on the left side of the equation and inverse tangent function is applied, the following relation is obtained:

$$\theta_1^+ - \hat{\theta} = \arctan\left(\frac{V_q}{V_d} - \frac{f(\omega, 2\omega, 6\omega, 12\omega \dots)}{V_1^+ \cos(\theta_1^+ - \hat{\theta})}\right). \quad (9)$$

If no oscillating term in Equation (9) exists, it can be concluded that the angle difference $\theta_1^+ - \hat{\theta}$ is linearly dependent to the output of inverse tangent function applied to the ratio of quadrature and direct voltage component. With the regulation of the inverse tangent function output to zero, alignment of θ_1^+ and $\hat{\theta}$ can be achieved. Due to the grid voltage disturbances, this premise is not valid in general case.

In order to create the small-signal model of PLL that uses the previously mentioned principle for synchronization, the linearized model of dependence presented in Equation (9) has to be obtained. If an inverse tangent function is applied on both sides of Equation (8), the following relation is obtained:

$$\arctan\left(\frac{V_q}{V_d}\right) = \arctan\left(\frac{\sin(\theta_1^+ - \hat{\theta})}{\cos(\theta_1^+ - \hat{\theta})} + \frac{f(\omega, 2\omega, 6\omega, 12\omega \dots)}{V_1^+ \cos(\theta_1^+ - \hat{\theta})}\right). \quad (10)$$

If we consider Equation (10) near the normal operating point (angle difference $\theta_1^+ - \hat{\theta}$ near zero), approximations $\sin(\theta_1^+ - \hat{\theta}) \approx \theta_1^+ - \hat{\theta}$ and $\cos(\theta_1^+ - \hat{\theta}) \approx 1$ can be made. The previous equation is then transferred in the form:

$$\arctan\left(\frac{V_q}{V_d}\right) = \arctan(\theta_1^+ - \hat{\theta}) + \frac{f(\omega, 2\omega, 6\omega, 12\omega \dots)}{V_1^+}. \quad (11)$$

Applying the Maclaurin series expansion on the right-side of Equation (11) and considering only the first two linearization terms provides the following relation applicable for small-signal modeling:

$$\arctan\left(\frac{V_q}{V_d}\right) = \theta_1^+ - \hat{\theta} + \frac{f(\omega, 2\omega, 6\omega, 12\omega \dots)}{V_1^+} \tag{12}$$

2.2. SRF-PLL Small-Signal Model

One of the simplest synchronization algorithms with a broad theoretical application in RESs is SRF-PLL, with a proposed block diagram presented in Figure 1a. The Laplace complex variable is denoted with p , expected fundamental frequency with ω_{ff} , fundamental frequency correction signal with $\Delta\omega$, and the error signal (output of the inverse tangent function) with $e(p)$. The phase-locked loop typically consists of a phase detector (PD) that generates a signal with phase error information, LF for a phase error elimination, and a frequency/phase generation block called the voltage-controlled oscillator (VCO) [5,7–10]. The most commonly used LF is a proportional-integral (PI) controller, and in this paper, the parallel form with the proportional gain k_p and the integral time constant T_i was chosen. The appropriate small-signal model of SRF-PLL can be obtained using Figure 1a and Equation (12). This model is shown in Figure 1b, where

$$D(p) = L\left(\frac{f(\omega, 2\omega, 6\omega, 12\omega \dots)}{V_1^+}\right),$$

and L denotes the Laplace operator. Compared to the control structures presented in [7,8,10], the proposed structure in this paper uses an additional inverse tangent function eligible to operate in four quadrants (atan2). This modification makes the loop gain independent of the grid voltage amplitude, reduces the nonlinearity of PLL, and avoids large outputs that can be expected with plain normalization in the case of zero division at the cost of higher computational effort [8,10].

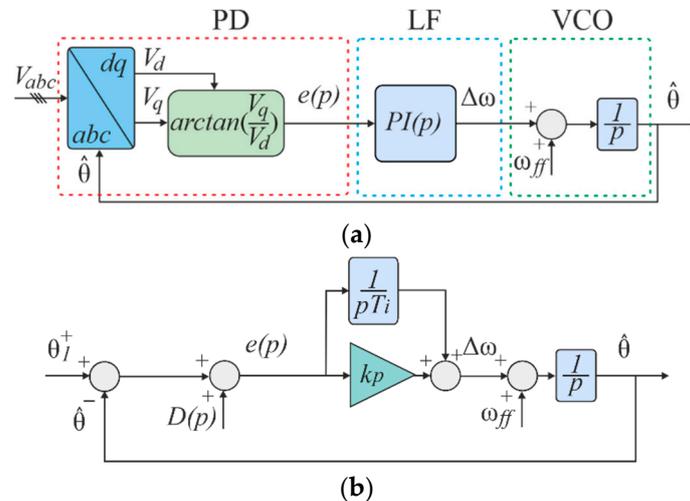


Figure 1. Synchronous reference frame phase-locked loop (PLL). (a) Block diagram; (b) small-signal model.

Using the provided small-signal model, the open-loop transfer function can be obtained as:

$$G_{ol-srf}(p) = \frac{\hat{\theta}}{\theta_1^+} \Big|_{D(p)=0} = \left(k_p + \frac{1}{pT_i}\right) \frac{1}{p} \tag{13}$$

One of the ways to obtain unknown proportional gain and integral time constant is by comparing the closed-loop transfer function and the canonical second-order transfer function [5,7] as in Equation (14), where the desired natural frequency ω_n and damping ratio ζ are selected.

$$G_{cl-srf}(p) = \frac{G_{ol-srf}(p)}{1 + G_{ol-srf}(p)} = \frac{k_p p + \frac{1}{T_i}}{p^2 + k_p p + \frac{1}{T_i}} = \frac{2\zeta\omega_n p + \omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}. \tag{14}$$

With the comparison of appropriate coefficients, the proportional gain and the integral time can be obtained as:

$$\begin{aligned} k_p &= 2\zeta\omega_n \\ T_i &= \frac{1}{\omega_n^2} \end{aligned} \tag{15}$$

3. Description of the Proposed PLL and Design Guidelines

The problem for accurate synchronization, as presented in Equation (12), are disturbances that are periodic in nature that are multiples of the fundamental frequency. Possible oscillations caused by disturbances have relatively low frequency compared to the bandwidth of SRF-PLL implying, since usually the PI controller is used as the LF, that not sufficient attenuation of these disturbances is provided [5,8].

3.1. Enhancement of SRF-PLL with Repetitive Control Based Filter

The initially proposed enhancement of SRF-PLL is shown in Figure 2a, inspired by the RC presented in [16,17] used for current ripple elimination in multi-sampled digitally controlled systems. The only modification of SRF-PLL is located in its LF before the PI controller. RC is implemented in a negative feed-back, classical plug-in manner with the idea of removing residual disturbance error that cannot be eliminated by the controller. The details of the proposed modification, from the error signal $e(p)$ to the filtered error signal $\bar{e}(p)$ are presented in Figure 2b. Detail representation of the modification shows that the proposed repetitive part $RC(p)$ consists of only one gain block with gain K , one delay line with delay time T , and one feedback line. The value T corresponds to the period of fundamental disturbance whose cancellation, along with the cancellation of its frequency multiples, is desired. Additionally, it presents a period for steps that the repetitive part uses to approach the desired value [16,17].

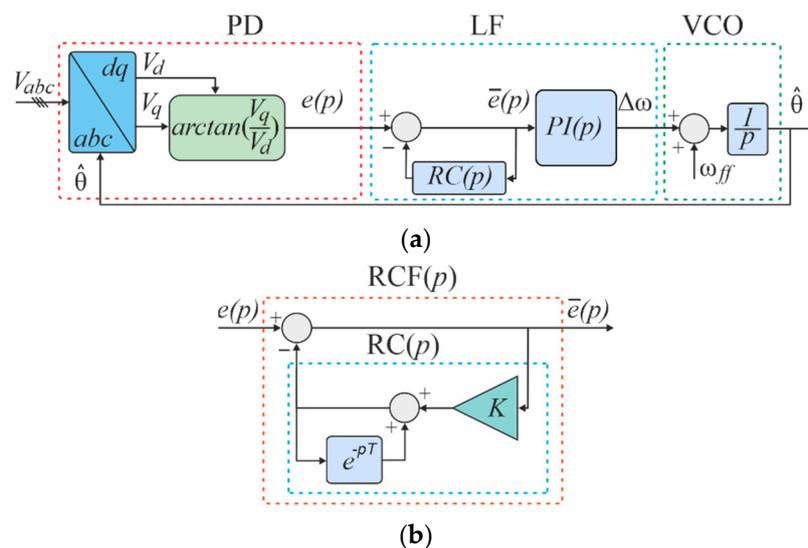


Figure 2. Block diagrams. (a) synchronous reference frame phase-locked loop (SRF-PLL) with initial modification; (b) repetitive disturbance rejector.

Transfer functions of the RC and the part from the error signal $e(p)$ to the filtered error signal $\bar{e}(p)$ named the repetitive control filter (RCF) are provided in the complex and discrete domain in Equations (16) and (17), respectively. Value N is the closest integer of the ratio between delay time T

and sampling period T_s and does not change, since no frequency adaptive method has been suggested in this paper.

$$RC(p) = \frac{K}{1 - e^{-pT}} \vee RC(z) = \frac{K}{1 - z^{-N}}, \tag{16}$$

$$RCF(p) = \frac{1 - e^{-pT}}{K + 1 - e^{-pT}} \vee RCF(z) = \frac{1 - z^{-N}}{K + 1 - z^{-N}}. \tag{17}$$

The Bode plot of the RCF along with the filter frequently used in modern synchronization algorithms, MAF, is presented in Figure 3. From the Bode plot, it can be observed that the proposed filter presents MAF with the additional derivative term. RCF blocks the DC component and passes high-frequency components with the attenuation determined with parameter K . A lower value of K shifts the Bode amplitude plot of the RCF upwards, as can be observed from Equation (17).

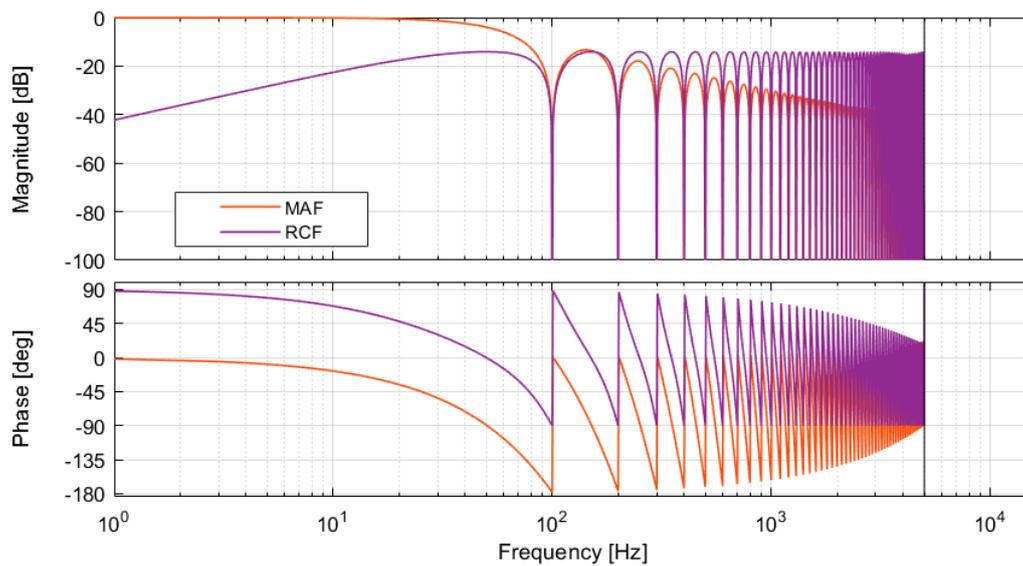


Figure 3. Bode plots of moving average filter (MAF) and repetitive control filter (RCF) (parameters are selected according to Table 2).

3.2. Phase and Frequency Tracking Ability of the Proposed PLL

The derived small-signal model of the SRF-PLL with the initially proposed modification, using Equations (12) and (16) and Figure 2, is presented in Figure 4. The phase tracking ability of the initially proposed PLL has to be examined since the proposed filter blocks the DC component of the input signal. Dependence of the error signal $e(p)$ on the fundamental grid phase angle, when there are no additional disturbances in the system ($D(p) = 0$) can be written as Equation (18):

$$e(p) = \frac{p^2 T_i (1 - e^{-pT} + K)}{p^2 T_i (1 - e^{-pT} + K) + (1 + p k_p T_i) (1 - e^{-pT})} \theta_1^+(p) \tag{18}$$

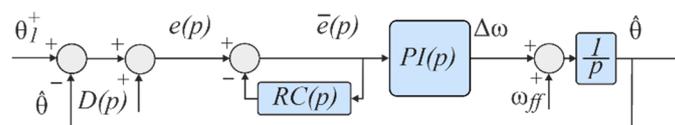


Figure 4. Small signal model of SRF-PLL with the initially proposed modification.

For a steady-state error analysis, the final value theorem can be used. When the proposed structure is subjected to a phase angle jump ($\theta_1^+(p) = \frac{\Delta\theta}{p}$, where $\Delta\theta$ is arbitrary phase jump angle at constant and nominal grid frequency), a steady-state error signal is calculated using L'Hospital's Rule as follows:

$$\begin{aligned} \lim_{p \rightarrow 0} pe(p) &= \lim_{p \rightarrow 0} p \frac{p^2 T_i (1 - e^{-pT} + K)}{p^2 T_i (1 - e^{-pT} + K) + (1 + pk_p T_i) (1 - e^{-pT})} \frac{\Delta\theta}{p} \\ \lim_{p \rightarrow 0} pe(p) &= 0 \Delta\theta \end{aligned} \tag{19}$$

From the previous equation, it can be concluded that the proposed structure has no problem in the steady-state tracking of abrupt (step) fundamental grid voltage phase angle change. Usable PLL also has to have a phase tracking ability when the grid fundamental frequency is different than the nominal ($\theta_1^+(p) = \frac{\Delta\omega}{p^2}$, where $\Delta\omega$ is the arbitrary deviation of the fundamental frequency from the nominal). When substituted in Equation (18), Equation (20) can be obtained as:

$$\begin{aligned} \lim_{p \rightarrow 0} pe(p) &= \lim_{p \rightarrow 0} p \frac{p^2 T_i (1 - e^{-pT} + K)}{p^2 T_i (1 - e^{-pT} + K) + (1 + pk_p T_i) (1 - e^{-pT})} \frac{\Delta\omega}{p^2} \\ \lim_{p \rightarrow 0} pe(p) &= \frac{T_i}{T} K \Delta\omega \end{aligned} \tag{20}$$

Equation (20) shows the inability of the initially proposed structure to follow the fundamental grid voltage phase angle without a steady-state error in situations when the frequency varies from the nominal. In order to solve this problem, additional compensation consisting of a gain KT_i/T from the output of $PI(p)$ to the estimated FGVVPA is proposed. In Figure 5a, a complete block diagram of the proposed PLL is presented, hereafter called the repetitive control enhanced synchronous reference frame phase-locked loop (RCE-PLL). Figure 5b presents the small-signal model of the RCE-PLL as the small-signal model from Figure 5c, only in a different form. The $\hat{\theta}_1^+$ presents an estimated angle of the positive fundamental grid voltage vector, and it differs from the reference frame vector angle $\hat{\theta}$ when the frequency differs from the nominal.

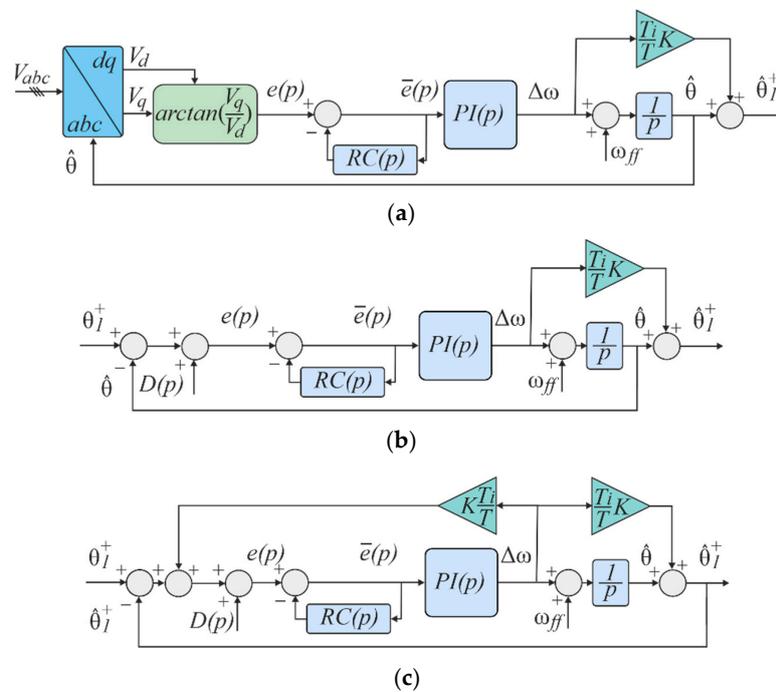


Figure 5. RCE-PLL. (a) Block diagram; (b) small-signal model; (c) different form of the small-signal model.

Figure 6 presents the comparison between the implemented model (Figure 5a) and the suggested small-signal model (Figure 5c) during transients in order to test the credibility of the small-signal model for later stability analysis. Testing was done in MATLAB/Simulink R2018b (Update 5) with the RCF implementation presented in Appendix A used for the experimental testing. Both models had an identical parameter setup as shown in Table 2. Algorithms were tested on the following situations: (i) 0.0 s, initial synchronization; (ii) 0.1 s, phase angle jump of 30° ; and (iii) 0.2 s, frequency step change to 52 Hz. As depicted in Figure 6, the proposed small-signal model could precisely predict the transient behavior of RCE-PLL. Since the presented RC uses a time delay of 10 ms, the disturbance eradication steps of the same period can be observed in Figure 6.

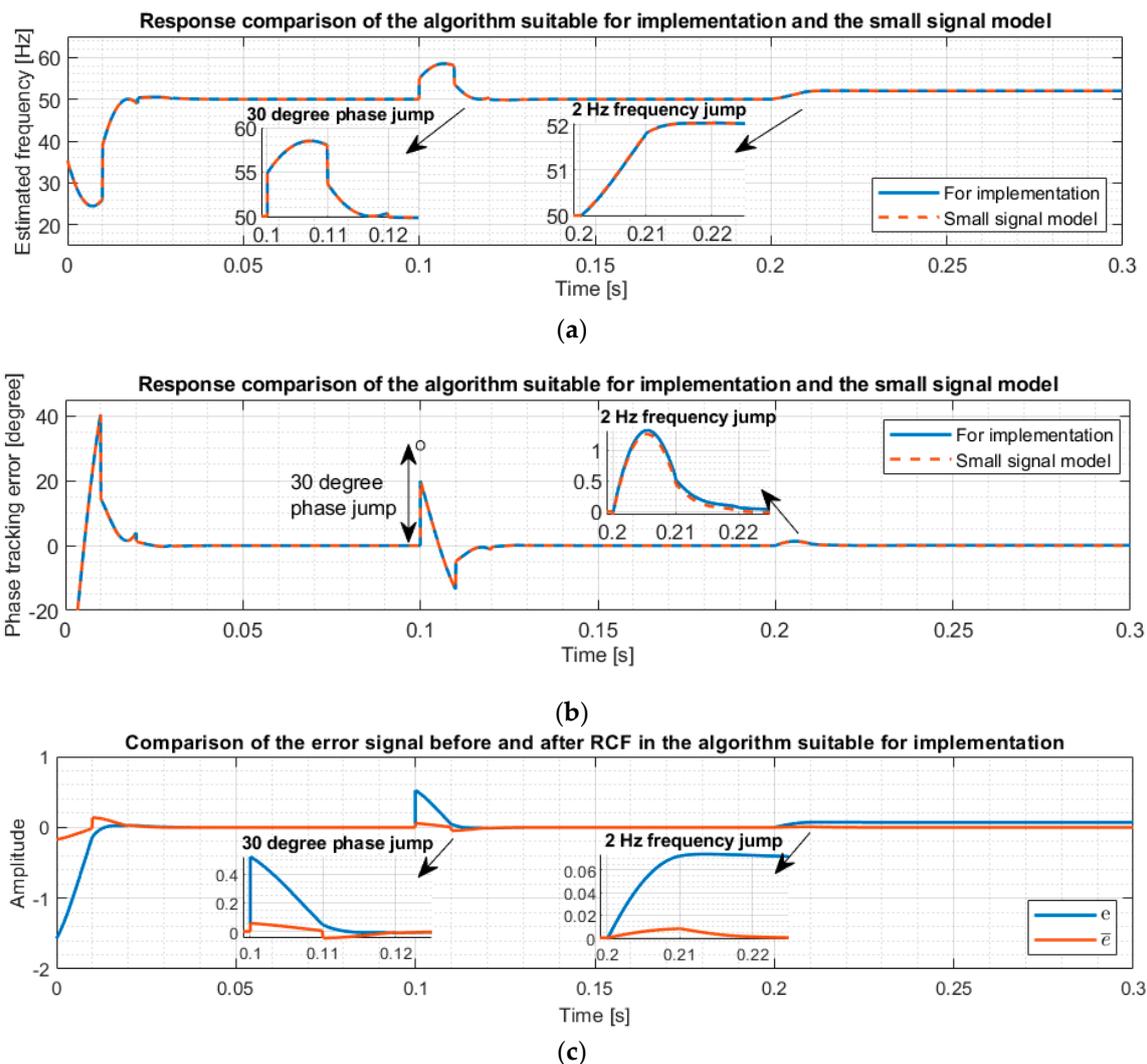


Figure 6. Dynamic behavior of RCE-PLL and its small-signal model. (a) Estimated frequency; (b) fundamental grid voltage vector phase angle error; (c) error signal before and after the RCF.

Using Figure 6, two fundamental roles of online compensation block can be observed. First, from Figure 6b, it can be seen that although the phase jump in 0.1 s is 30° , at that moment, a phase angle error signal of around 20° can be observed. The RCF can immediately pass part of the step-change signal from the input to the output. Through the proportional term of the PI controller and the online compensation term, this step change of the output of RCF can be immediately transferred to the estimated voltage vector angle prediction. Second, observing the Figure 6c constant error signal $e(p)$ from 0.2 s onward can be noted when the frequency is different from the nominal, but the filtered

error signal $\bar{e}(p)$ fades away after about 20 ms. This implies that the compensation term is uses the accumulated value in the integrator part of the PI controller for phase compensation.

3.3. Stability Analysis of RCE-PLL

For stability analysis, the transfer function of the system will be rearranged to obtain the form presented in [18], convenient for the stability analysis of a system with a plug-in repetitive controller [12–14,18]. Using Figure 5c, the closed-loop transfer function of RCE-PLL can be written as:

$$G_{cl}(p) = \frac{\hat{\theta}_1^+}{\theta_1^+} \Big|_{D(p)=0} = \frac{RCF(p)PI(p)(\frac{1}{p} + \frac{T_i}{T}K)}{1 + RCF(p)PI(p)\frac{1}{p}} \quad (21)$$

Using simple mathematic manipulations, Equation (21) can be rewritten in the form of Equation (22). According to this equation, the closed-loop transfer function can be presented as a series connection of four subsystems, as shown in Figure 7.

$$G_{cl}(p) = (1 - e^{-pT}) \cdot \frac{PI(p)\frac{1}{p}}{1 + PI(p)\frac{1}{p}} \cdot \frac{1}{1 - \left(1 - \frac{K}{1 + PI(p)\frac{1}{p}} e^{pT}\right) e^{-pT}} \cdot (1 + p\frac{T_i}{T}K) \quad (22)$$

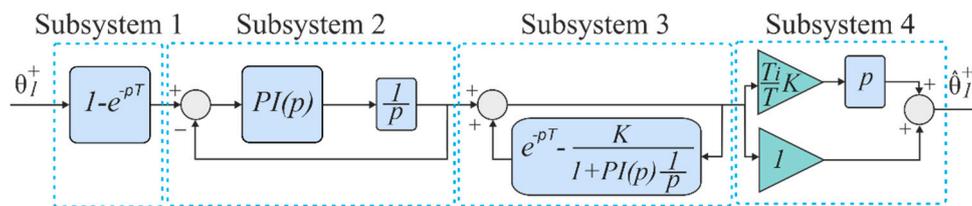


Figure 7. Representation of the RCE-PLL closed-loop transfer function as a series connection of four subsystems.

For every phase angle oscillation with a frequency that is an integer multiple of inverse time delay T , the output of the subsystem 1 from Figure 7 in the steady-state will reach 0. This proves the ability of RCE-PLL to successfully eliminate periodic disturbances of the selected fundamental frequency and its multiples. As can be seen from the same figure, subsystem 2 is just the SRF-PLL without any modification. According to [18], two sufficient stability conditions for SRF-PLL with plug-in RC are:

1. The roots $1 + PI(p)\frac{1}{p}$ being in the left half-plane of the complex plane. This stability condition can be fulfilled with appropriate controller parameter selection using Equation (15).
2. For all frequencies below the Nyquist frequency ($\omega \in [0, \pi/T_s]$), the following equation should be applicable:

$$\left| e^{-j\omega T} - \frac{Ke^{j\omega T}}{1 + PI(j\omega)\frac{1}{j\omega}} e^{-j\omega T} \right| < 1 \quad (23)$$

Equation (23) is obtained after transforming the feedback term of subsystem 3 into the time-domain ($p \Leftrightarrow j\omega$). Using the assumption $|e^{-j\omega T}| \leq 1$, a sufficient stability condition can be derived in Equation (24).

$$0 < |K| < 2 \left| 1 + PI(j\omega)\frac{1}{j\omega} \right| \quad (24)$$

The only one freely adjustable parameter is K and in the next subsection, the method for its optimal selection is proposed.

3.4. Optimal Value of Parameter K

For the selection of the optimal value of parameter K in this paper, the iterative approach was suggested. In the first step, the parameters of the PI controller can be calculated according to Equation (15) with the selection of the natural frequency and damping ratio. For that selection of parameters, the optimal value of K is determined with the simulation using the small-signal model and control system analysis (like MATLAB/Simulink and Linear Analysis Tool), considering Equation (24) as the upper limit. The last two steps are repeated until the eventual combination of the PI controller parameters and K is obtained, which meets the design criteria (like phase margin or settling time), if possible. In addition, to be considered during this procedure, while inspecting Equation (17), is that smaller values of K provide smaller attenuation of disturbances not located on predetermined frequencies for attenuation (notches).

An illustration of the phase and frequency settling times (inside the 2% band) as a function of parameter K for different values of natural frequency and constant damping ratio (0.707) is presented in Figure 8a. Phase margin and crossover frequency obtained using the above-mentioned toolbox are presented in Figure 8b. From the latter figure, a tendency can be observed of decreasing phase margin for the increase of natural frequency.

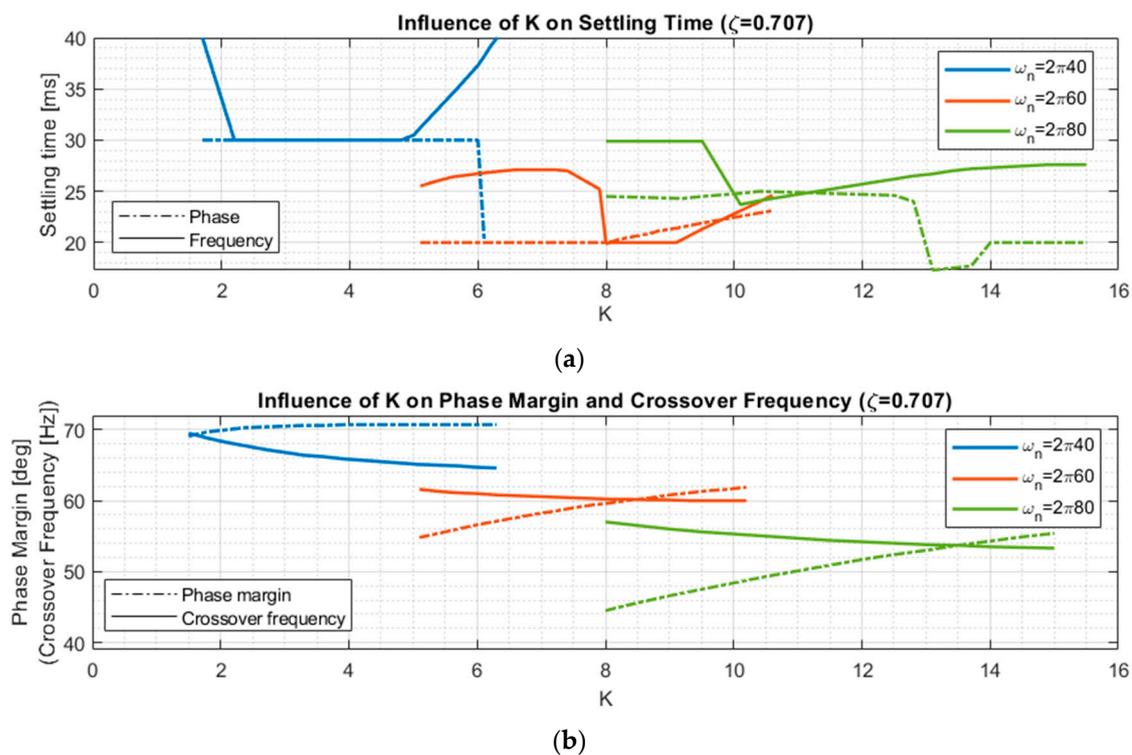


Figure 8. Influence of parameter K on different aspects of the system for different PI controller parameters. (a) Phase angle and frequency settling time; (b) Phase margin and crossover frequency.

Using Figure 8, the combination of natural frequency $\omega_n = 2\pi 60$ rad/s and parameter $K = 8.1$ is selected. This selection enables the RCE-PLL for both a phase and frequency settling time inside the 2% band for no more than 20 ms, according to the Linear Analysis Tool. Finally, open- and closed-loop Bode plots of RCE-PLL along with other PLLs (designed according to Table 2) used for comparison are presented in Figure 9a,b, respectively. RCE-PLL has the largest crossover frequency, and its phase margin is second only to SRF-PLL. Figure 9b shows an envelope of RCE-PLL closed-loop gain at about -5 dB with a slope of 0 dB/dec after the first designed disturbance rejection frequency. Compared to -20 dB/dec of QT1- and -40 dB/dec of MAF-PLL, it is to be expected that the eventual occurrence of disturbances that are not considered for rejection when the RCE-PLL is designed, might not have

sufficient attenuation. Finally, degradation of the RCE-PLL FGVVPA estimation performance can be expected in the presence of evenly distributed noise, high-frequency noise, or interharmonics. The occurrence of interharmonics is possible in a weak grid that contains a substantial share of photovoltaic inverters with the maximum power point tracking algorithm operating with low output power, arc furnaces, asynchronous conversion systems, or wind turbines with substantial mechanical oscillations [20]. One can speculate based on the provided information that the application of RCE-PLL is limited to the control of converters with decent quality voltage sensors, connected to a strong grid with low-frequency drift, and copes with disturbances related to voltage imbalance or harmonics.

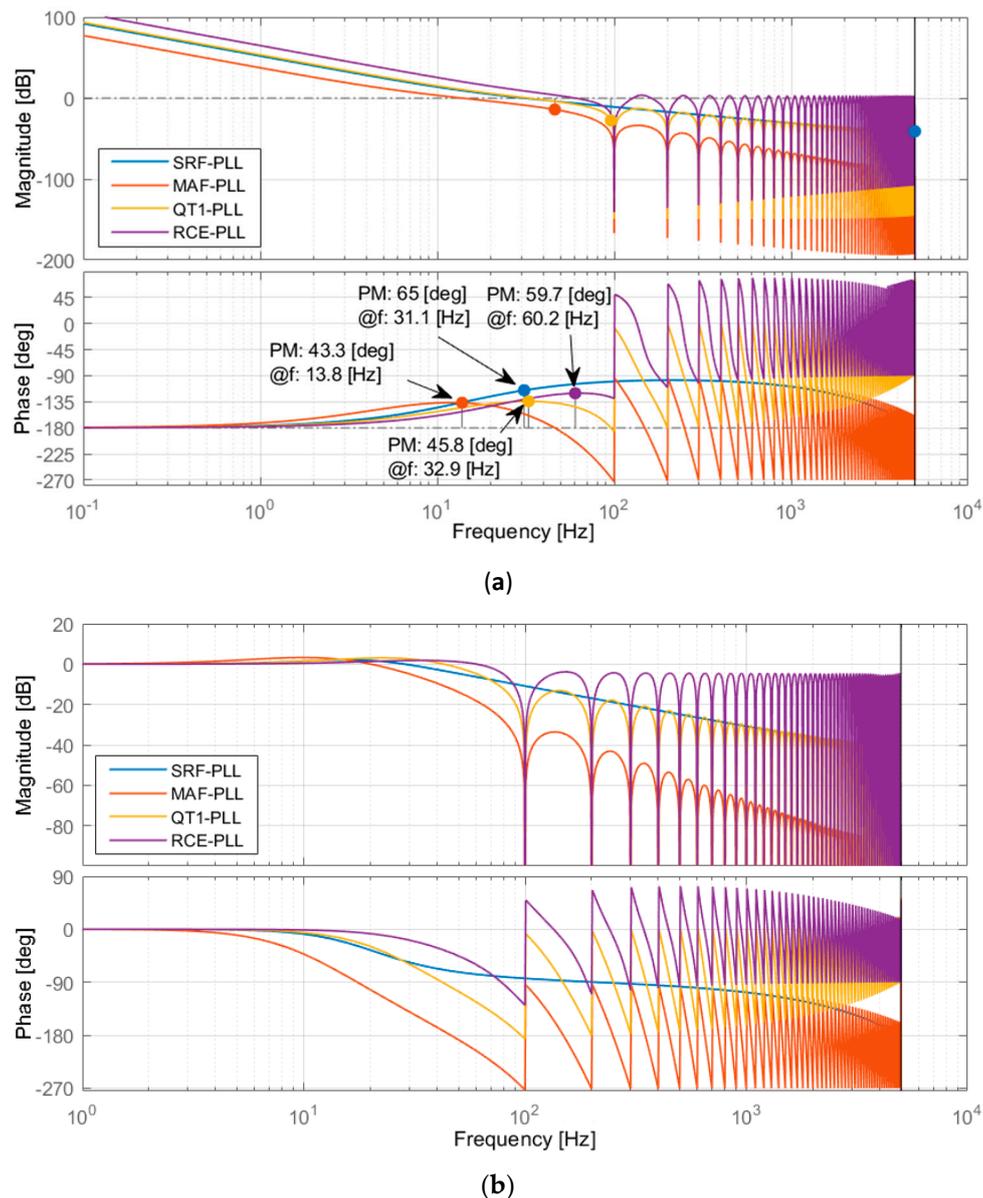


Figure 9. RCE-PLL and other algorithms used for the experimentation (parameter setup as in Table 2). (a) Open-loop bode plots; (b) closed-loop bode plots.

4. Main Results

The performance of the proposed algorithm was tested on dedicated hardware in the laboratory. For the sake of comparison, SRF-PLL, MAF-PLL, QT1-PLL, and RCE-PLL were operated independently of one another in parallel using the same voltage measurements.

4.1. Experiment Setup and Testing Methodology

The laboratory setup is shown in Figure 10 where the setup consists of a dSpace ds1103 controller board and a PC with installed MATLAB/Simulink R2018b (Update 5) and ControlDesk 6.4 R2018b (Patch 1) software. All synchronization algorithms were compiled and executed in parallel on the board. RCF was implemented using the MATLAB function presented in Appendix A. The board also hosts the functions designed for three-phase voltage emulation with programmable disturbances and harmonics. Generated voltages are sent through analogue outputs of the board to analogue inputs of the same board. Compiled algorithms use readings of those analogue inputs as if they are the actual three-phase voltages from sensors. The exact fundamental vector phase angle and rotation speed of the generated voltages are obtainable at the output of the emulation functions and used for the settling times calculations.

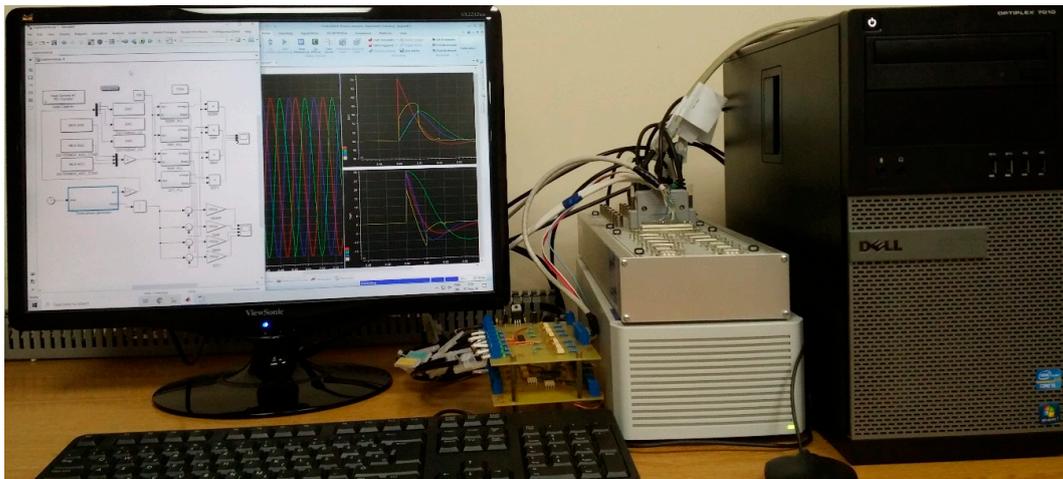


Figure 10. Photograph of the experimental setup.

Details of the algorithm implementation are provided in Table 2. For the selected parameter values of all tested algorithms, the Bode plot can be seen in Figure 9. Tuning of the MAF-PLL was done according to [9], while the parameters of QT1-PLL were selected using [10] as a guide.

Table 2. Details of the implemented algorithms.

Algorithm	Parameter	Value
-	Sampling time	100 μ s
All	Execution speed	10 kHz
RCE-PLL	Natural frequency, ω_n	$2\pi 60$ rad/s
	Damping ratio, ζ	0.707
	Proportional gain, k_p	533.146
	Integral time, T_i	7.04 μ s
	Delay length, N	100
	Coefficient, K	8.1
	Expected fundamental frequency, ω_{ff}	$2\pi 50$ rad/s
SRF-PLL	Natural frequency, ω_n	$2\pi 20$ rad/s
	Damping ratio, ζ	0.707
	Proportional gain, k_p	177.715
	Integral time, T_i	63.32 μ s
	Expected fundamental frequency, ω_{ff}	$2\pi 50$ rad/s
MAF-PLL	Coefficient, b	2.4
	Proportional gain, k_p	83.333
	Integral time, T_i	345.6 μ s
	MAF window length, N	100
	Expected fundamental frequency, ω_{ff}	$2\pi 50$ rad/s
QT1-PLL	Proportional gain, k_p	92.34
	Expected fundamental frequency, ω_{ff}	$2\pi 50$ rad/s
	MAF window length, N	100

For the settling time calculation in all tests, the ± 0.1 Hz band in the case of frequency and $\pm 0.8^\circ$ band in the case of phase error were used [21].

The transient behavior of the selected algorithms will be shown in the event of:

1. Phase jump;
2. Voltage sag;
3. Voltage harmonics; and
4. Frequency step and ramp change.

The comparison of selected algorithms (that are implemented as frequency nonadaptive) in a steady-state was done on a set of tests that included:

1. Voltage sag with grid frequency variation;
2. Voltage harmonics with grid frequency variation;
3. DC offset; and
4. Random noise.

4.2. Transient Behavior of Selected Algorithms

4.2.1. Phase Jump

Responses of the tested algorithms in the situation of a $+30^\circ$ phase jump at the instance of 0.5 s were examined and shown in Figure 11. The voltage waveform is shown in Figure 11a while Figure 11b shows the estimated frequency of each algorithm. Significant estimated frequency overshoot in the moment of the phase jump can be observed with SRF-PLL, which can lead to unexpected tripping operation [6]. QT1- and MAF-PLL had the lowest overshoot on the tested range of phase jumps, making the converter using them the least susceptible to the mentioned unexpected tripping. The frequency settling times for SRF-, MAF-, QT1- and RCE-PLL were 47 ms, 83 ms, 44 ms, and 28.7 ms, respectively. Figure 11c shows the difference between the actual and estimated fundamental voltage vector phase angle. Phase angle settling times were 38 ms, 72 ms, 29 ms, and 20 ms for the algorithms with the previously listed order. The RCE-PLL could not meet the 25 ms time mark due to the frequency settling time that took almost 4 ms longer. From the same figure, it can be observed that RCE-PLL can compensate about one-third of the phase jump error instantly with the provided selection of parameters.

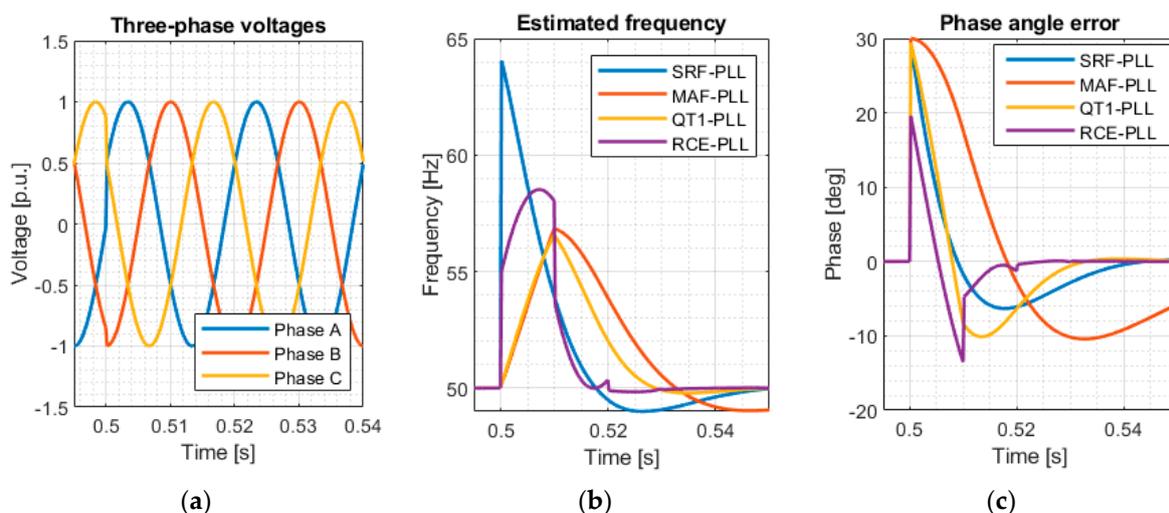


Figure 11. The $+30^\circ$ phase jump test. (a) Grid voltage waveforms; (b) estimated grid frequency; (c) phase angle error.

4.2.2. Voltage Sag

Selected algorithms were tested on the Type C voltage sag with a depth of 0.7 with the rectangular transition, as it is one of the most frequent sags with the depth chosen from most often to the expected range [22]. The results are summarized in Figure 12. Voltage sag occurred at the instance of 0.5 s as can be noticed from the voltage waveform in Figure 12a. The estimated frequency displayed in Figure 12b shows the inability of SRF-PLL to suppress the inverse voltage component, which led to undamped oscillations. MAF-, QT1-, and RCE-PLL can successfully suppress this component for 32 ms, 25 ms, and 19.5 ms in the case of frequency, and 19 ms, 9 ms, and 11 ms in the case of phase angle (observable in Figure 12c), respectively, making QT1-PLL and RCE-PLL eligible for operation using 25 ms as a criterion.

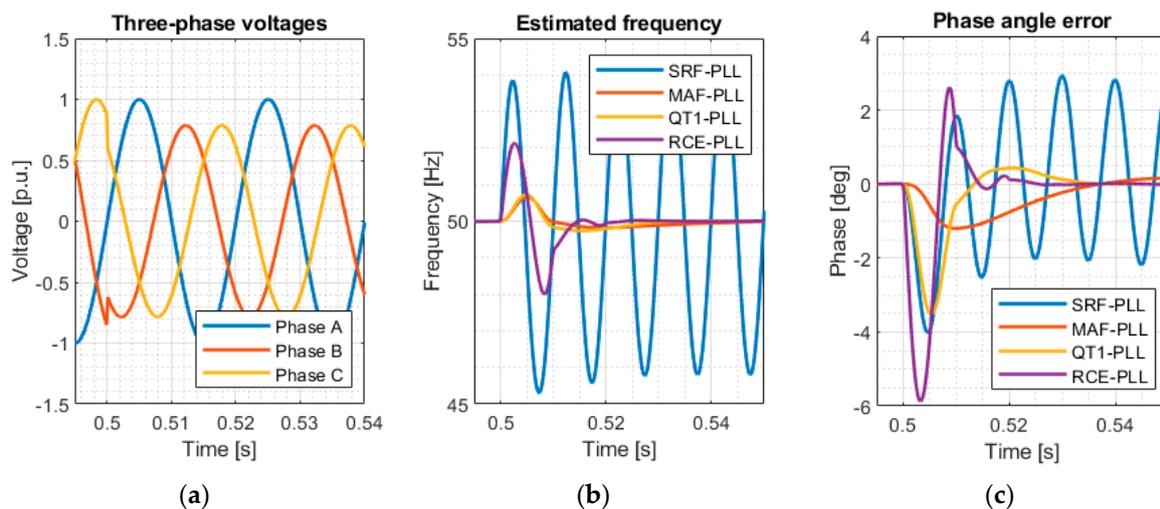


Figure 12. Voltage sag Type C, depth 0.7 test. (a) Grid voltage waveforms; (b) estimated grid frequency; (c) phase angle error.

4.2.3. Voltage Harmonics

The synchronization algorithm to be implemented in modern power grids should be able to estimate voltage parameters quickly and reliably in the presence of voltage harmonics. For a voltage harmonic test, the harmonic amplitudes shown in Table 3 were selected. Figure 13 shows the response of each tested algorithm on the voltage harmonics. As shown in Table 1, the listed harmonics will occur at six-fold and twelve-fold fundamental frequency. When the fundamental frequency is nominal MAF-, QT1- and RCE-PLL can completely suppress these disturbances. It takes 9 ms for QT1- and MAF-PLL, and 16 ms for RCE-PLL to achieve frequency settling, with a transient response shown in Figure 13b. For the phase angle estimation displayed in Figure 13c, RCE-PLL required 10 ms, SRF-PLL 5 ms, while the other two algorithms had a transient response that did not leave the $\pm 0.8^\circ$ band.

Table 3. The amplitude of each harmonic during the test.

Harmonic Order	Amplitude (%) ¹
5th	6
7th	5
11th	3.5

¹ With respect to the fundamental.

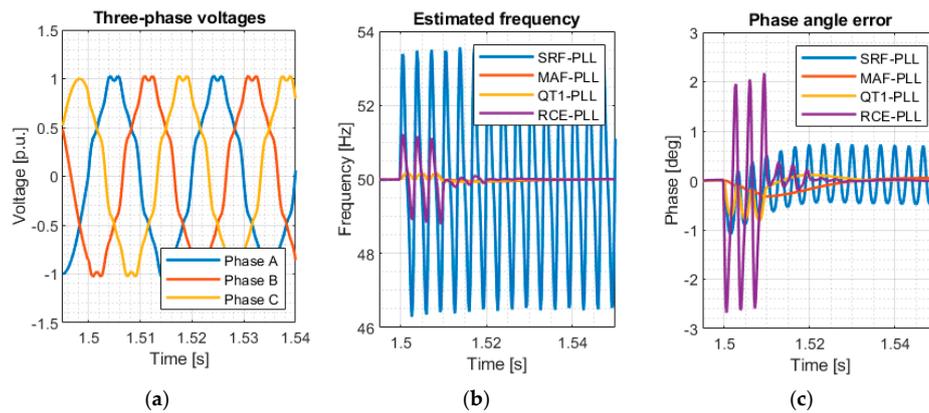


Figure 13. Voltage harmonics test. (a) Grid voltage waveforms; (b) estimated grid frequency; (c) phase angle error.

4.2.4. Frequency Ramp and Step Change

The response of the selected algorithms on +100 Hz/s frequency ramp change can be observed through Figure 14a–c. Concerning the frequency estimation, SRF- and MAF-PLL had no steady-state tracking errors. QT1-PLL had a steady-state error of 1.09 Hz, while RCE-PLL had a steady-state error of 0.57 Hz. During this frequency ramp change, MAF-PLL exhibited the most significant phase angle error. SRF- and QT1-PLL had a phase angle error of 2.28° and 1.93°, while RCE-PLL had a steady-state phase tracking error of 0.5°.

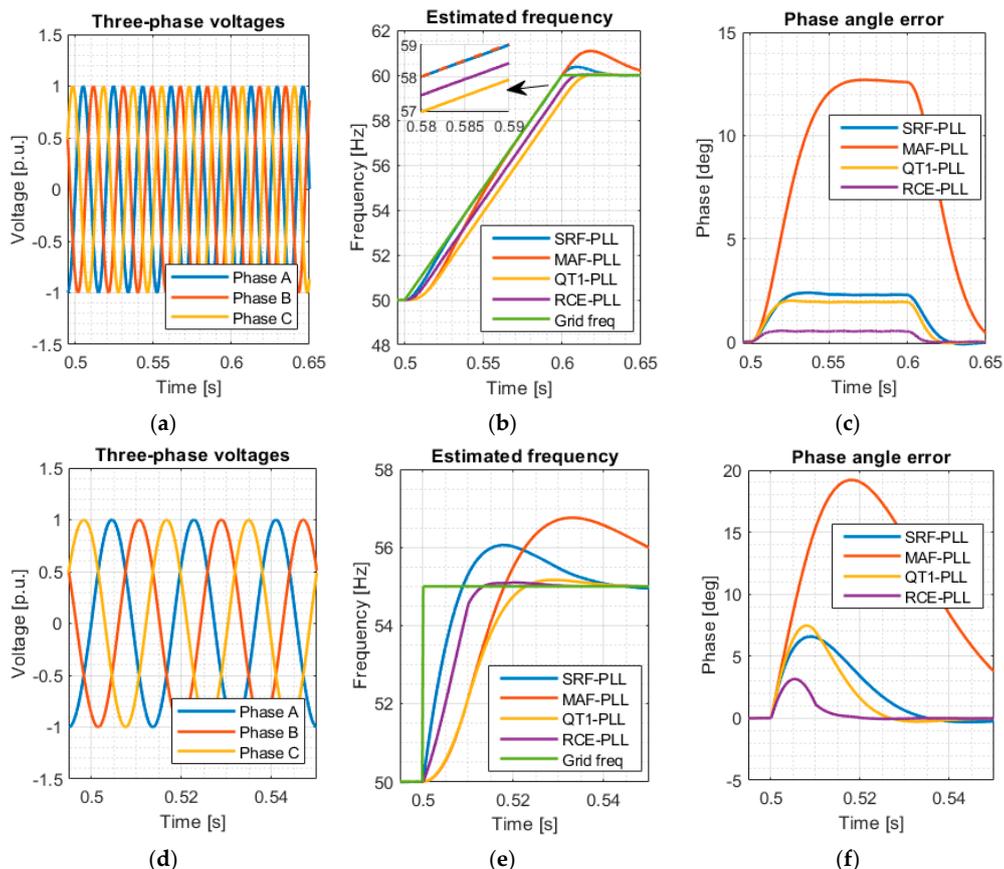


Figure 14. Grid frequency change test (a–c): +100 Hz/s ramp change; (d–f): Frequency step change to 55 Hz. (a) Grid voltage waveforms; (b) estimated grid frequency; (c) phase angle error; (d) grid voltage waveforms; (e) estimated grid frequency; (f) phase angle error.

The next conducted test was an abrupt frequency change from 50 Hz to 55 Hz. The grid voltage waveform during this test, along with the estimated frequency and phase angle error, are displayed in Figure 14d–f. RCE-PLL had the shortest frequency lock time of 20 ms, followed by QT1-PLL with the time of 35 ms, SRF-PLL with 39 ms, and MAF-PLL, which took 74 ms. Concerning the phase angle, the tested algorithms required 11 ms, 22.5 ms, 29 ms, and 62 ms, respectively.

4.3. Steady-State Behavior of Selected Algorithms

4.3.1. Voltage Sag with Grid Frequency Variation

Fundamental grid frequency can deviate from the nominal during grid operation and it is of interest to demonstrate the effectiveness of all algorithms in suppressing steady-state oscillations with fundamental frequency variation. For the parameters of voltage sag presented in Section 4.2.2, the amplitude of the undamped frequency and phase angle oscillations can be seen in Figure 15a,b, respectively. Frequency drift of up to ± 1 Hz had little effect on the disturbance attenuation capabilities of SRF-PLL. As expected, RC based RCE-PLL showed the biggest susceptibility to fundamental frequency variation. In order for the RCE-PLL estimated frequency to stay in the ± 0.1 Hz band, the maximum drift of the fundamental frequency has to be in the -0.4 Hz– $+0.35$ Hz range. The other tested algorithms fulfilled the settling band criterion on the tested frequency deviation. Concerning the phase angle in the tested deviation band, none of the tested algorithms had a settling problem.

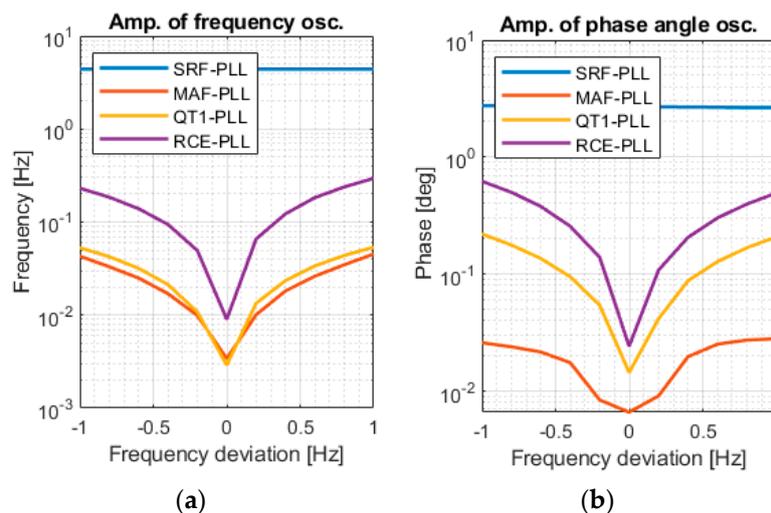


Figure 15. Effect of fundamental frequency deviation on the amplitude of undamped oscillations during voltage sag. (a) Frequency; (b) phase angle.

4.3.2. Voltage Harmonics with Grid Frequency Variation

Selected algorithms were subjected to harmonic polluted voltages as defined in Section 4.2.3. The amplitude of their estimated frequency and phase angle oscillations as a function of fundamental frequency change is shown in Figure 16a,b, respectively. For both the frequency and phase angle estimation, the frequency drift did not have a significant influence on SRF-PLL filtering capabilities. The impact of frequency deviation on the RCE-PLL was higher than in the previous test, as expected. When the fundamental frequency deviates from the nominal value, harmonic bound to fundamental frequency deviate from the expected frequency of occurrence that times more as the order of harmonic. For this test, RCE-PLL will settle inside the defined band if the fundamental frequency stays in the -0.25 Hz– $+0.17$ Hz range for frequency settling and -0.55 Hz to $+1$ Hz for the phase angle settling. MAF- and QT1-PLL had no settling band problem for a frequency deviation in the tested region.

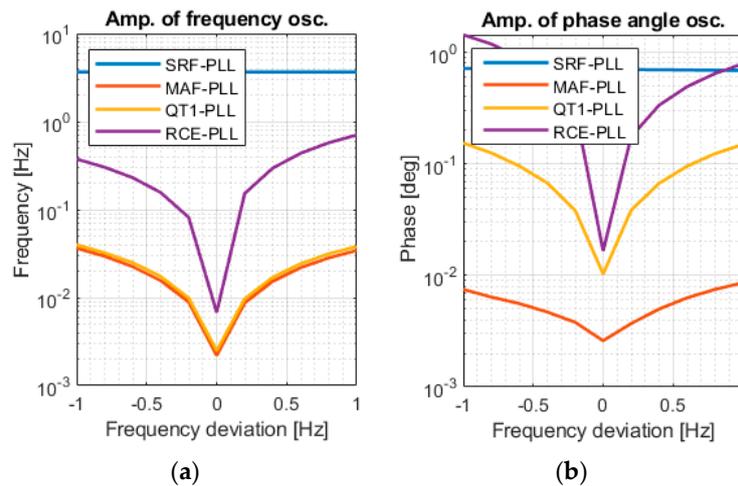


Figure 16. Effect of fundamental frequency deviation on the amplitude of undamped oscillations during voltage harmonics. (a) Frequency; (b) phase angle.

4.3.3. DC Offset

The synchronization algorithm, in general, has to cope with the DC offset or noise in the measured voltage waveform. All algorithms were tested on up to 2% DC offset in phase A. Neither the MAF-, QT1-, or RCE-PLL filters were designed with appropriate delays that suppressed the DC offset oscillations. The amplitude of the undamped oscillations in the frequency estimation is shown in Figure 17a, and the phase angle estimation in Figure 17b. Only a 0.5% DC component is required to make the RCE- and SRF-PLL ineligible for frequency estimation. QT1- and MAF-PLL were more resilient, requiring 1.3% and 1.5% of DC offset for frequency estimation oscillations to leave a defined frequency band. Only RCE-PLL had a problem with the phase angle estimation when a 1.8% DC offset was present.

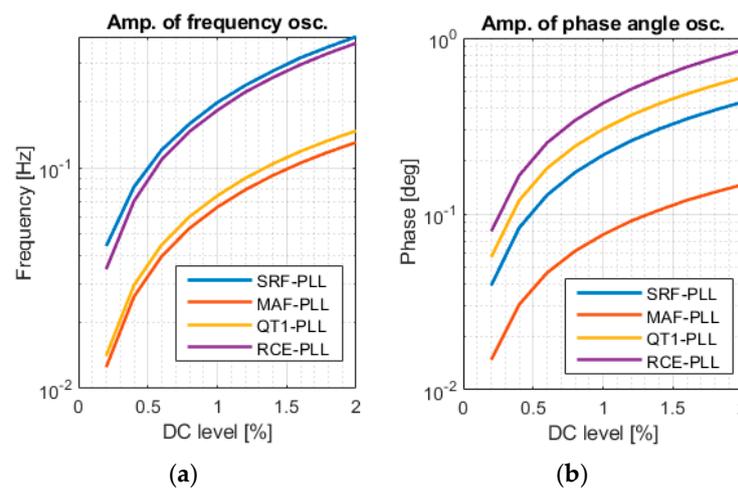


Figure 17. Effect of DC offset in phase A on the amplitude of undamped oscillations. (a) Frequency; (b) phase angle.

4.3.4. Measured Noise

For the noise test, all three phases were polluted with random noise evenly distributed over 10 kHz sampling frequency with a maximum amplitude of $\pm 2\%$. As a performance indicator, the standard deviation measurement was used. The standard deviation of each algorithm's frequency and phase angle estimation in the function of noise level can be observed in Figure 18a,b, respectively. Noise had an order of magnitude larger impact on SRF- and RCE-PLL than on MAF- and QT1-PLL in

the frequency estimation, due to the MAF in the control loop of the latter two. For the phase angle estimation, RCE-PLL had the smallest tolerance on measurement noise.

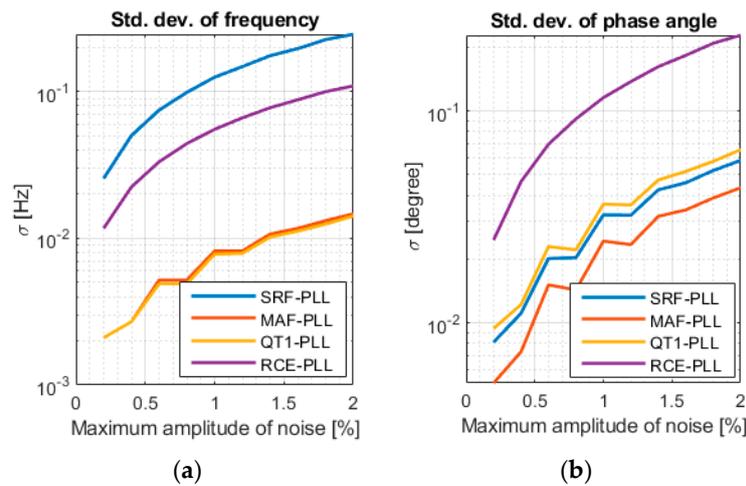


Figure 18. Effect of three-phase signal noise on parameters of interest. (a) Standard deviation of frequency; (b) standard deviation of phase angle.

4.4. Summary

A concise summary of the exhibited performances of the tested algorithms along with the comparison of implementation complexity, tuning complexity, and stability margins of each algorithm is presented in Table 4.

Table 4. Summary of results and implementation complexity.

Algorithm		SRF-PLL	MAF-PLL	QT1-PLL	RCE-PLL
Number of parameters to configure		2	3	2	4
Complexity of implementation		low	medium	medium	high
Phase margin (degree)		65	43.3	45.8	59.7
Phase jump +30°					
Settling time (cycles)	Frequency ¹	2.35	4.15	2.2	1.44
	Phase angle ²	1.9	3.6	1.45	1
Maximum overshoot	Frequency (Hz)	14	6.7	6.5	8.5
	Phase angle (degree)	30	30	30	20
Voltage sag, Type C depth 0.7					
Settling time (cycles)	Frequency ¹	-	1.6	1.25	0.98
	Phase angle ²	-	0.95	0.45	0.55
Susceptibility to frequency variation		low	low	medium	high
Voltage harmonics					
Settling time (cycles)	Frequency ¹	-	0.45	0.45	0.8
	Phase angle ²	0.25	0	0	0.5
Susceptibility to frequency variation		low	low	medium	high
Measurement disturbances					
Susceptibility to measurement disturbances		high	low	medium	high
Ramp frequency change					
Steady-state error	Frequency (Hz)	0	0	1.09	0.57
	Phase angle (degree)	2.28	12.7	1.93	0.5
Frequency step-change +5 Hz					
Settling time (cycles)	Frequency ¹	1.95	3.7	1.75	1
	Phase angle ²	1.45	3.1	1.1	0.55
Maximum overshoot	Frequency (Hz)	1.1	1.75	0.25	0.2
	Phase angle (degree)	6.5	19	7.5	3

¹ ±0.1 Hz band; ² ±0.8° band.

From the presented table, it can be concluded that of all the tested algorithms, SRF-PLL had the lowest implementation complexity and the biggest phase margin. It had the highest overshoot during the phase jump, and was the least suitable for phase and frequency estimation in the presence of voltage imbalance or harmonics when the grid frequency was equal to nominal. In general, for the estimated parameter settling, around two fundamental frequency cycles are required.

MAF-PLL had the lowest variation of estimated parameters when its input voltages contained disturbances, harmonics, or imbalance for the whole tested frequency range. Along with SRF-PLL, it can track fundamental frequency ramp changes without a steady-state error. The drawbacks are the slow settling time and significant phase angle error in the transient after a fundamental frequency change.

QT1-PLL offers faster phase angle jump synchronization than MAF-PLL. In terms of the influence of frequency variation, DC offset or noise on the estimated frequency shares the MAF-PLL's small susceptibility to these disturbances. The estimated phase angle with QT1-PLL had about an order of magnitude higher oscillations than in the case of MAF-PLL, which was noted with frequency deviation, but for a tested range of variation, the oscillations were inside the defined settling band.

RCE-PLL had the highest implementation complexity and the highest number of parameters for setup. Its phase margin was around 60° , second only to SRF-PLL. The RCE-PLL phase angle estimation was the most susceptible to measurement disturbances and significant frequency variation; in the presence of harmonics, it could create oscillations worse than SRF-PLL. The same frequency deviation can cause estimated frequency oscillations that are almost an order of magnitude higher than MAF-PLL. Concerning the settling time, it provided an improvement over QT1-PLL in almost all tests, proving unfit for all voltage parameter estimations for no more than 25 ms only in the case of phase jump.

5. Conclusions

A new synchronization algorithm RCE-PLL that uses RC and SRF-PLL was proposed in this paper. RCE-PLL presents an improvement over QT1-PLL in most conducted tests in terms of settling time, since the grid voltage parameter estimation inside the ± 0.1 Hz band for frequency and $\pm 0.8^\circ$ band for phase angle can be done usually for no more than one period. For the parameter configuration that enables this settling time, the phase margin of RCE-PLL was higher when compared to MAF- or QT1-PLL. The online compensation term in RCE-PLL enables instant compensation of part of the phase angle error. Furthermore, RCE-PLL is insensitive to the change of grid voltage amplitude.

The drawback of the proposed structure is a significant deterioration of its filtering capabilities when fundamental frequency differs from the nominal, implying that necessary future improvement lies in a frequency adaptive RC in RCE-PLL. The instantaneous phase jump feature requires further examination, with the eventual goal of compensating the complete phase jump when it occurs.

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Conflicts of Interest: The authors declare no conflicts of interest.

Acronyms and Symbols

RES	Renewable Energy Sources
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Arrays
FGVVA	Fundamental Grid Voltage Vector Phase Angle
FGVVF	Fundamental Grid Voltage Vector Frequency
PLL	Phase-Locked Loop
PCC	Point of Common Coupling
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop

DDSRF-PLL	Decoupled Double SRF-PLL
MAF	Moving Average Filter
MAF-PLL	Moving Average Filter based SRF-PLL
QT1-PLL	Quasi-Type 1 PLL
SOGI	Second-Order Generalized Integrator
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PR	Proportional-Resonant
LF	Loop Filter
PD	Phase Detector
VCO	Voltage-Controlled Oscillator
LPF	Low Pass Filter
BPF	Band Pass Filter
RC	Repetitive Control
RCF	Repetitive Control Filter
RCE-PLL	Repetitive Control Enhanced SRF-PLL
h	Order of harmonic
V_{abc}	Voltages in natural reference frame (abc)
$V_{\alpha\beta}$	Voltages in the stationary reference frame ($\alpha\beta$)
V_{dq}	Voltages in the synchronous reference frame (dq)
$V_{abc,dc}$	DC voltage in natural reference frame
$V_{\alpha\beta,dc}$	Voltage components in stationary reference frame that are consequence of DC voltages in natural reference frame
$V_{dq,osc}$	Voltage components in synchronous reference frame that are consequence of DC voltages in natural reference frame
V_h^\pm	Voltage amplitude of h -th positive (+) or negative (-) sequence harmonic
ω	Fundamental frequency
ϕ_h^\pm	Initial phase angle of h -th positive (+) or negative (-) sequence harmonic
θ_h^\pm	Phase angle of h -th positive (+) or negative (-) sequence harmonic
$\hat{\theta}$	Instantaneous phase angle of the synchronous reference frame vector
θ_1^+	Positive fundamental grid voltage vector phase angle
$\hat{\theta}_1^+$	Estimated angle of the positive fundamental grid voltage vector
p	Laplace complex variable
ω_n	Natural frequency
ζ	Damping ratio
k_p	Proportional gain
T_i	Integral time constant
K	Gain of repetitive controller
T	Delay time of repetitive controller
T_s	Sampling time
N	Closest integer ratio between delay time T and sampling period T_s
ω_{ff}	Expected fundamental frequency
$\Delta\omega$	Fundamental frequency correction signal
$e(p)$	Error signal
$\bar{e}(p)$	Filtered error signal
$D(p)$	Model of disturbances due to oscillating terms in Laplace domain

Appendix A

The following MATLAB .m function presents a RCF implementation suitable for dSpace ds1103.

```

function out = fcn(in, K, N)
%{

Implementation of Repetitive Control Filter

Part of File      : RCE-PLL
Author           : Filip Filipović
Date            : June '19

Description:
Inputs
-      in      - obtained sample,          type: double
-      K      - value of coefficient K,     type: double
-      N      - number of delays,         type: int16

Output
-      out     - filtered sample,          type: double

Inside function persistent variables
-      inputs  - array of previously obtained samples
                                     type: array<double>
-      outputs - array of previously generated outputs
                                     type: array<double>
%}

% Define variables that have persistent values
persistent inputs outputs;
if(isempty(inputs))
    inputs = zeros(1, 150);    %150 is the maximum number of delays. Change
    outputs = zeros(1, 150); %this number if required.
end

% Obtaining input(output) value from N-steps ago
delay_in = inputs(N);
delay_out = outputs(N);
% Calculation of the output
out = 1/(1+K) * (in - delay_in + delay_out);
% Latest samples are inserted in array to be used in next iteration
inputs = [in, inputs(1:end-1)];
outputs = [out, outputs(1:end-1)];

```

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