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A Three-Level DC-Link Quasi-Switch Boost T-Type Inverter with Voltage Stress Reduction

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Abstract: In recent years, the three-level T-Type inverter has been considered the best choice for many low and medium power applications. Nevertheless, this topology is known as a buck converter. Therefore, in this paper, a new topology incorporating the dc-link type quasi-switched boost network with the traditional three-level T-type inverter is proposed to overcome the limit of traditional three-level T-Type inverter. The space vector pulse width modulation scheme is considered to control this topology, which provides some benefits such as enhancing modulation index and reducing the magnitude of common-mode voltage. For this scheme, the zero, medium, and large vectors are utilized to generate the output voltage. The shoot-through state which is adopted by turning on all power switches of inverter leg is inserted into zero vector to boost the dc-link voltage. As a result, there is no distortion at the output waveform. The control signal of intermediate network power switches is also detailed to improve the boost factor and voltage gain. As a result, the voltage stress on power devices like capacitors, diodes, and switches is decreased significantly. To demonstrate the outstanding of proposed structure and its control strategy, some comparisons between the proposed method and other ones are performed. Simulation and experimental prototype results are conducted to verify the accuracy of the theory and effectiveness of the inverter.

Keywords: quasi-switched boost inverter; three-level T-type inverter; shoot-through; three-level inverter; intermediate network; dc-link type; common-mode voltage

1. Introduction

Recently, the multilevel inverters (MIs) have been widely used for industrial applications due to their advantages such as better output voltage quality, smaller low-pass filter size requirement, and the lower voltage stress on switching devices compared to the two-level inverters [1,2]. There are three basic topologies of MIs which are neutral point clamped (NPC) inverter, cascade, and flying capacitor (FC) inverter. Nevertheless, these topologies use plenty passive components such as diodes for NPC structure, capacitors for FC configuration, or isolate dc input sources for cascade form of the inverter. Thus, these configurations produce high system size, cost, and power loss, which are not suitable for low and medium voltage applications [1–3]. For that reason, the three-level T-type inverter (3L-T^{2}I) was explored to replace conventional MIs to provide superior in low and medium voltage applications [1–3]. These topologies have both particular advantages and disadvantages, but the same drawback of these is inability to operate under shoot-through (ST) condition which is generated when all switches in any phase leg are triggered on simultaneously. Besides, traditional topologies behave as a buck converter which produce output voltage where the peak-peak value is smaller than the dc-link voltage.

To overcome these limits, the inverter based on Z-source (ZS) topology was explored in [4]. By using one more diode, two additional inductors, and two additional capacitors, this topology is known as a single-state converter with a buck-boost capability and ST immunity. This topology operates in two main modes which are non-shoot-through (NST) mode and ST mode. The ST mode is used to boost the dc-link voltage from the constant input power source to achieve the desire ac output voltage at the load. By using ST mode which is achieved by switching all switches in the inverter leg, this topology can solve the ST problem, which causes the short-circuit phenomenon in conventional inverters, without incorporating the dead-time in the control signals of switches before feeding to switches, so the output distortion can be avoided. Due to the benefits of ZS topology, it is widely applied to photovoltaic (PV) systems [5], uninterruptable power supply (UPS) systems [6], and motor drives, etc. In [7–12] the authors explored the combination between the ZS network and the conventional 3L-T^{2}I as well as 3L-NPCI topologies. In these studies, to create a three-level voltage at the output of the intermediate network, two capacitors were used to split the dc input power supply. As a result, two output terminals of the ZS network and the mid-point of input power source generate a three-level voltage feeding to the inverter leg. This topology inherits all advantages of MIs as well as the buck-boost capability and ST immunity of the ZS network. The ZS network uses an input diode to connect the input power source to the intermediate network, which causes discontinuous input current, thus it generates stress on the input power source. This drawback makes it difficult to apply to the PV system. Moreover, another disadvantage of this topology is the large stress on ZS network components.

In [13–18] a novel type of impedance network called quasi-Z-source (qZS) was proposed to overcome the limitations of the ZS network. In this topology, the input current is continuous and voltage stress on capacitors is reduced, significantly. To inherit the outstanding advantages of MIs, a combination of the qZS network with 3L-T^{2}I was discussed in [2,19–25]. These studies connected two identical qZS networks in cascade form to produce a three-level voltage at the output terminal. Therefore, it improves the quality of output voltage. However, it also leads to increase of the number of passive components such as capacitors and inductors. As a result, the weight, size, and cost of the system are increased significantly. On the other hand, the qZS network is not flexible to control because the boost factor just depends on the ST duty ratio of inverter leg which is limited by $(1 - m)$, where m is the modulation index.

With one more active switch, the quasi-switch boost (qSB) network saves one inductor and one capacitor compared to the qZS topology whereas the boost factor is maintained [26]. In this study, the single-phase three-level H-bridge was considered to incorporate with the qSB network. However, the inductor current ripple of this structure is quite large. The authors of [27] presented a pulse width modulation (PWM) scheme based on phase shift carrier method to reduce the inductor current ripple and enhance the boost factor of the converter. In [28–32], a combination of the 3L-T^{2}I with the qSB network was discussed. In these studies, two identical qSB networks were connected in cascade form with one inductor less to create a three-level voltage at output load voltage. Moreover, a PWM strategy to reduce the inductor current ripple as well as enhancing the boost factor of the converter was also presented. In [28–32], the boost factor is very flexible to control because of using an additional duty cycle of intermediate switches. Therefore, unlike other impedance-source networks, this topology can operate with a large input power source range without affecting the modulation index of the inverter. To inherit the benefits of the PWM scheme discussed in [28], a PWM strategy was proposed in [29] to enhance the stabilization of the system by solving the open-circuit faults of switching devices in the inverter leg as well as the intermediate network. In [30], the negative effect of common-mode voltage (CMV) generated in the three-level qSB T-type inverter is minimized by applying the proposed space-vector modulation technique. The studies in [31,32] presented space vector pulse width modulation (SVP) schemes to reduce the total harmonic distortion (THD) value of output voltage. Furthermore, the PWM control method of [32] also reduced the magnitude of CMV without affecting the quality of output voltage.

In [33,34], a new topology of the qSB network known as the dc-link type of the qSB (DqSB) was discussed. This topology with the modified PWM control method reduced the stress on the capacitor as well as enhancing the voltage gain. As a result, the stress on power devices of the intermediate network was decreased significantly. Similar to [28–32], in [33,34], two coefficients were used to control the boost factor of the converter. Therefore, this topology is also flexible to control and enables operation under a large input voltage range.

In this paper, a combination of the DqSB network with 3L-T^{2}I is introduced. The PWM strategy is based on the SVP which uses zero vector, medium vectors, and large vectors to generate a reference vector that provides CMV reduction capability. The operation principle and theory analysis are also detailed in this paper. The advantages of this configuration are demonstrated by comparing it to other topologies and schemes. The simulation and experimental results are shown to validate the effectiveness of the proposed structure. The advantages of the proposed three-level DC-link type quasi switch boost T-type inverter (3L-DqSBT^{2}I) scheme over the conventional three-level quasi switch boost T-type inverter (3L-qSBT^{2}I) scheme are as follows:

- The boost factor and voltage gain are improved compared to the conventional 3L-qSBT^{2}I.
- The modulation index is increased by adopting SVP technique.
- The voltage stress on power devices like capacitors, diodes, and switches is decreased significantly.
- The magnitude of CMV is reduced compared to the conventional 3L-qSBT^{2}I.

The rest of this paper is divided into four parts. Section 2 shows the introduced topology with its PWM control strategy. Section 3 presents the comparison of the proposed structure to others to demonstrate the effectiveness of introduced topology. Section 4 presents the simulation and experimental results to verify the accuracy of the introduced structure. Section 5 shows the summary of this paper.

2. Three-Level DC-Link Type Quasi-Switched Boost T-Type Inverter Topology

The 3L-DqSBT^{2}I topology consists of an intermediate network and an inverter leg. The DqSB network is used to connect the input voltage with the 3L-T^{2}I structure to boost the dc-link voltage, as illustrated in Figure 1. The input power supply is split into two equal sources. Each source feeds to an identical DqSB network, which consists of one inductor, one capacitor, two diodes, and one active switch. The 3L-T^{2}I topology is the same as conventional MIs topology which can generate a three-level voltage at output terminal which are $+V_{PN}/2$, *zero*, and $-V_{PN}/2$ which correspond to "P" state, "O" state, and "N" state, respectively, where V_{PN} is the dc-link voltage of the inverter. The output of the inverter feeds to the three-phase resistor load through a three-phase low pass filter (LC filter) to improve the quality of output load voltage as well as the output load current.

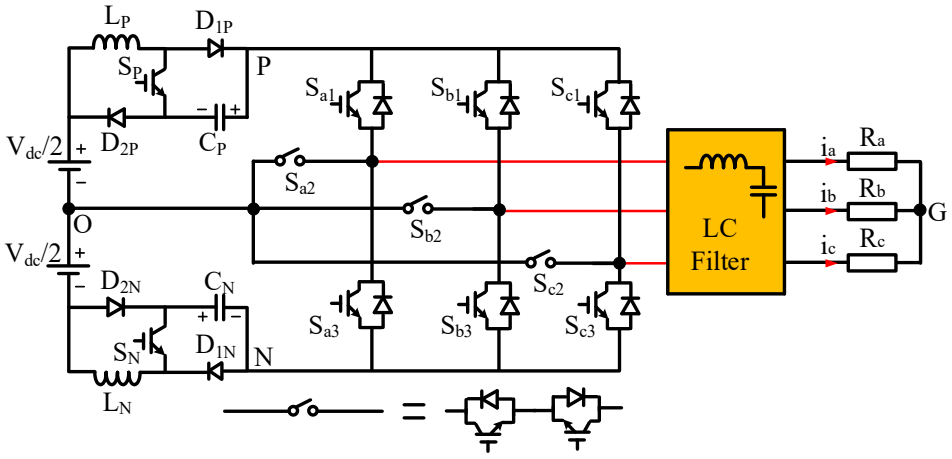

Figure 1. Three-level DC-link type quasi switch boost T-type inverter (3L-DqSBT^{2}I) topology.

2.1. Operating Principles

Similar to other single-state inverter topologies, this structure also operates under two main modes which are NST and ST modes. In NST mode, the 3L-T^{2}I circuit can produce a three-level voltage at the output terminal by triggering corresponding switches as shown in Table 1. When S_{x1} is switched on, the output voltage is achieved $+V_{PN}/2$ which is the half of dc-link voltage generated by the DqSB network. While the output voltage obtains $-V_{PN}/2$ when S_{x3} is turned on. The zero value is produced at output voltage when S_{x2} is triggered on. The NST mode consists of two sub-modes which are NST 1 and NST 2, as presented in Figure 2. The ST mode is achieved when all switches in the inverter leg are triggered on, as a result, the output load voltage in this time interval is zero. Therefore, in order to decrease the waveform distortion at the output, the ST signal is inserted within the time interval when the output voltage is *zero*.

Table 1. Switching states of 3L-DqSBT^{2}I ($x = a, b, c$).

Mode	ON Switches	ON Diodes	V_x
NST 1	S_P, S_N	D_{2P}, D_{2N}	$+V_{PN}/2$, 0 or $-V_{PN}/2$
NST 2	S_{x1} or S_{x2} or S_{x3}	D_{1P}, D_{1N}, D_{2P}, D_{2N}	$+V_{PN}/2$, 0 or $-V_{PN}/2$
ST	S_{x1}, S_{x2}, S_{x3}	D_{1P}, D_{1N}	0

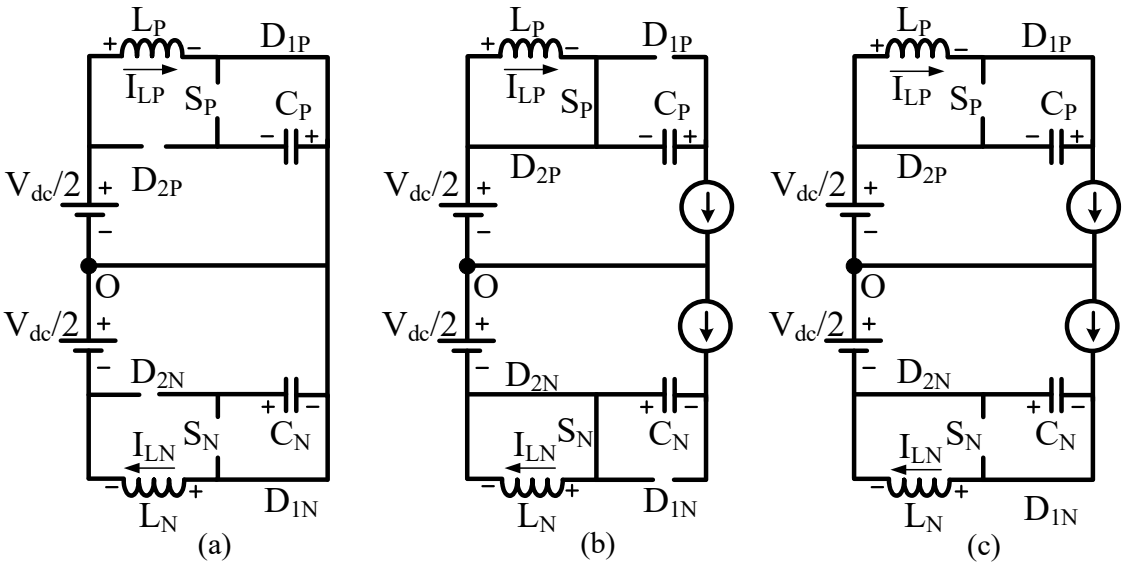

Figure 2. Modes of 3L-DqSBT^{2}I: (**a**) shoot-through (ST), (**b**) non-shoot-through (NST) 1, (**c**) NST 2.

In NST 1 as shown in Figure 2b, the switches S_P and S_N are triggered on. Therefore, the diode D_{1P} and D_{1N} are reversed bias whereas diode D_{2P} and D_{2N} are forward bias. The inductors L_P and L_N are short circuit by active switches and diodes D_{2P} and D_{2N} of the DqSB network. As a result, the current through two inductors is kept constant. The voltages across two inductors are expressed as:

$$V_{LP} = V_{LN} = 0 \tag{1}$$

In NST 2 as shown in Figure 2c, the switches S_P and S_N are triggered off, all diodes of the intermediate network are forward bias. As a result, the capacitors C_P and C_N are charged from L_P and L_N, respectively. The voltages of these inductors are calculated as:

$$\begin{cases} V_{LP} = -V_{CP} \\ V_{LN} = -V_{CN} \end{cases} \tag{2}$$

In ST mode, all switches of 3L-T^{2}I are turned on, simultaneously. As a result, the diodes D_{1P} and D_{1N} are forward bias whereas diodes D_{2P} and D_{2N} are reversed bias. The inductors L_P and L_N store energy from the input power source. The voltages of two inductors are expressed as:

$$V_{LP} = V_{LN} = V_{dc}/2 \tag{3}$$

2.2. SVP Scheme to Reduce CMV

In [2,30,32] the authors figured out that the CMV causes some problems in power systems such as electromagnetic interference or bearing current and shaft voltage, etc. Thus, CMV reduction is necessary to enhance the reliability of the system. The CMV generated by the inverter is identified as:

$$V_{CMV} = V_{GO} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \tag{4}$$

where V_{AO}, V_{BO}, and V_{CO} are three-phase output pole voltage.

Based on Equation (4), the magnitude of CMV can be limited from $-V_{PN}/6$ to $+V_{PN}/6$ by using only zero vector, medium vectors, and large vectors to synthesize the reference vector during operation of the inverter [2,32]. Thus, the space vector diagram of the three-level inverter is divided into 12 sectors to analyze the operation of the converter, as shown in Figure 3.

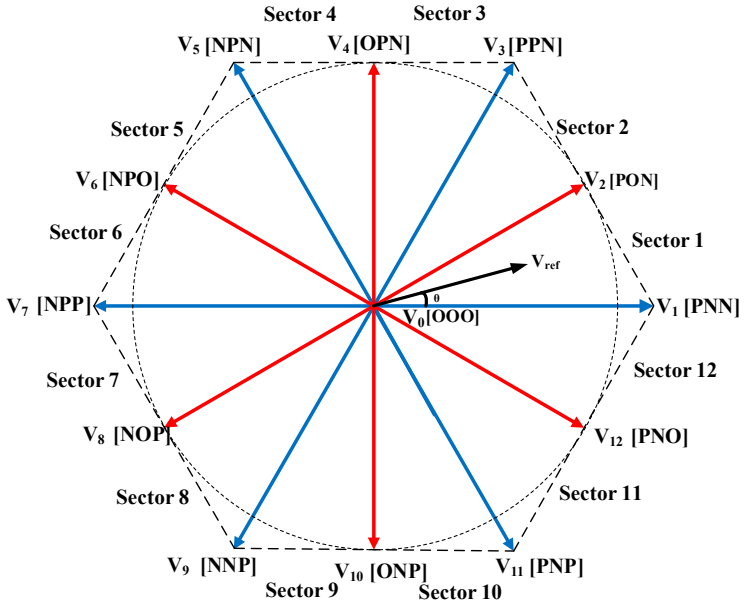

Figure 3. Space vector diagram to reduce common-mode voltage (CMV) for 3L-DqSBT^{2}I.

In general, assuming that the reference vector ($\vec{V}_{ref}$) is located in sector 1 or sector 2, the $\vec{V}_{ref}$ is synthesized as follows:

Case 1: When the $\vec{V}_{ref}$ is located in sector 1, the $\vec{V}_0$, $\vec{V}_1$, and $\vec{V}_2$ are adopted to generate the $\vec{V}_{ref}$. Thus, the relationship between these vectors can be expressed as:

$$\begin{cases} \vec{V}_{ref} \cdot T = \vec{V}_0 \cdot T_Z + \vec{V}_1 \cdot T_L + \vec{V}_2 \cdot T_M \\ T = T_Z + T_M + T_L \end{cases} \tag{5}$$

where,

(1) $\vec{V}_{ref}$—reference vector,

(2) $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_2$—zero vector, large vector, and medium vector, respectively,

(3) T—switching period of the inverter,

(4) T_Z, T_M, T_L—the on-times of $\vec{V}_0$, $\vec{V}_2$, and $\vec{V}_1$, respectively.

Similar to [2], the drew-time of each vector can be expressed as:

$$\begin{cases} T_M = 2mT\sin(\theta) \\ T_L = \sqrt{3}mT\sin(\pi/6-\theta) \\ T_Z = T - T_M - T_L \end{cases} \quad (6)$$

Case 2: Similar to sector 1, for sector 2, the $\vec{V}_{ref}$ can be expressed as:

$$\begin{cases} \vec{V}_{ref}\cdot T = \vec{V}_0\cdot T_Z + \vec{V}_3\cdot T_L + \vec{V}_2\cdot T_M \\ T = T_Z + T_M + T_L \end{cases} \quad (7)$$

The drew-time of $\vec{V}_0$, $\vec{V}_2$, and $\vec{V}_3$ can be identified as [2]:

$$\begin{cases} T_M = 2mT\sin(\pi/3-\theta) \\ T_L = \sqrt{3}mT\sin(\theta-\pi/6) \\ T_Z = T - T_M - T_L \end{cases} \quad (8)$$

Not similar to the study of [2] which only used the ST signal to boost the dc-link voltage, this topology also uses the active switches of the DqSB network to enhance the dc source. Thus, the switching sequence for sector 1 and sector 2, the ST insertion, and the control signal of DqSB's switches are reselected, as shown in Figure 4.

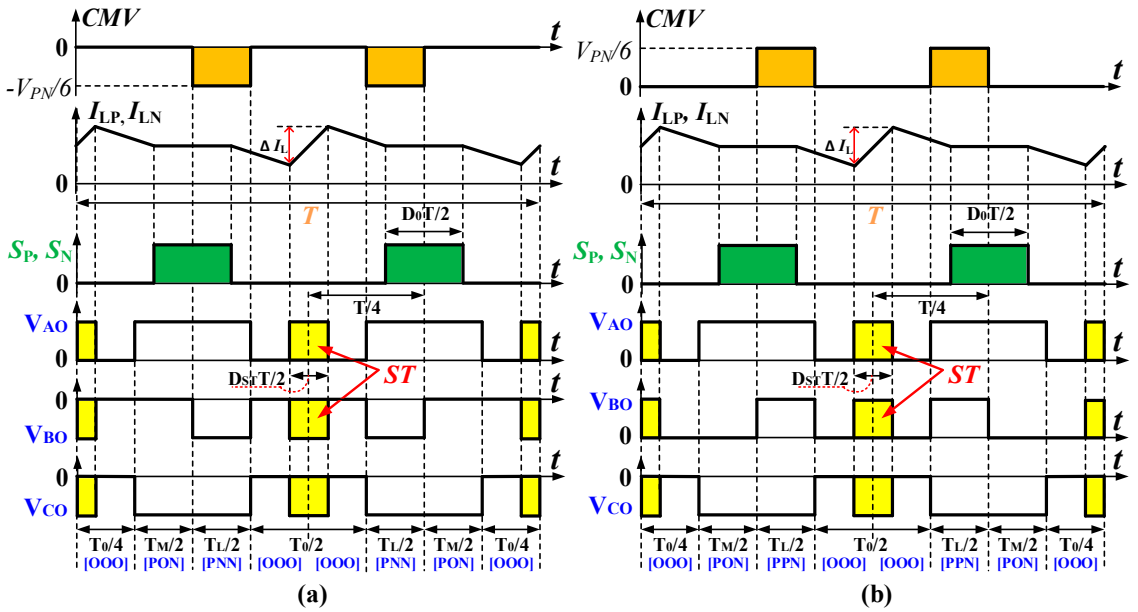

Figure 4. Switching sequence and ST insertion for (**a**) sector 1 and (**b**) sector 2.

By applying this way to other sectors, the drew-time of each vector as well as the switching sequence can be easily identified.

2.3. Steady-State Analysis

In one period of switching (T), the time interval of ST state is (D_{ST}·T), while (D_0·T) is the time interval of NST 1. Therefore, the value $(1 - D_{ST} - D_0)T$ is the time interval of NST 2. Applying the

volt-second balance for two inductors L_P and L_N with the note that ($V_{CP} = V_{CN} = V_C$), the voltages across these capacitors can be calculated as:

$$V_C = V_{CP} = V_{CN} = \frac{1}{2} \cdot \frac{D_{ST}}{1 - D_0 - D_{ST}} V_{dc} \tag{9}$$

The inductor current ripple is calculated as:

$$\begin{cases} \Delta I_{LP} = \frac{V_{dc} \cdot D_{ST}}{4 \cdot L_P \cdot f} \\ \Delta I_{LN} = \frac{V_{dc} \cdot D_{ST}}{4 \cdot L_N \cdot f} \end{cases} \tag{10}$$

where,

(1) ΔI_{LP}, ΔI_{LN}—inductor current ripples of L_P and L_N, respectively,
(2) f—switching frequency of the inverter,
(3) D_{ST}—ST duty ratio,
(4) D_0—duty cycle of S_P and S_N.

The peak value of dc-link voltage (V_{PN}) is the sum of two capacitors voltage and the dc input source, which is identified as:

$$V_{PN} = V_{dc} + 2 \cdot V_C = \frac{1 - D_0}{1 - D_0 - D_{ST}} V_{dc} \tag{11}$$

Based on Equation (11) the boost factor (B) can be calculated as:

$$B = \frac{V_{PN}}{V_{dc}} = \frac{1 - D_0}{1 - D_0 - D_{ST}} \tag{12}$$

The peak value of first harmonic of output phase voltage ($V_{x,peak}$) can be identified as:

$$V_{x,peak} = m \cdot \frac{2}{\sqrt{3}} \cdot \frac{V_{PN}}{2} = \frac{m}{\sqrt{3}} \cdot \frac{1 - D_0}{1 - D_0 - D_{ST}} V_{dc} \tag{13}$$

The voltage gain (G) of the converter is expressed as:

$$G = \frac{V_{x,peak}}{V_{dc}} = \frac{m}{\sqrt{3}} \cdot \frac{1 - D_0}{1 - D_0 - D_{ST}} \tag{14}$$

The relationship between modulation index, the ST duty ratio, and the duty cycle of DqSB's switches are illustrated as:

$$\begin{cases} 0 \le m \le 1 \\ m + D_{ST} \le 1 \\ D_{ST} + D_0 < 1 \end{cases} \tag{15}$$

3. Comparison to Other Configurations

To validate the accuracy of the proposed topology and its PWM control method, some investigations about boost factor, voltage gain, and voltage stress on power devices are conducted for the ZS inverter (ZSI) proposed in [8], the qZS inverter (qZSI) introduced in [2,19], the qSB inverter (qSBI) with two sources and two inductors proposed in [35], the qSBI with reducing number of sources and inductors in [36], and the proposed 3L-DqSBT^{2}I.

Table 2 presents the overall comparison between 3L-DqSBT^{2}I and other topologies. It can be seen that the qZSI uses the largest number of passive components (four inductors and four capacitors), while the ZSI, the qSBI in [35], and the 3L-DqSBT^{2}I save two inductors and two capacitors compared to the qZSI. The qSB in [36] uses the smallest number of passive components for the intermediate network

which just has one inductor and two capacitors. While, the diode and active switch of the qSBI and the 3L-DqSBT^{2}I are used more than the ZSI and qZSI. Two active switches and four diodes are used for both the qSBI and the 3L-DqSBT^{2}I, while the ZSI and qZSI just use two diodes, as shown in Table 2.

Table 2. Comparison between 3L-DqSBT^{2}I with other configurations and PWM methods.

	ZSI in [8]	qZSI with PWM in [19]	qZSI with PWM in [2]	qSBI with PWM in [34]	qSBI with PWM in [35]	Proposed 3L-DqSBT^{2}I
Boost factor, B	$1/(1-2D_{ST})$	$1/(1-2D_{ST})$	$1/(1-2D_{ST})$	$1/(1-2D_{ST})$	$1/(1-2D_{ST})$	$(1-D_0)/(1-D_0-D_{ST})$
Voltage gain, G	$m{\cdot}B/\sqrt{3}$	$m{\cdot}B/2$	$m{\cdot}B/\sqrt{3}$	$m{\cdot}B/2$	$m{\cdot}B/2$	$m{\cdot}B/\sqrt{3}$
Capacitor voltage stress, V_c/V_{dc}	$(1-D_{ST})B$	$D_{ST}{\cdot}B/2$, $(1-D_{ST})B/2$	$D_{ST}{\cdot}B/2$, $(1-D_{ST})B/2$	$B/2$	$B/2$	$0.5{\cdot}D_{ST}/(1-D_0-D_{ST})$
Diode voltage stress, V_D/V_{dc}	B	$B/2$	$B/2$	$B/2$	$B/2$	$0.5{\cdot}D_{ST}/(1-D_0-D_{ST})$, $B/2$
Switch voltage stress, V_S/V_{dc}	NA	NA	NA	$B/2$	$B/2$	$0.5{\cdot}D_{ST}/(1-D_0-D_{ST})$
Inductors	2	4	4	2	1	2
Capacitors	2	4	4	2	2	2
Diodes	2	2	2	4	4	4
Switches	NA	NA	NA	2	2	2
Input current ripple	Very high	Small	Small	Small	Small	High

Figure 5 shows the investigations about boost factor versus ST duty ratio and the voltage gain versus modulation index for these topologies and PWM methods, and it is noted that the modulation index is set to $(1-D_{ST})$ to achieve the highest voltage gain for each scheme. As illustrated in Figure 5a, the boost factor of the 3L-DqSBT^{2}I depends on two coefficients which are the duty cycle of the DqSB network's active switches (D_0) and the ST duty ratio (D_{ST}). With the increase of D_0, the boost factor of the 3L-DqSBT^{2}I is increased, whereas the boost factor of other topologies is just up to the D_{ST}. When the value 0.5 is applied to D_0, the 3L-DqSBT^{2}I produces the same boost factor to the other configurations. However, by applying the SVP method, the voltage gain of the ZSI in [8], and the qZSI in [2], the 3L-DqSBT^{2}I has the larger voltage gain which is $2/\sqrt{3}$ times larger than the others, as illustrated in Figure 5b. Similar to the boost factor versus the ST duty ratio, the 3L-DqSBT^{2}I just provides superior in voltage gain when $D_0 > 0.5$. For that reason, in this paper, the value 0.6 was selected for coefficient D_0 as an example to analyze the effectiveness of the proposed topology.

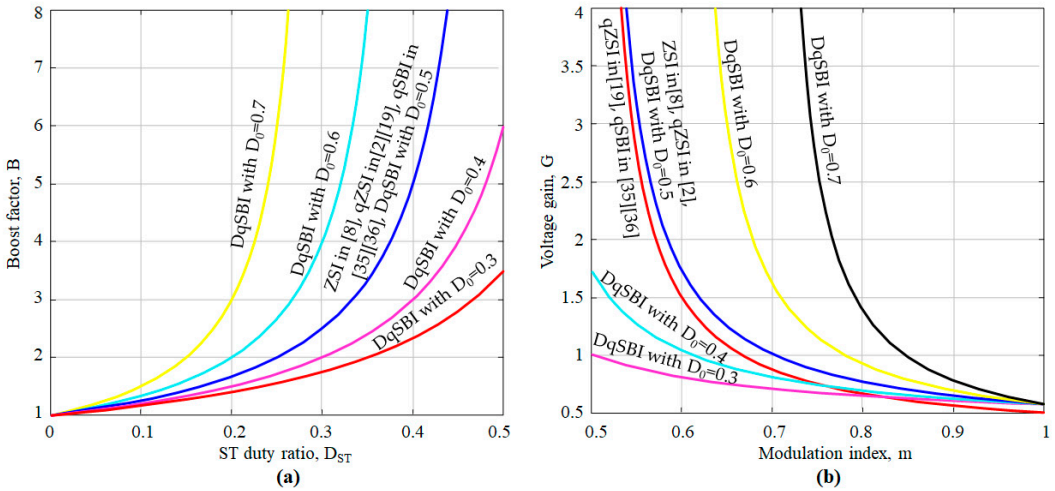

Figure 5. Investigation about (**a**) boost factor versus ST duty ratio and (**b**) voltage gain versus modulation index.

Figure 6 shows the investigations of voltage stress on power components such as capacitor voltage stress, diode voltage stress, and switch voltage stress with the note that there are four capacitors in the qZSI with unequal voltage stress on their, as shown in Table 2. Thus, this comparison was

conducted for each capacitor of the qZSI. Furthermore, the diode voltage stress of each diode of the qSBI and 3L-DqSBT^{2}I is also not equal to each other. Therefore, the investigation was also carried out for each diode. As presented in Figure 6a, the qZSI is superior in capacitor voltage stress for both methods in [2,19], while the qSBI produces higher voltage stress on the capacitor than the ZSI. In general, the proposed 3L-DqSBT^{2}I is better than the ZSI and qSBI. Moreover, in the range of low voltage gain, the 3L-DqSBT^{2}I is also better than the qZSI. Furthermore, all diodes of 3L-DqSBT^{2}I have less voltage stress compared to other configurations, as shown in Figure 6b. This figure also points out that the qZSI is better than ZSI about voltage stress on diodes with the same voltage gain value. As the impedance-source networks in [2,8,19] do not have any active switches, the ZSI and qZSI are not considered to investigate for switch voltage stress which is shown in Figure 6c. As the voltage stress of the active switch is equal to the capacitor voltage, the 3L-DqSBT^{2}I has less voltage stress on the switch than the qSBI.

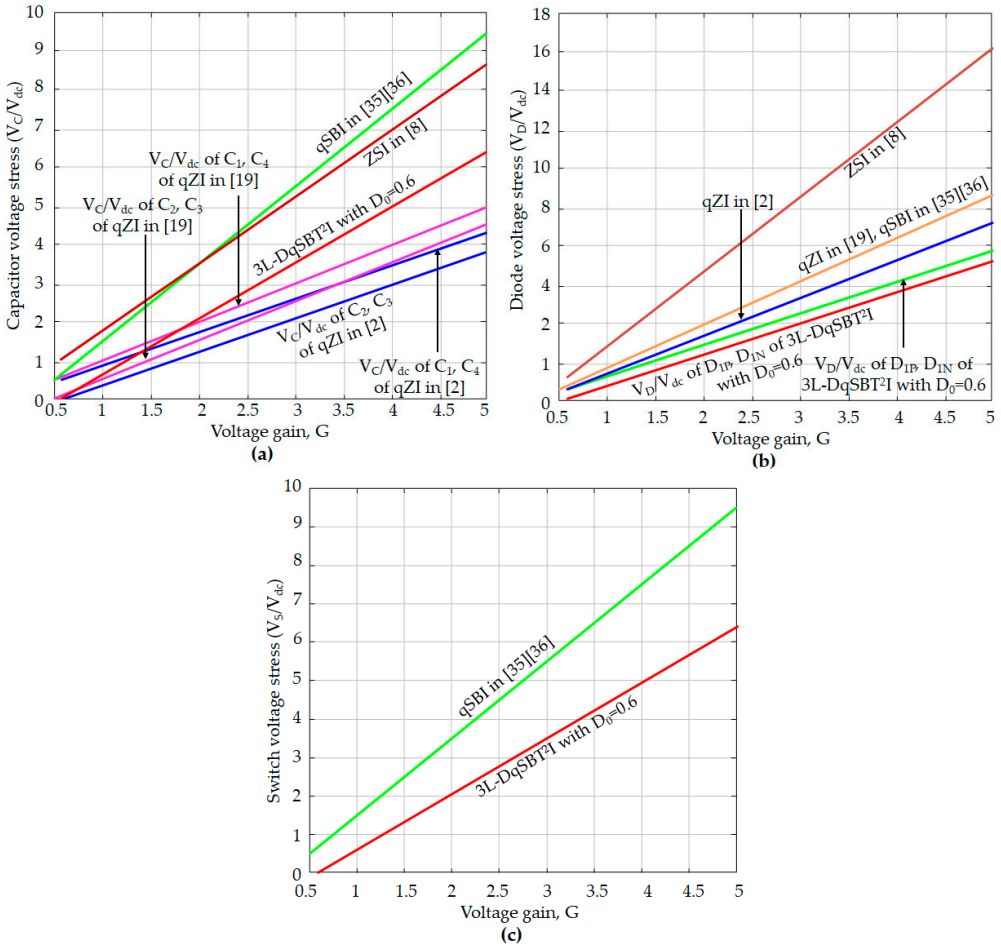

Figure 6. Investigation about (**a**) capacitor voltage stress versus voltage gain, (**b**) diode voltage stress versus voltage gain, and (**c**) switch voltage stress versus voltage gain.

4. Simulation and Experimental Results

4.1. Simulation Results

The accuracy of the proposed inverter was validated by simulation results with the help of PSIM software. The parameters used for simulation are listed in Table 3. Before feeding to three-phase resistor load, the three-phase low pass filter was used to mitigate the magnitude of high-frequency harmonics. To produce a root mean square (RMS) output phase voltage of 110 V from the input voltage of 200 V, the modulation index was 0.85. Thus, from Equation (15) the ST duty cycle must be 0.15.

Table 3. Simulation and experiment parameters.

Parameter/Components		Values
DC input voltage	V_{dc}	200 V
Output voltage	$V_{x,RMS}$	110 V_{RMS}
Output frequency	f_o	50 Hz
Carrier frequency	f_s	5 kHz
ST duty cycle	D_{ST}	0.15
Modulation index	m	0.85
Boost inductors	$L_P = L_N$	1 mH/20 A
Capacitors	$C_1 = C_2$	2200 µF/600 V
LC filter	L_f *and* C_f	3 mH and 10 µF
Diode	D_{1P}, D_{2P}, D_{1N}, D_{2N}	DSEI60-12A (1200 V, 60 A)
Switches	S_P and S_N S_{x1} and S_{x3} S_{x2}	6R045A (650 V, 60 A) FGL40N150D (1500 V, 40 A) FGL40N120D (1200 V, 40 A)
Resistor load	R	40 Ω

Figure 7 from top to bottom shows the simulation results for input voltage, capacitor voltages, output pole voltage, output phase voltage, and harmonic spectrum. By using 0.6 for D_0 and 0.15 for ST duty ratio (D_{ST}), as shown in Table 3, the capacitor voltages (V_{CP} and V_{CN}) are boosted to 60 V from 200 V of the dc input source, as illustrated in Figure 7. Therefore, the peak value of dc-link voltage can be identified as 320 V by summing the capacitor voltages and the input voltage. The peak-peak value of output pole voltage is equal to the dc-link voltage which has three levels: 160 V ($+V_{PN}/2$), zero, and −160 V ($-V_{PN}/2$), as shown in Figure 7. The output phase voltage has seven levels and its peak-peak value is varied from $-2/3V_{PN}$ to $+2/3V_{PN}$, as shown in Figure 7. By using the modulation index of 0.85, the peak value of the first order harmonic of output phase voltage is 156 V, approximately, as presented in Figure 7. The THD value of output phase voltage is 54.59%, which is measured by using the harmonic spectrum in Figure 7.

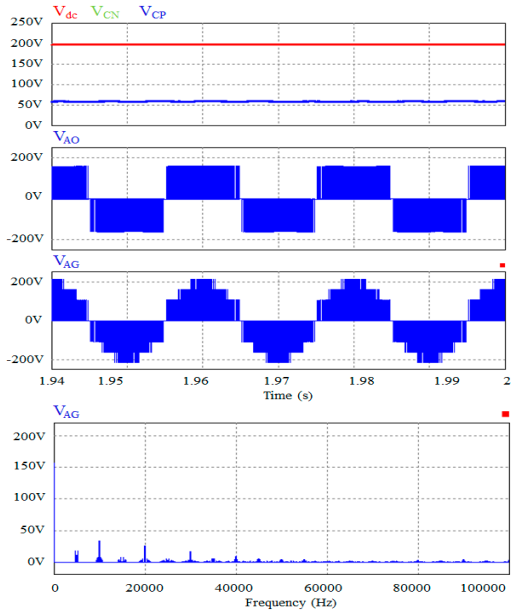

Figure 7. Simulation results of input voltage (V_{dc}), capacitor voltages (V_{CP}, V_{CN}), output pole voltage (V_{AO}), output phase voltage (V_{AG}), and harmonic spectrum of V_{AG}.

Figure 8 from top to bottom presents the simulation results for dc-link voltage, line-line voltage, and CMV. By using the full ST insertion, the dc-link voltage is varied from zero to the peak-value of dc-link voltage which is 320 V achieved in NST mode. The peak value of output line-line voltage is equal to dc-link voltage, so the top part of V_{AB} is varied from zero to 320 V, as illustrated in Figure 8. The old sectors of space vector diagram produce CMV varying from 0 to $-V_{PN}/6$, whereas the even sectors produce the CMV which varies from 0 to $+V_{PN}/6$. Therefore, when applying the introduced method, the CMV frequency is three times larger than the output voltage, and the peak-peak value of it is equal to $V_{PN}/3$ which varies from $-V_{PN}/6$ to $+V_{PN}/6$. The RMS value of CMV is 32.7 V_{RMS}.

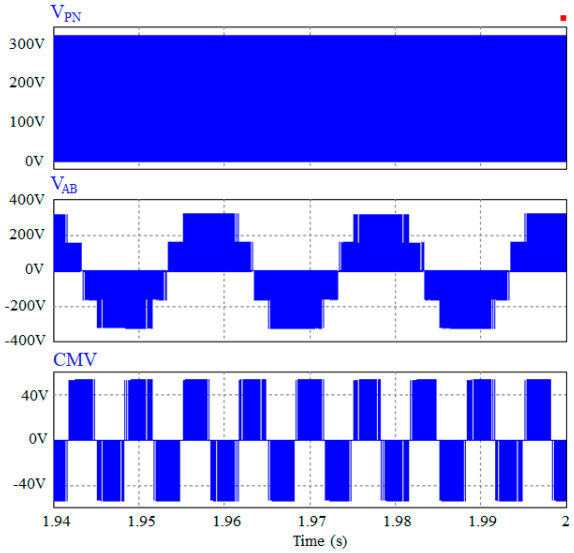

Figure 8. Simulation results of dc-link voltage (V_{PN}), line-line voltage (V_{AB}), and CMV.

Figure 9 from top to bottom shows the simulation results of the inductor current, three-phase output load voltage, and three-phase output load current. The inductor currents of two inductors are equal to each other. The average value of inductor currents is 11.7 and 11.6 A for I_{LP} and I_{LN}, respectively. Due to applying the low-pass filter before the resistor load, the output load voltage, as well as the output load current, have a good quality. The THD value of these waveforms is 2.38% for both voltage and current waveforms. The RMS value of output load voltage and output load current are 111 V_{RMS} and 2.78 A_{RMS}.

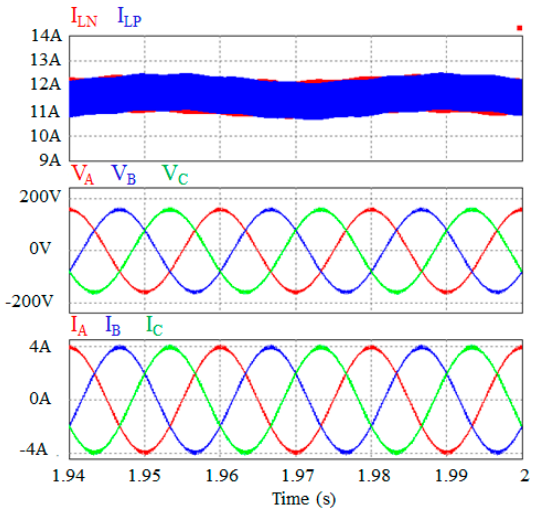

Figure 9. Simulation results of inductor current (I_{LP}, I_{LN}), three-phase output load voltage (V_A, V_B, V_C), three-phase output load current (I_A, I_B, I_C).

Figure 10 shows the simulation results of dc-link voltage, inductor current, DqSB network's active switch voltage stress, diode voltage stress. The inductor L_P stores energy in ST mode which appeared when the diode D_{2P} is reserved bias, as illustrated in Figure 10. In this time interval, the current through L_P linearly increases. The inductor current ripples are measured as 1.5 and 1.44 A for L_P and L_N, respectively. The inductor current is kept constant when S_P is turned on and the diode D_{1P} is reserved bias, as shown in Figure 10. As all switches of the inverter branch are triggered on, the DC-link voltage is zero in ST mode, whereas it achieves maximum value in NST mode, as presented in Figure 10.

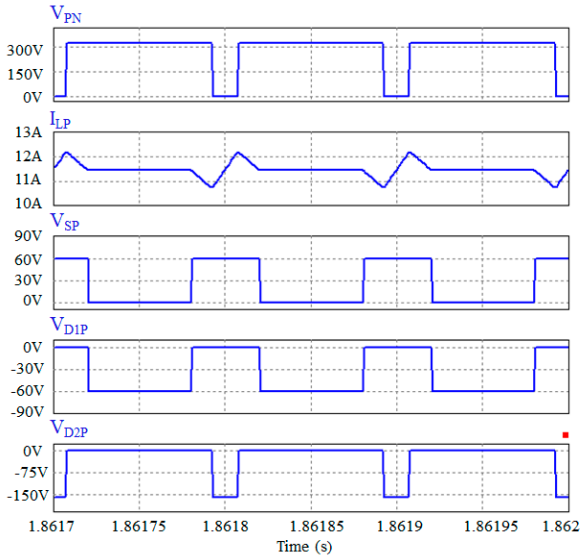

Figure 10. Simulation results of dc-link voltage (V_{PN}), inductor current (I_{LP}), DqSB network's active switch voltage stress (V_{SP}), diode voltage stress (V_{D1P}, V_{D2P}).

Figure 11 shows the investigation about voltage gain versus THD value of V_{AG} and voltage gain versus CMV. When the voltage gain increases, the modulation index decreases, which is demonstrated in Section 3. Thus, the THD value of output phase voltage increases with the increase of voltage gain. With all value of voltage gain, the 3L-DqSBT^{2}I method always produces a smaller value of THD value of V_{AG} than that of the SinPWM method in [35], as presented in Figure 11a. Moreover, the RMS value of CMV produced by the 3L-DqSBT^{2}I method is superior to that of the SinPWM method in [35], as illustrated in Figure 11b.

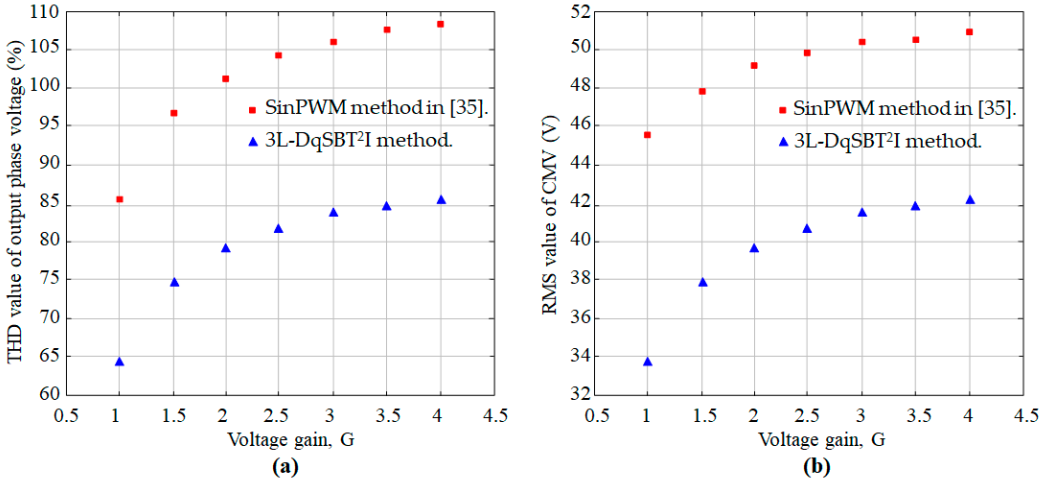

Figure 11. Comparison of (**a**) THD value of output phase voltage versus voltage gain, (**b**) RMS value of CMV versus voltage gain.

4.2. Experimental Results

The performance of the proposed inverter was further validated through the experiment. A 1 kW prototype was carried out in a laboratory with the parameters listed in Table 3, which is the same as the simulation. This prototype was controlled by a DSP F28335 microcontroller and FPGA Cyclone II EP2C5T144C8. The gate-drive was based on TLP250, which fed to IGBT FGL40N150D, which are low-side and high-side switches of 3L-T^{2}I branch, while IGBT FGL40N120D and MOSFET 6R045A were installed for bidirectional switches and DqSB network's switches, respectively. The three-phase resistive load was considered to verify the proposed methods, which was fed through three-phase LC filter with the cut-off frequency of approximately 1 kHz by applying 3 mH and 10 µF for inductor value and capacitor value, respectively. The photo of experiment prototype is illustrated in Figure 12. The experimental results are shown in Figure 13.

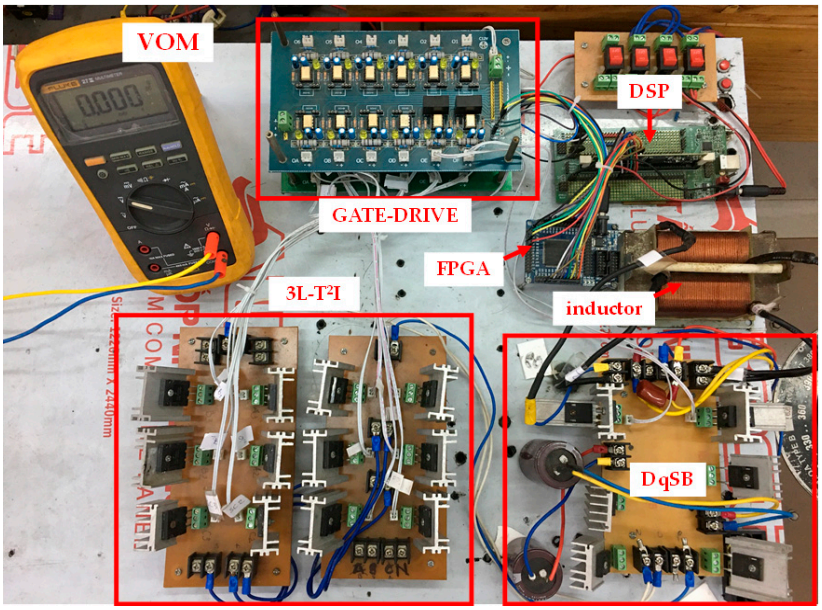

Figure 12. Experimental prototype.

Figure 13 shows the experimental results of output phase voltage (V_{AG}), CMV, output line-line voltage (V_{AB}), output load voltage (V_A), output load current (I_A), inductor current (I_{LP}), diode voltage (V_{D1P} and (V_{D2P}), dc-link voltage (V_{PN}), dc input voltage (V_{dc}), capacitor voltage (V_{CP} and V_{CN}), and the harmonic spectrum of output phase voltage and output load current.

The capacitor voltages (V_{CP} and V_{CN}) are, respectively, boosted to 53 and 51 V from 200 V dc input source by applying the ST duty ratio of 0.15 and coefficient D_0 of 0.6, as shown in Figure 13c. Therefore, the peak-value of dc-link voltage is 304 V which is the sum of capacitor voltage and dc input power supply, as presented in Figure 13c. The variation of top part of output line-line voltage is from zero to dc-link voltage. The output phase voltage has seven-level voltage which varies from $-2/3V_{PN}$ to $+2/3V_{PN}$. The form of output load voltage and output load current are sinewave which are achieved by applying LC filter before feeding to the load, as illustrated in Figure 13b. Their RMS values are 104 V_{RMS} and 2.5 A_{RMS}, respectively. The simulated values are nearly the calculated values, whereas the calculated values are higher than the measured values. This is because the SVP method is used to obtain a high voltage gain, and the voltage drops across the devices, caused by high currents, are dominant. The CMV generated by proposed topology when applying introduced method varies from $-V_{PN}/6$ to $+V_{PN}/6$, as shown in Figure 13a. The RMS value of CMV is 32.6 V_{RMS}. Figure 13c shows that the inductor current is linearly increased when the dc-link voltage achieves zero value while the diode D_{2P} is reserved bias which represents ST state. While, the constant value of inductor current is obtained when NST mode 1 is achieved, which is represented by reserving bias the diode D_{1P}.

Figure 13e,f shows the harmonic spectrum of V_{AG} and I_A. It can be seen that the peak-value of the harmonic spectrum of output phase voltage is 104 V_{RMS} at the first-order harmonic of 50 Hz. By using a low-pass LC filter, the magnitude of high-frequency harmonics of V_{AG} is reduced and approximately equal to zero. The magnitude of the first harmonic of the load current, I_A is around 2.5 A_{RMS} as illustrated in Figure 13f. Based on the harmonic spectrum analysis, the THD values of output voltage and current can be calculated as 62.4% and 2.77%, respectively.

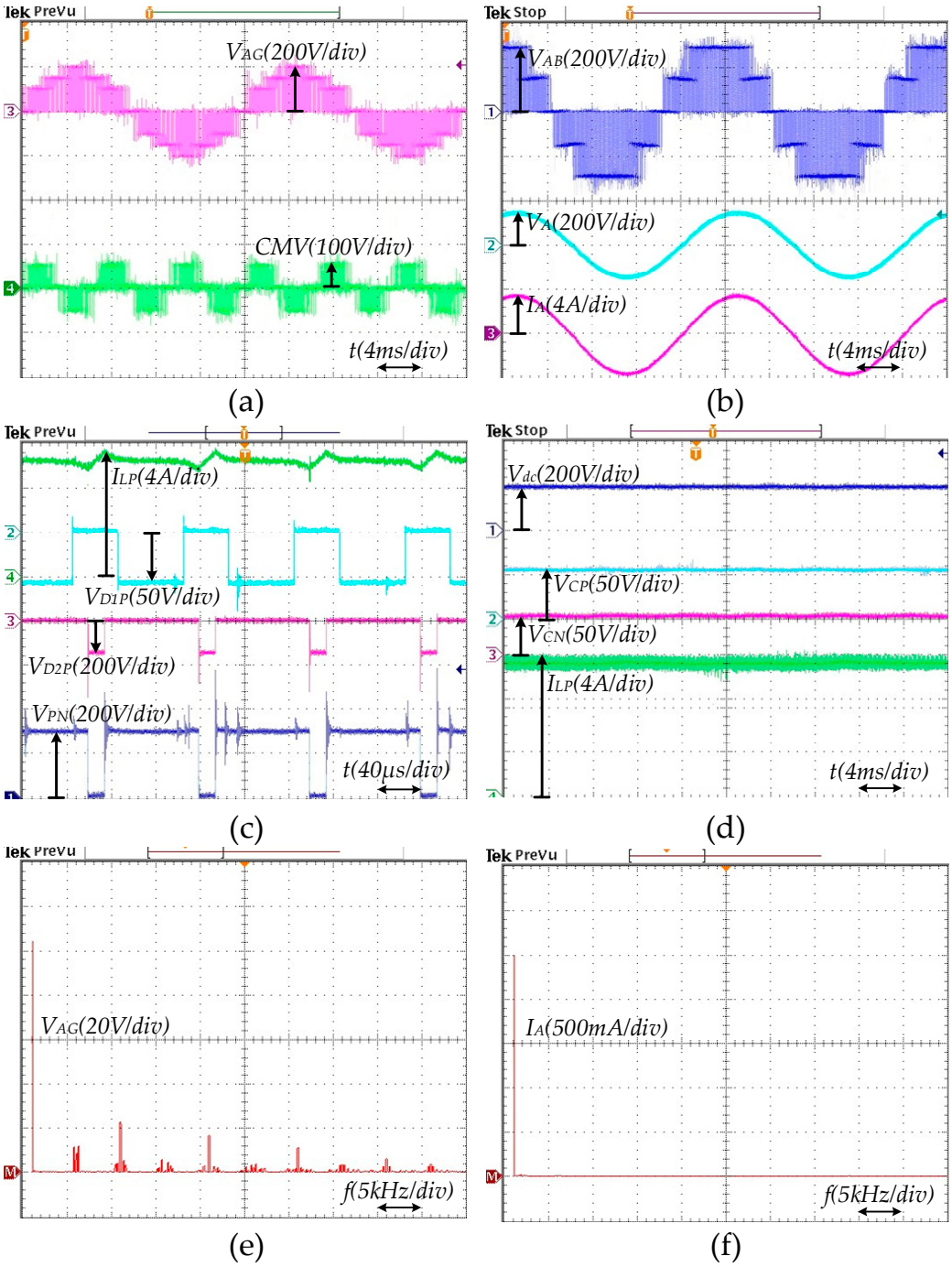

Figure 13. Experimental results of 3L DqSBT^{2}I under SVP control method. (**a**) output phase voltage V_{AG} and common-mode voltage, (**b**) output line-line voltage V_{AB}, output load voltage V_A, output load current I_A, (**c**) inductor current I_{LP}, diode voltages V_{D1P}, V_{D2P}, dc-link voltage V_{PN}, (**d**) input voltage V_{dc}, capacitor voltages V_{CP}, V_{CN}, inductor current I_{LP}, (**e**) harmonic spectrum of V_{AG}, and (**f**) harmonic spectrum of I_A.

5. Conclusions

This paper proposed the 3L DqSBT^{2}I configuration which combines all advantages of the 3LT^{2}I and the DqSB network. This configuration is controlled by the SVP technique with some benefits such as enhancing modulation index and reducing the magnitude as well as the slew-rate of CMV. In this scheme, the zero vector, medium vectors, and large vectors were utilized to generate the output voltage. The control signal of intermediate network power switches was also detailed to provide the high boost factor and voltage gain. As a result, the voltage stress on power devices like capacitors, diodes, and switches were decreased significantly. To validate the performance of the proposed method, the PSIM simulation and the laboratory prototype experiment were conducted. Furthermore, the comparisons between the proposed method and other conventional schemes were carried out to confirm the effectiveness of the proposed technique. Due to all benefits mentioned above, this configuration is suitable for low and medium voltage applications like photovoltaic systems or motor drives.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

3L-T2I	three-level T-Type inverter
3L-DqSBT2I	three-Level DC-link type quasi switch boost T-type inverter
B	boost factor of the inverter
CMV	common-mode voltage
D_0	duty cycle of DqSB network's active switches
DqSB	dc-link type of the qSB
D_{ST}	shoot-through duty ratio
FC	flying capacitor
f	switching frequency of the inverter
G	voltage gain of the inverter
I_A	A-phase output load current
I_{LP}	inductor L_P current
ΔI_{LP}	inductor current ripple of L_P
I_{LN}	inductor L_N current
ΔI_{LN}	inductor current ripple of L_N
m	modulation index
MIs	multilevel inverters
NPC	neutral point clamped
NST	non-shoot-through
PV	photovoltaic systems
PWM	pulse width modulation
qSB	quasi-switch boost
qSBI	quasi-switch boost inverter
qZS	quasi-Z-source
qZSI	quasi-Z-source inverter
RMS	root mean square
ST	shoot-through
SVP	space vector pulse width modulation
T	switching period of the inverter

THD	total harmonic distortion
T_M	drew-time of medium vector
T_L	drew-time of large vector
T_Z	drew-time of zero vector
UPS	uninterruptable power supply
$\vec{V}_0$	zero vector
$\vec{V}_1$, $\vec{V}_3$	large vectors
$\vec{V}_2$	medium vector
V_{AB}	output line-line voltage
V_{AG}	A-phase output phase voltage
V_{AO}	A-phase output pole voltage
V_{BO}	B-phase output pole voltage
V_C	capacitor voltage
V_{CMV}	common-mode voltage
V_{CN}	voltage across C_N
V_{CO}	C-phase output pole voltage
V_{CP}	voltage across C_P
V_{dc}	dc input voltage
V_{D1P}	diode D_{1P} voltage
V_{D2P}	diode D_{2P} voltage
V_{GO}	common-mode voltage
V_{LP}	voltage across L_P
V_{LN}	voltage across L_N
V_{PN}	dc-link voltage
$\vec{V}_{ref}$	reference vector
V_{SP}	switch S_P voltage
$V_{x,\,peak}$	peak value of the first harmonic of output phase voltage
ZS	Z-source
ZSI	Z-source inverter

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