

Article

# Understanding Turn-On Transients of SiC High-Power Modules: Drain-Source Voltage Plateau Characteristics

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Received: 19 June 2020; Accepted: 21 July 2020; Published: 24 July 2020



**Abstract:** The SiC (silicon carbide) high-power module has great potential to replace the IGBT (insulated gate bipolar transistor) power module in high-frequency and high-power applications, due to the superior properties of fast switching and low power loss, however, when the SiC high-power module operates under inappropriate conditions, the advantages of the SiC high-power module will be probably eliminated. In this paper, four kinds of SiC high-power modules are fabricated to investigate fast switching performance. The variations in characteristics of drain-source voltage at turn-on transient under the combined conditions of multiple factors are studied. A characteristic of voltage plateau is observed from the drain-source voltage waveform at turn-on transient in the experiments, and the characteristic is reproduced by simulation. The mechanism behind the voltage plateau is studied, and it is revealed that the characteristic of drain-source voltage plateau is a reflection of the miller plateau effect of gate-source voltage on drain-source voltage under the combined conditions of fast turn-on speed and low DC bus voltage, while the different values of drain-source voltage plateau are attributed to the discrepancy of structure between upper-side and lower-side in the corresponding partial path of the drain circuit loop inside the module, with the standard 62 mm package outline.

**Keywords:** power module; silicon carbide; turn-on transient

## 1. Introduction

The switching transient of power devices/modules has been widely studied, based on double pulse test (DPT) experiments. There were many reports about the influence of structure of power converter/module on switching transient, such as the issue of overshoot voltage by drain circuit loop [1,2], the oscillation issue by inductance of gate driver loop [3], the different switching speed due to the difference of module structure [4–7], the voltage/current spikes by interconnect parasitics of power converters [8], and the switching loss by parasitic capacitance of a power module/converter [9–11]. These studies showed that the influence of structure on switching transient was reflected in multiple fields or dimensions, e.g., overshoot voltage, oscillation, and switching loss.

There were reports about the impact of test conditions on switching transient, such as the influence of load on switching transients [12], the variations in external gate resistance caused different slew rate of drain-source voltage [13], the parameters of the gate driver circuit determined the maximum switching speed [14]. The influence of test condition on switching transient was mainly related to the field of switching speed.

For the influence of switching speed on switching transient, the research was mainly focused on the serious issues existed along with fast switching, such as the high frequency oscillation in upper-side

and the excessively low negative voltage spike in lower-side for gate-source voltage of a silicon carbide (SiC) power module [15], the temporary shoot-through issue [16,17], the cross-talk issue for a converter with typical half-bridge configuration [18,19]. These studies illustrated that fast switching speed with different structure of module/converter caused different characteristics of switching transient. This meant that the abnormal transients caused by the switching speed were usually the results by the combined impacts of structure and switching speed.

Most of the previous works about turn-on transient of power devices/modules mainly focused on the influence for the variation of a single factor or a combined impact of two factors, such as parasitic inductance of structure and the switching speed. However, the characteristics of drain-source voltage at turn-on transient in a real system can be varied under combined conditions that multiple factors change together.

As mentioned in previous surveys of the literature, under the impact of single factor, the turn-on transients change in one dimension, e.g., only a single characteristic of gate-source voltage appears, or the values of some key turning points for drain-source voltage waveform vary but the overall characteristic of drain-source voltage ( $v_{DS}$ ) waveforms does not change. However, under the combined impacts of the multiple factors, the turn-on transients vary likely in one more dimension, also, the trend of change in characteristics of drain-source voltage could be observed clearly. For example, along with the values of key turning points for drain-source voltage waveform vary, the characteristics in the shape of drain-source voltage waveform also change probably from a two-substage-falling to a single-stage-falling.

As we all know, the switching performance of the power module, i.e., turn-on speed and power loss, is directly related to the characteristics of drain-source voltage at turn-on transient. Compared with the characteristic of  $v_{DS}$  waveforms consisting of only single-stage-falling, the characteristic of  $v_{DS}$  waveforms consisting of the two-substage-falling prevents  $v_{DS}$  from falling down as quickly as possible. Consequently, the turn-on process is prolonged and power loss is increased at turn-on transients. As a result, the advantages of the SiC high-power module over high speed switching and high-frequency performance are eliminated.

Therefore, it is important to understand the mechanism of the variations in characteristics of drain-source voltage under the combined impacts of multiple factors. It is conducive to enabling the advantages of the SiC high-power module over high speed switching and high-frequency performance; on the other hand, it can also help reduce the difference in switching performance of the module between upper-side and lower-side.

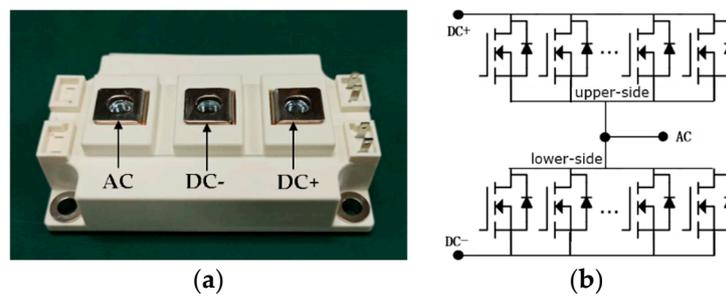
In this work, based on the developed SiC high-power modules and the clamped inductive DPT rig, the variations in characteristics of  $v_{DS}$  under the combined impacts of various SiC power dies, module's structure, turn-on speed and test conditions are firstly investigated by experiments. Then, the characteristics of drain-source voltage plateau are studied by simulation.

The paper is organized as follows. Section 2 introduces the experiment setup which includes the developed SiC high-power modules and a clamped inductive load DPT rig. In addition, the typical turn-on transient process of module is briefly introduced. Section 3 shows the experimental results about the characteristics of drain-source voltage plateau. In Section 4, the mechanism behind the characteristics of the drain-source voltage plateau is studied with modeling and simulation. Finally, Section 5 concludes the article.

## 2. Experiment Setup

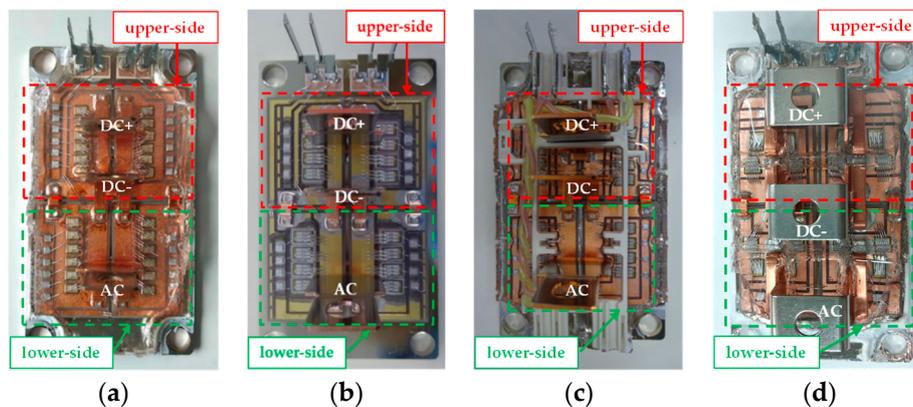
### 2.1. Introduction of the Developed SiC High-Power Module

Four kinds of SiC high-power modules, which are designated as module\_A, module\_B, module\_C, and module\_D, are developed for investigating the turn-on transient characteristics of the module at high current output. All power modules have the same physical outline of standard 62 mm package and the circuit topology of half-bridge configuration, as shown in Figure 1.



**Figure 1.** Outline and circuit topology of the developed silicon carbide (SiC) high-power module: (a) standard 62 mm package outline, (b) circuit topology of half-bridge configuration.

The difference among these modules are mainly reflected in the inner structure and the used power dies including the types and the parallel number of the power dies. As shown in Figure 2, the inner structure of the module\_B is same with that of the module\_A, but different from that of module\_C, while the structure of module\_D is different from that of other modules.



**Figure 2.** The inner structure inside the developed SiC power modules: (a) module\_A, (b) module\_B, (c) module\_C, (d) module\_D.

As shown in Table 1, there are two types of SiC-MOSFET dies adopted inside the developed modules, the type of adopted SiC-MOSFET dies in module\_A is different from that of other modules. The parallel number of SiC-MOSFET dies in module\_B is same with that of module\_C, and the parallel number of SiC-MOSFET dies in module\_D is different from that of module\_B and module\_C.

**Table 1.** The used SiC dies inside the developed power module.

Modules <sup>1</sup>	Module_A	Module_B	Module_C	Module_D
SiC-MOSFET dies	S2301TCST	CPM2-1200-0025B	CPM2-1200-0025B	CPM2-1200-0025B
Parallel number of dies	12	8	8	4
Supplier of dies	ROHM	CREE	CREE	CREE
Input capacitance	24.12 nF	22.30 nF	22.30 nF	12.15 nF
Voltage/Current ratings	1200 V/300 A	1200 V/400 A	1200 V/400 A	1200 V/200 A

<sup>1</sup> Note: There are anti-parallel SiC-SBD dies as freewheeling diodes in the module\_D, which is the CPW5-1200-Z050B from CREE, its parallel number is 4. There are no anti-parallel diodes used in the other modules.

With the various designs for the number of parallel-connected power die inside the module, the values of input capacitance of the modules are different accordingly. Thus, the various turn-on speed can be achieved for the modules under the same test conditions (same  $V_{DD}$ ,  $I_O$ , and  $R_{gext}$ ), and with a same gate driver circuit in the following experiments. This is helpful for the study of influence of turn-on speed on the turn-on transient, especially the characteristics of drain-source voltage.

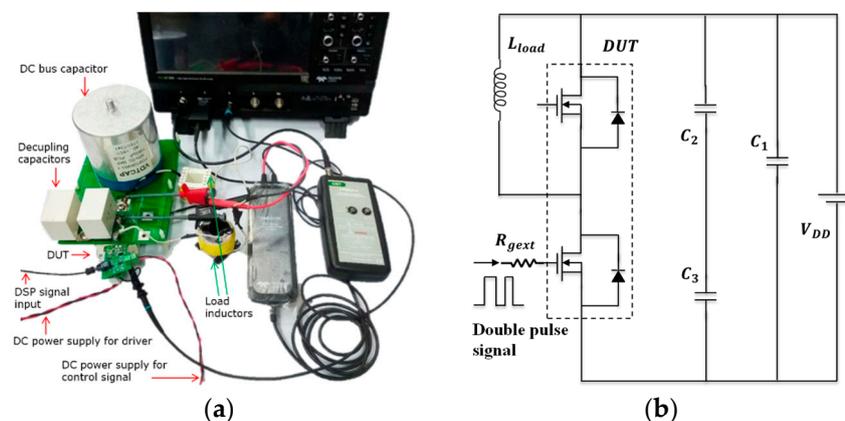
The module\_B has the same structure but different power dies with module\_A, and also have the same power dies but different structure with module\_C. The module\_D is designed with only 4 parallel SiC-MOSFET dies and a consequent very small input capacitance to enable a faster turn-on at high current output. It is worth noting that the circuit is carefully designed to eliminate severe negative gate-source voltage spike during the turn-on transient.

In order to slow down appropriately turn-on speed, the additional common source path is introduced in both module\_A and module\_B, but for other modules, the common source path inside modules is minimized. In addition, since the turn-on speed of module\_D is much higher than other modules, in order to avoid the interference due to a faster turn-on speed to the gate-source voltage of the module at turn-on transient, the difference in gate-source routings for the parallel power dies is reduced, and the symmetry of them is improved, meanwhile, the drain-source path inside module is also optimized to reduce its parasitic inductance.

Based on these designs, the influence of power dies on characteristics of  $v_{DS}$  can be compared between module\_A and module\_B, while the influence of module's structure on characteristics of  $v_{DS}$  can be compared between module\_B and module\_C. The impact of the faster turn-on speed on characteristics of  $v_{DS}$  can be reflected from module\_D under the same gate driver circuit and test conditions.

## 2.2. Introduction of the Double Pulse Test Platform

The physical picture of the clamped inductive DPT rig is shown in Figure 3a. The device under test (DUT) is the developed module. The decoupling capacitor is from KEMET. The load inductor is self-fabricated by serial-connected two inductors. The DC bus capacitor with part number of FG810K901-1 is from VDTCAP. The voltage rating of this DC bus capacitor is 900 V. Due to this, we have to ensure that the sum of the applied DC bus voltage ( $V_{DD}$ ) and overshoot voltage is no more than 900 V at experiments.



**Figure 3.** The inductive load double pulse test (DPT) circuit platform: (a) physical picture, (b) schematic diagram of circuit.

The 1GHz high definition oscilloscope with part number of HDO6104A used for acquiring the voltage and current signals is from Teledyne Lecroy. A Rogowski current waveform transducer with part number of CWT miniHF 1B utilized to measure drain-source current of DUT is from PEM, the bandwidth of this current probe is 30 MHz. A passive voltage probe with part number of PP026-2 used for measuring gate-source voltage is from Teledyne Lecroy, the bandwidth of this voltage probe is 500 MHz. A high voltage differential probe with part number of HVD3106 used to obtain the drain-source voltage is from Teledyne Lecroy, the bandwidth of this high voltage probe is 120 MHz.

The schematic diagram of the DPT circuit is shown in Figure 3b. The double pulse signal is applied to the gate-source of DUT by gate-driver circuit. The gate-source voltage for turning off and

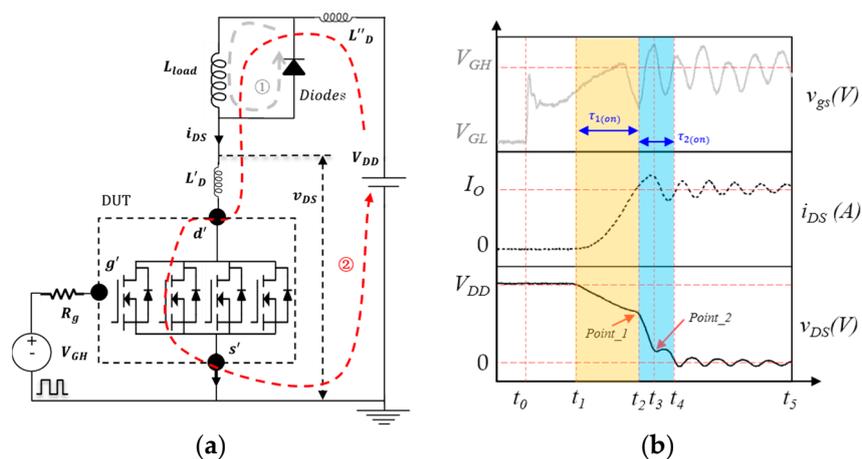
turning on switches is  $-2.3$  V and  $17.5$  V, respectively. The  $R_{gext}$  is external resistor of the gate driver circuit. The values of electrical parameter of some components in DPT rig are listed in Table 2.

**Table 2.** The value of electrical parameter of components in DPT rig.

Components	Names	Value
DC-bus capacitor	C1	1000 $\mu$ F
Decoupling capacitor	C2	3 $\mu$ F
Decoupling capacitor	C3	3 $\mu$ F
Load inductor	$L_{load}$	160 $\mu$ H

### 2.3. Introduction of the Turn-On Transient Process for SiC High-Power Module

The diagram of commutation paths at turn-on transient is shown in Figure 4a, SiC MOSFET dies are in off-state off initially, the voltage applied between gate and source ( $V_{GS}$ ) is set to  $V_{GL}$ , the load current circulates along the loop\_①, as shown by the gray dash line. At turn-on transient the gate-source voltage ( $V_{GS}$ ) increase from  $V_{GL}$  to  $V_{GH}$ , the circulating current starts to transfer from the loop\_① to the loop\_②, as marked by red dash line. After turn-on transient process, the load current flows fully by SiC-MOSFETs, instead of the freewheeling diodes.



**Figure 4.** Typical diagrams for turn-on transient analysis for SiC high-power module in DPT: (a) commutation paths of the current flow, (b) turn-on transient process.

The typical diagram of turn-on transient for SiC high-power module is shown in Figure 4b. The whole fall process of  $v_{DS}$  at turn-on transient can be divided by two distinct phases.

The phase from  $t_1$  to  $t_2$  is the 1st turn-on interval,  $\tau_1(\text{on})$ . During the  $\tau_1(\text{on})$ , with the  $i_{DS}$  rises to  $I_O$ , the  $v_{DS}$  fall linearly with time and the  $v_{gs}$  is pulled down to a lowest value, due to the negative feedback effect. The voltage drop induced by the rising  $i_{DS}$  and parasitic inductance is given by

$$\Delta V_{DS} = L_D \frac{di_{DS}}{dt} \quad (1)$$

where  $L_D$  is the parasitic inductance of the whole drain circuit loop in DPT, which includes the parasitic inductance of routings from the power terminals of “DC+” to “DC−” inside the module,  $L_{D,1}$ , and the parasitic inductance of drain circuit loop excluding the routings inside the module in DPT,  $L_{D,2}$ .

The phase from  $t_2$  to  $t_4$  is the reverse recovery process of the freewheeling diodes, which is the 2nd turn-on interval,  $\tau_2(\text{on})$ . It consists of two sub-phases. During sub-phase from  $t_2$  to  $t_3$ , the  $i_{DS}$  continues to rise to its maximum, since the voltage starts to be clamped to freewheeling diode, the  $v_{DS}$  reduces in a higher  $dv_{DS}/dt$  due to reverse recovery. During the sub-phase from  $t_3$  to  $t_4$ , the reverse

recovery current of freewheeling diode decreases from its maximum to zero, the  $i_{DS}$  also decreases from the maximum to  $I_O$ , the turn-on transient of SiC-MOSFET is completed at the end of this phase.

During this phase from  $t_2$  to  $t_4$ , the operation mode of SiC-MOSFET dies changes from saturation region to linear region. After  $t_4$ , the SiC-MOSFET is fully turned-on. All  $v_{gs}$ ,  $v_{DS}$ ,  $i_{DS}$  characteristics are kept in oscillation state with their respective frequencies which are determined by the parasitic parameters in the circuit.

As shown in Figure 4b, during the  $v_{DS}$  falls from  $V_{DD}$  to zero, the operation mode of SiC-MOSFET dies changes from saturation region to linear region. Point\_1 is the turning point for  $v_{DS}$ , changing from  $\tau_1(\text{on})$  to  $\tau_2(\text{on})$  during SiC-MOSFET dies operate in saturation region, which corresponds to the moment when  $i_{DS}$  rises to  $I_O$ , while Point\_2 is the turning point in  $v_{DS}$  when the operation mode of SiC-MOSFET dies changing from saturation to linear region, which corresponds to the moment when  $i_{DS}$  rising up to the maximum value.

Under the combined impacts of multiple factors such as various test conditions, turn-on speed and structures of DUT, the turn-on transients of  $v_{DS}$  from  $t_1$  to  $t_4$  are probably varied in more than one dimension, the values of the key turning point vary, and, meanwhile, the characteristics of  $v_{DS}$  waveforms such as the number of key turning points and the shape of drain-source voltage waveform also change, so that the different characteristics of the falling process of  $v_{DS}$  waveforms could be observed. Therefore, in order to facilitate comparison between the modules in the following sections, we neglect the variations in the value of the turning point and just focus on changes in characteristics of  $v_{DS}$ , such as the number of key turning points, whether there is a characteristic of point\_2 or not, and whether there is a characteristic of the voltage plateau or not.

### 3. Experimental Results

The turn-on transient of SiC high-power module is essentially the charging process of the input capacitance of the module by the gate driver circuit. The rise of  $i_{DS}$  is determined by the charging speed of the input capacitance of the module. We can simply view this system consisting of gate driver and the input capacitance of the module as a one-order low-pass resistance-capacitance (RC) network, where the output of gate driver circuit can be regarded as input signal of the network, and the gate-source voltage ( $v_{gs}$ ) is the output of this network. The response of this network to the turn-on signal determines the ideal transient waveform of  $v_{gs}$  and defines the turn-on speed of the module. To facilitate analysis, we use the rise time of this one-order low-pass RC network as a precursor of turn-on speed of the module. Since the module operates in saturation mode, the  $i_{DS}$  is proportional to the  $v_{gs}$  at turn-on transient. Hence, a shorter rise time means a faster turn-on speed for the developed modules.

The rise time of the output for the one-order low-pass RC network can be given by

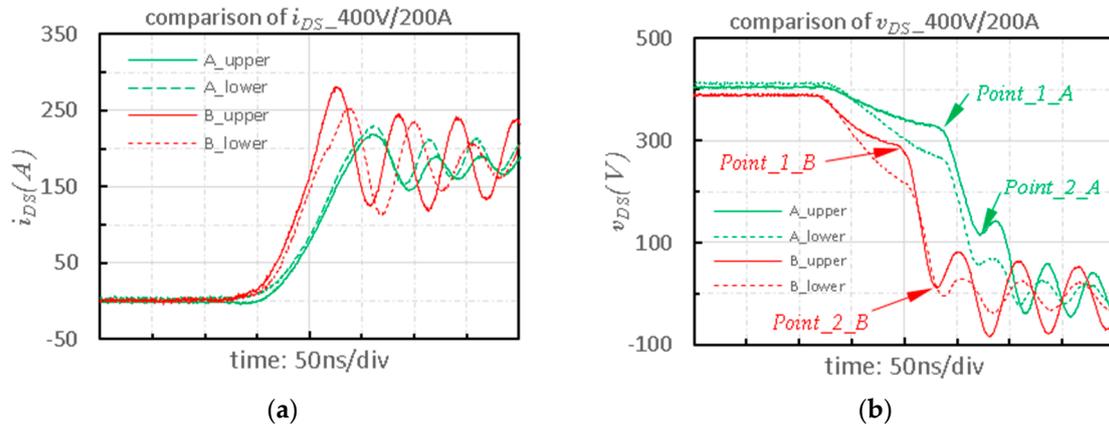
$$t_r = 2.2R_gC_{iss} \quad (2)$$

where  $t_r$  is rise time,  $R_g$  is the resistance of the whole gate driver loop,  $C_{iss}$  is the input capacitance of the module. According to Equation (3), there are two ways to increase the turn-on speed of the developed modules for a specific gate driver circuit, namely, reducing the external gate resistance in DPT and driving a module with a lower input capacitance. Based on the input capacitance of the developed modules shown in Table 1, it is predicted that the turn-on speed of module\_A is the slowest, while module\_D is the fastest under the same test conditions (same  $V_{DD}$ ,  $I_O$ , and  $R_{gext}$ ).

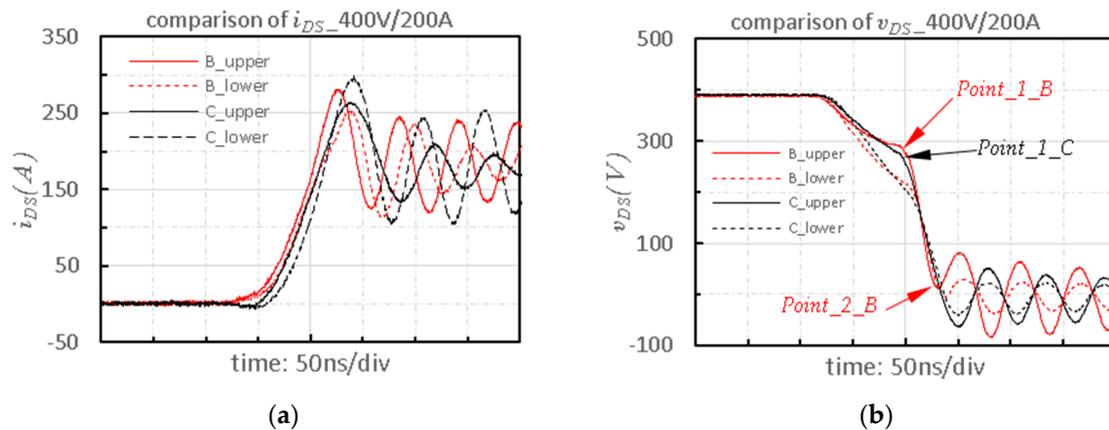
In order to investigate the influence of module's structures on the turn-on transient of  $v_{DS}$ , the comparative experiments are carried out under various conditions of  $V_{DD}$ . Finally, the trend of changes in influence of module's structures on characteristics of  $v_{DS}$  with the increase of tun-on speed or the reduce of  $V_{DD}$  is summarized.

### 3.1. Turn-On Transient at Condition of Relatively High $V_{DD}$

The experimental results under relatively high  $V_{DD}$  are shown in Figures 5–7, where  $V_{DD}$  is set to be 400 V,  $I_O$  is set to be 200 A, and  $R_{gext}$  is set to be 2.4  $\Omega$ . The green, red, black, and purple lines stand for the experimental results of module\_A, module\_B, module\_C, and module\_D, respectively; the solid and dash lines stand for the experimental results of the upper-side and lower-side respectively for a corresponding module.



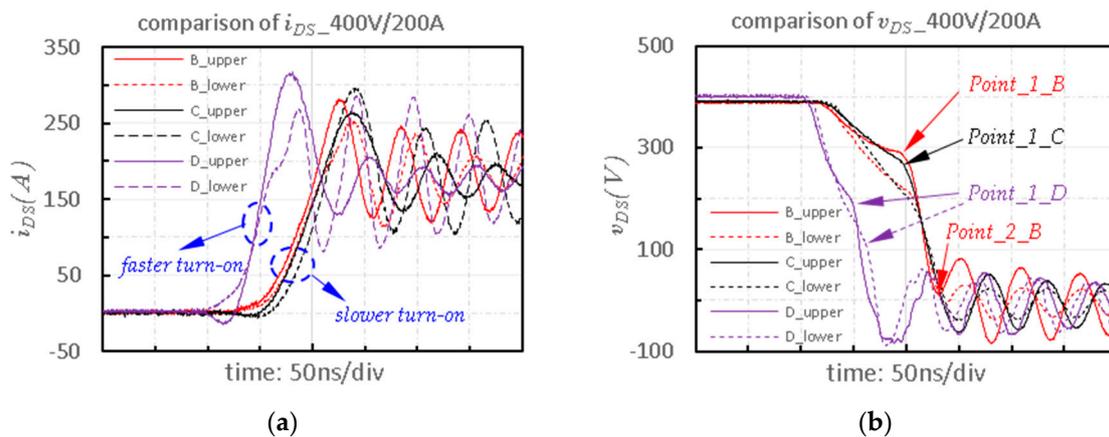
**Figure 5.** The comparison of turn-on transient waveforms of the modules with the same structure design but different power dies under condition of high  $V_{DD}$ : (a) waveform of  $i_{DS}$ , (b) waveform of  $v_{DS}$ .



**Figure 6.** Comparison of turn-on transient waveforms of the modules with different structure design but same power dies under condition of high  $V_{DD}$ : (a) waveform of  $i_{DS}$ , (b) waveform of  $v_{DS}$ .

Figure 5 shows the comparison of turn-on transient waveforms of module\_A and module\_B, which have the same structure design but different power dies. The characteristics of  $v_{DS}$  are same with each other, the characteristics of  $v_{DS}$  of two modules show two turning points, as marked by Point\_1 and Point\_2 in Figure 5b, though the values of the turning points corresponding to each other show some difference between two modules, such as 28.7 V in upper-side and 30.4 V in lower-side for Point\_1.

Figure 6 shows the comparison of turn-on transient waveforms of module\_B and module\_C, which have the same power dies but different structure designs. The characteristics of  $v_{DS}$  of module\_C is different from that of the module\_B, and there is only Point\_1 existing in  $v_{DS}$  waveform, Point\_2 which corresponds to the operation mode of SiC-MOSFET dies changing from saturation to linear region is not observed in  $v_{DS}$ , as shown in Figure 6b. In addition, the difference in value of  $v_{DS}$  at Point\_1 between these two modules still exists but it is reduced, e.g., it is just 16.4 V on the upper-side, while it is 9.6 V on the lower-side.



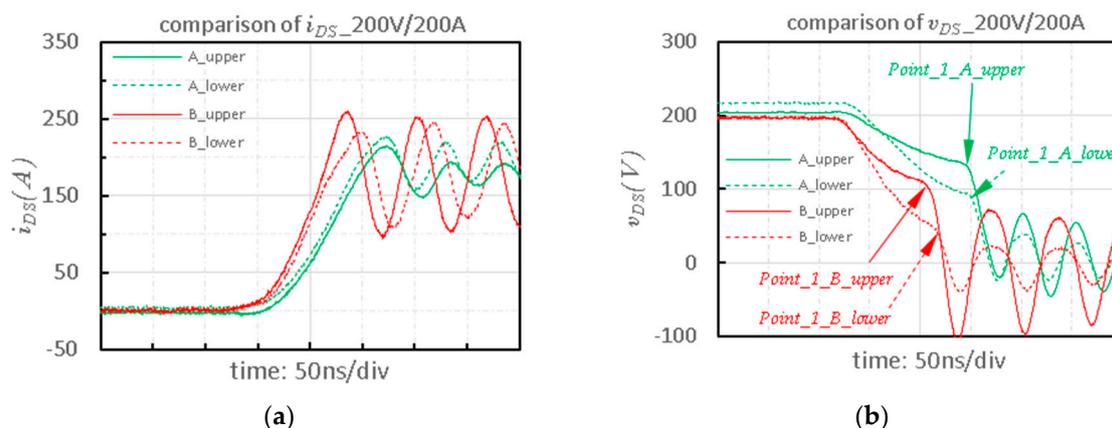
**Figure 7.** The turn-on transient waveforms of SiC high-power modules under condition of high  $V_{DD}$ : (a) waveform of  $i_{DS}$ , (b) waveform of  $v_{DS}$ .

Figure 7 shows the comparison of turn-on transient waveforms of the modules with various turn-on speed. The turning on process of module\_D is faster than that of the other modules, due to the smaller input capacitance and shorter rise time, the characteristic of  $v_{DS}$  in module\_D is fully different from that of other two modules, Point\_1 is negligible and Point\_2 disappears, as shown in Figure 7b. This means that as turn-on speed increases, the  $v_{DS}$  falls faster at turn-on transient, as a result, the characteristics that is corresponding to the operation mode of SiC-MOSFET dies changing from saturation to linear region in  $\tau_2(\text{on})$  disappear in  $v_{DS}$ , and characteristics that is corresponding to the  $v_{DS}$  changing from  $\tau_1(\text{on})$  to  $\tau_2(\text{on})$  during the SiC-MOSFET dies operating in saturation mode, start to be weakened in  $v_{DS}$ .

In summary, although the voltage values of the corresponding Point\_1 are different from each other, the characteristics of  $v_{DS}$  for the modules with the same structure design are same, and the characteristics of  $v_{DS}$  for the modules with the different structure design are different.

### 3.2. Turn-On Transient at Condition of Low $V_{DD}$

The experimental results under the condition of relatively low  $V_{DD}$  are shown in Figures 8 and 9, where  $V_{DD}$  is set to be 200 V,  $I_O$  is set to be 200 A, and  $R_{gext}$  is set to be 2.4  $\Omega$ .



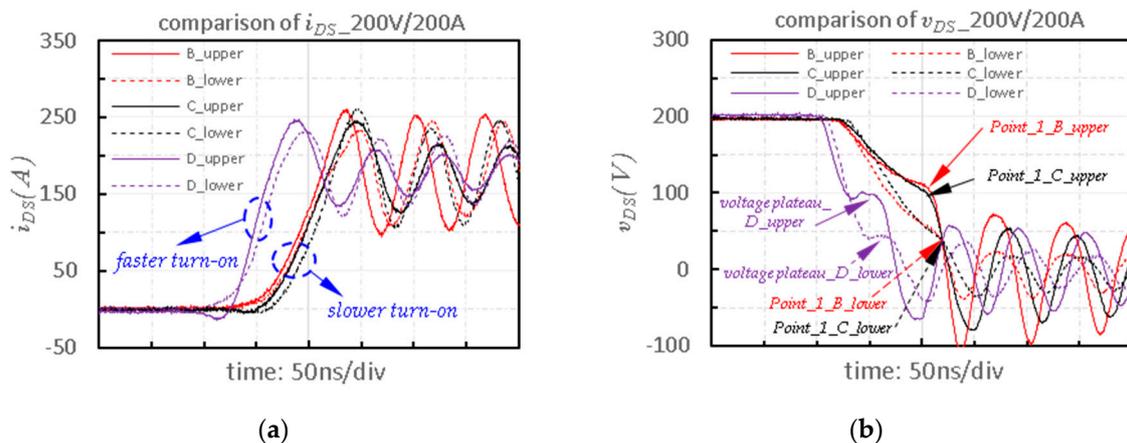
**Figure 8.** The turn-on transient waveforms of the modules with the same structure design but different power dies under condition of low  $V_{DD}$ : (a) waveform of  $i_{DS}$ , (b) waveform of  $v_{DS}$ .

Figure 8 shows the comparison of turn-on transient waveforms of module\_A and module\_B in low  $V_{DD}$  condition, the two modules have the same structure design but different power dies. It is shown that the characteristics of  $v_{DS}$  of the two modules are similar, that is, only one turning point

is observed. This is different from the case of high  $V_{DD}$  condition. The decrease of  $V_{DD}$  causes the characteristic corresponding to the operation mode of SiC-MOSFET dies changing from saturation to linear region in  $\tau_2(\text{on})$  disappears in  $v_{DS}$ . As depicted previously, the difference in values of  $v_{DS}$  at Point\_1 between the two modules still exists. The difference in values of  $v_{DS}$  at Point\_1 between the two modules is 13.5 V in upper-side and 40.8 V in lower-side.

The characteristics of  $v_{DS}$  for the modules with the same structure design are same, though the level of  $V_{DD}$  takes effect on characteristics of  $v_{DS}$  at turn-on transient and there is a difference in the value of  $v_{DS}$  at point\_1 between the different modules.

Figure 9 shows the comparison of turn-on transient waveforms of module\_B, module\_C, and module\_D in condition of low  $V_{DD}$ . For module\_B and module\_C, their turn-on speed is relatively slower, the characteristics of  $v_{DS}$  is not different from each other, although the module structure design is different. Namely, both modules show only one turning point. The discrepancy in characteristics of  $v_{DS}$  caused by the difference of module structures in the case of high  $V_{DD}$  condition is not observed in lower  $V_{DD}$  case. Hence, the lower  $V_{DD}$  weakens the influence of module's structures on the characteristics of  $v_{DS}$ , the difference of module's structures does not result in the different characteristics of  $v_{DS}$ , except for the difference in values of  $v_{DS}$  at Point\_1 between two modules which is 8.8 V at the upper-side and 2.4 V at the lower-side for Point\_1.



**Figure 9.** The turn-on transient waveforms of SiC high-power modules under condition of low  $V_{DD}$ : (a) waveform of  $i_{DS}$ , (b) waveform of  $v_{DS}$ .

However, when the turn-on speed is faster as for module\_D, the voltage plateau is observed from the characteristic of  $v_{DS}$  for both upper-side and lower-side, also, the value of  $v_{DS}$  for the voltage plateau in upper-side is higher than that of lower-side by about 50 V.

Table 3 shows the comparison about characteristics of  $v_{DS}$ . Under the condition of relatively high  $V_{DD}$ , the characteristics of  $v_{DS}$  are greatly affected by the module's structure. If the module's structures are same, the characteristics of  $v_{DS}$  will be the same, even if the power dies inside the modules are different from each other. On the other hand, if the structures of the modules are different, the characteristics of  $v_{DS}$  are deviated from each other even if the used power dies and their parallel number inside the modules both are same. In addition, the faster turn-on speed can further alter the characteristics of  $v_{DS}$ , so that the characteristic of Point\_1 for  $v_{DS}$  changing from  $\tau_1(\text{on})$  to  $\tau_2(\text{on})$  become less obvious.

**Table 3.** The comparison about characteristics of  $v_{DS}$  over number of turning points.

Number of Turning Points	Module_A	Module_B	Module_C	Module_D
High $V_{DD}$	2	2	1	1
Low $V_{DD}$	1	1	1	1 <sup>1</sup>

<sup>1</sup> There are characteristics of drain-source voltage plateau observed in module\_D.

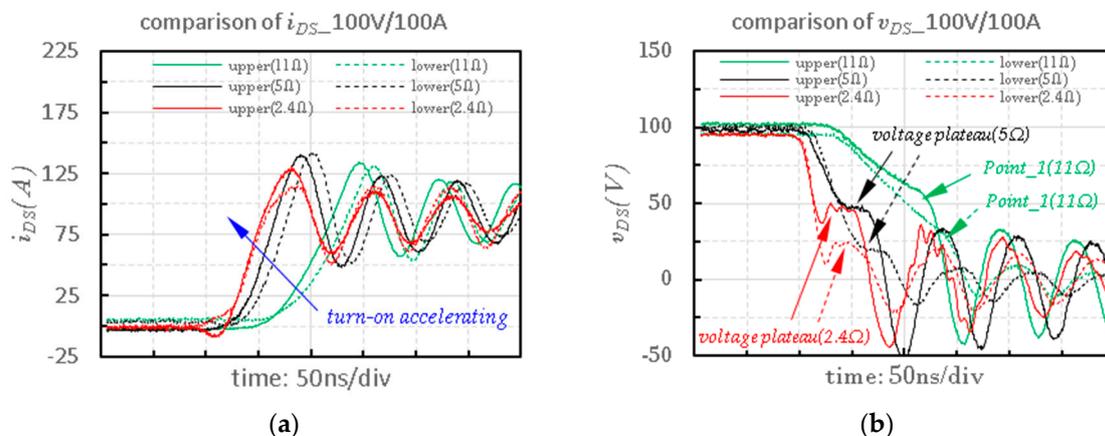
Under the condition of low  $V_{DD}$ , the difference of module's structures does not cause the significant different characteristics of  $v_{DS}$ , but the module design with faster turn-on speed causes the distinct characteristics of voltage plateau in  $v_{DS}$  between upper-side and lower-side of the module.

### 3.3. Turn-On Transient at Conditions of a Lower $V_{DD}$ and Various Turn-On Speed

Based on the qualitative comparison and analysis of experimental results shown in Figures 5–9, it can be supposed that the characteristics of voltage plateau shown from the  $v_{DS}$  waveforms at turn-on transient are due to the combined impacts of fast turn-on speed and low  $V_{DD}$  with a specific module structure.

In order to reveal the mechanisms behind the characteristics of the voltage plateau and the impacts of turn-on speed, test conditions and module structure, another experiment is carried out with module\_D, in which  $V_{DD}$  is fixed at a low value 100 V and the turn-on speed is controlled with three groups of external resistors ( $R_{gext}$ ).

Figure 10 shows the comparison of characteristics of  $v_{DS}$  among the various turn-on speeds by using different  $R_{gext}$ . The green, black, and red lines stand for the experimental results under the condition of  $R_{gext}$  equal to 11  $\Omega$ , 5  $\Omega$ , and 2.4  $\Omega$ , respectively, and the solid and dash lines stand for the upper-side and lower-side, respectively.



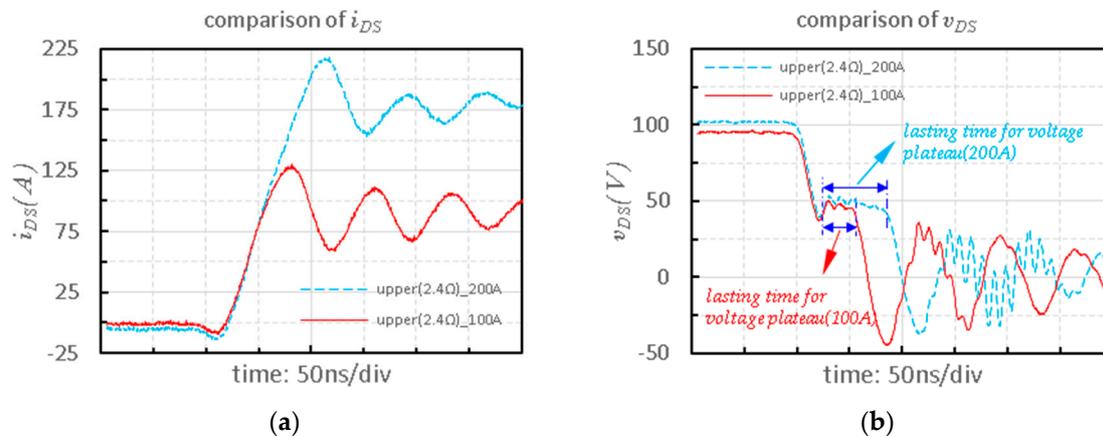
**Figure 10.** The comparison of turn-on transient waveforms of the module\_D among various turn-on speeds under condition of a lower  $V_{DD}$ : (a) waveform of  $i_{DS}$ , (b) waveform of  $v_{DS}$ .

From Figure 10, characteristics of voltage plateau in  $v_{DS}$  are observed for the cases of  $R_{gext}$  equals to 5  $\Omega$  and 2.4  $\Omega$ , in which the turn-on speed both are faster than 2.64 A/ns (this is turn-on speed of lower-side for the case of  $R_{gext}$  equals to 5  $\Omega$ ), the difference in value of the drain-source voltage plateau between upper-side and lower-side is almost same regardless of the rise of the turn-on speed, which is about 25 V.

In addition, the characteristic of Point\_1 is obvious for the case of  $R_{gext}$  equals to 11  $\Omega$ . Compared with the previous characteristics of negligible Point\_1 in  $v_{DS}$  shown in Figure 7b, it is further confirmed by experiment that the rise of the turn-on speed strengthens the influence of module's structure on the characteristics of  $v_{DS}$ .

Figure 11 shows that the load current ( $I_O$ ) has effect on characteristics of voltage plateau in  $v_{DS}$ , where the transient waveforms of the upper-side under the condition where  $V_{DD}$  is equal to 100 V,  $I_O$  is

equal to 200 A, and  $R_{gext}$  is equal to  $2.4 \Omega$  (dash lines with the color of light blue) are added together and aligned with time. It is disclosed that the increase in  $I_O$  just extends the lasting time of the voltage plateau for the characteristics of  $v_{DS}$ , it does not change the value of the voltage plateau.



**Figure 11.** The comparison of turn-on transient waveforms of the module\_D with an increased  $I_O$  under  $V_{DD}$  of 100 V: (a) waveform of  $i_{DS}$ , (b) waveform of  $v_{DS}$ .

In summary, for SiC high-power modules, the characteristics of  $v_{DS}$  are varied under combined conditions of multiple factors, such as the structure of the module, turn-on speed,  $V_{DD}$ , and  $I_O$ . The influence of the module's structure on the characteristics of  $v_{DS}$  is weakened as the  $V_{DD}$  reduces, and strengthened as the turn-on speed rises. If the turn-on speed is fast enough (e.g., more than 2.64 A/ns, as shown in previous experiments), under the condition of high  $V_{DD}$ , the characteristic of the turning point for  $v_{DS}$  changing from  $\tau_1$ (on) to  $\tau_2$ (on) during SiC-MOSFET dies operate in saturation region will become negligible, while under condition of low  $V_{DD}$ , the characteristic of voltage plateau will be observed in  $v_{DS}$ . Furthermore, the distinct characteristics of drain-source voltage plateau between the upper-side and lower-sides of the module are related to the combined impacts of fast turn-on speed and low DC bus voltage, as well as the different structures of the two sides inside the module.

#### 4. Simulation Study for Mechanism of Drain-Source Voltage Plateau

##### 4.1. Mechanism for Characteristic of Drain-Source Voltage Plateau

The  $v_{DS}$  of module\_D at turn-on transient is simulated by LTspice software. The diagram of the schematic circuit for simulation is shown in Figure 12. The parasitic inductance of drain circuit loop ( $L_D$ ) is also divided into two parts, which are  $L'_D$  and  $L''_D$ , respectively. The  $L'_D$  is the parasitic inductance belong to the partial path of drain circuit loop, which is shared with path between two test points for acquiring transient  $v_{DS}$ , while  $L''_D$  is the parasitic inductance related to the other part of the drain loop.

The simulation of the influence of the  $V_{DD}$  on voltage plateau is conducted based on the upper-side of module\_D. In simulation all the parameters and conditions are same with each other, except for the condition of  $V_{DD}$ , where  $V_{DD}$  is set to be 100 V, 200 V, 300 V, and 400 V, respectively. The value of the parasitic inductance related to the power module and DPT rig are extracted by Q3D software, which are listed in Table 4.

Table 4. Summary of the parasitic element of modules and DPT.

Parasitic Inductance of Paths or Routings	Symbol	Upper-Side	Lower-Side
Routings from terminals of DC+ and DC- inside module	$L_{D1}$ (nH)	16.46	16.46
Paths of drain circuit loop outside module in DPT	$L_{D2}$ (nH)	12.56	12.56
Common part of the routings, $L'_{D\_upper}$ and $L'_{D\_lower}$	$L'_D$ (nH)	7.95	5.14

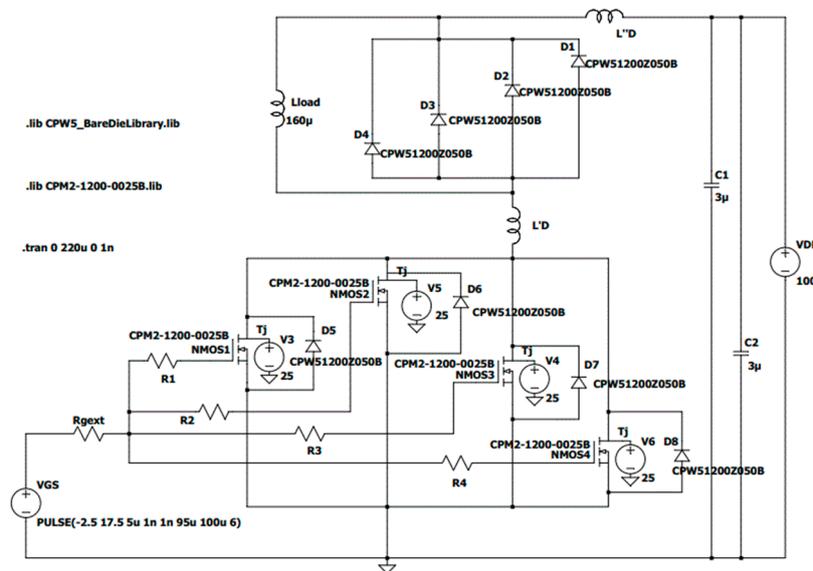


Figure 12. The diagram of schematic circuit for simulation by LTSpice.

Figure 13a shows that the characteristic of voltage plateau is observed as  $V_{DD}$  decreases ( $<300$  V) in simulation. The values of voltage plateau in condition of  $V_{DD}$  equals to 200 V and 100 V are about 100 V and 50 V, respectively. These simulation results about characteristics of voltage plateau in  $v_{DS}$  are in good agreement with the previous experimental results (Figures 9b and 10b).

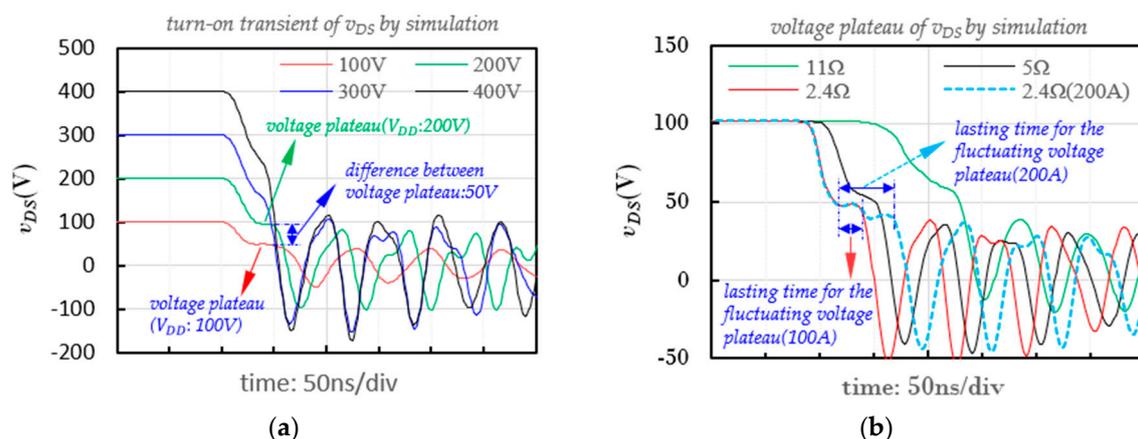


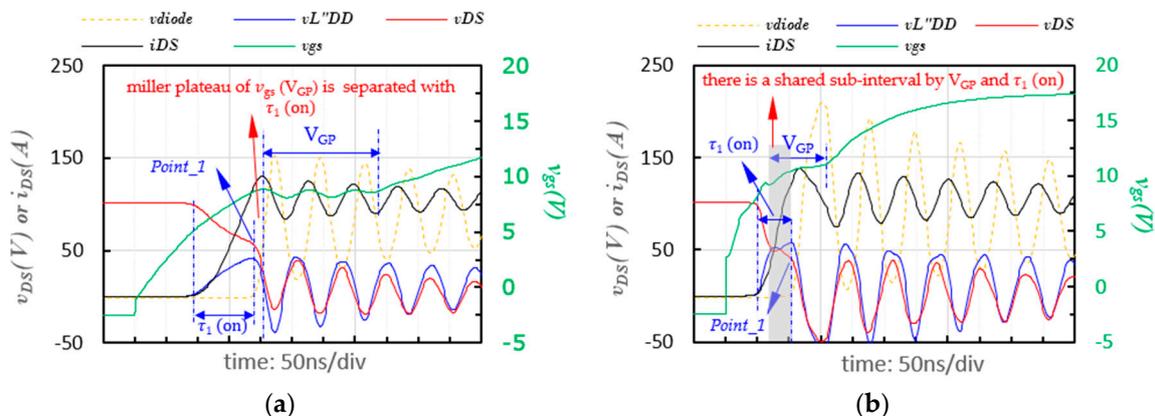
Figure 13. The simulation results about voltage plateau of  $v_{DS}$  for module\_D by LTSpice: (a) influence of  $V_{DD}$ , (b) influence of turn-on speed.

Figure 13b shows the simulation about the influence of rise of turn-on speed and  $I_O$  on characteristics of voltage plateau. The simulation conditions are same with that of experiments shown in Figures 10 and 11. With the rise of turn-on speed, the characteristic of voltage plateau emerges. The characteristic that the increased  $I_O$  does not change the value of voltage plateau and just increases the lasting time for the voltage plateau, which are also observed in simulation.

These simulation results about the characteristics of  $v_{DS}$  in voltage plateau agree with the experimental results. There is a little discrepancy of voltage fluctuation over voltage plateau between experiment (see dash line in light blue color in Figure 11b) and simulation (see the dash line in light blue color in Figure 13b). In the actual experiment the  $v_{DS}$  is forced into stage of voltage plateau, while the  $v_{DS}$  enters slowly stage of voltage plateau in simulation; secondly, the  $v_{DS}$  fluctuates over stage of voltage plateau more violently than that of simulations. This is due to the simplification of the simulation model, and some parasitic parameters or effects that may exist in actual experiment have not been considered.

Figure 14 shows that during the interval of  $\tau_1(on)$ , the  $V_{DD}$  and forward voltage drop of freewheeling diodes ( $V_{F\_diodes}$ ) are shared by  $L''_D$  and  $L'_D$ , and the transient voltage of these two parasitic inductance (which are  $v_{L''_D}$  and  $v_{DS}$ , respectively) are dependent on the slew rate of  $i_{DS}$ . The relationship is given by

$$V_{DD} + V_{F\_diodes} = (L'_D + L''_D) \frac{di_{DS}}{dt} \quad (3)$$

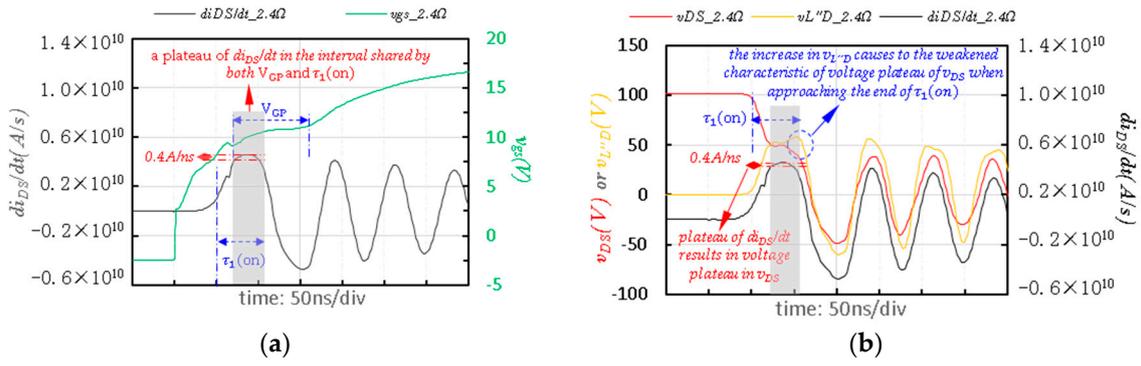


**Figure 14.** The simulation results about relationship between the  $\tau_1(on)$  of  $v_{DS}$  and miller plateau of  $v_{gs}$  under 100 V/100 A: (a) turn-on speed is slow ( $R_{gext} = 11 \Omega$ ), (b) turn-on speed is fast ( $R_{gext} = 2.4 \Omega$ ).

Before the interval of  $\tau_1(on)$ , the  $i_{DS}$  does not rise significantly, the  $v_{DS}$  is the sum of  $V_{DD}$  and  $V_{F\_diodes}$ , since the value of  $V_{F\_diodes}$  is about 1.3 V and the value of  $V_{DD}$  is several hundred volts, the value of  $v_{DS}$  is viewed as  $V_{DD}$ . During  $\tau_1(on)$ , the  $i_{DS}$  rises rapidly, the  $di_{DS}/dt$  also rise, accordingly, the voltage over the  $L''_D$  increase, as a result that the  $v_{DS}$  falls. After  $\tau_1(on)$ , the freewheeling diodes enter the reverse recovery process and start to regain the reverse voltage blocking capability. The voltage is clamped to the freewheeling diodes as shown by the dash line in orange color, accordingly, the  $v_{DS}$  shown by the solid-line in red color and the  $v_{L''_D}$  shown by the solid-line in blue color are collapsed.

When the turn-on speed is slow, as shown in Figure 14a, the miller plateau of  $v_{gs}$  ( $V_{GP}$ ) appears after  $\tau_1(on)$ , there is no any overlap between them. When turn-on speed is fast enough (e.g., more than 2.64 A/ns shown in previous experiments), as shown in Figure 14b, the interval of  $V_{GP}$  and  $\tau_1(on)$  have a shared sub-interval between them. This shared sub-interval in  $\tau_1(on)$  is a result caused by both fast turn-on speed and low  $V_{DD}$ .

In order to figure out the effect of this overlap between  $\tau_1(on)$  and GP on characteristics of drain-source voltage plateau, the simulation results about the slew rate of  $i_{DS}$  are analyzed in detail. Figure 15 shows that the  $di_{DS}/dt$  has a characteristic of plateau in this shared sub-interval by  $V_{GP}$  and  $\tau_1(on)$ . Since the tiny change in  $di_{DS}/dt$  (just 0.4 A/ns) in this shared sub-interval, the voltage over the inductance of  $L'_D$  changes by about 3.2 V in this shared sub-interval. Compared with the significant drop of  $v_{DS}$  in both the initial stage of  $\tau_1(on)$  and the whole  $\tau_2(on)$ , the falling of  $v_{DS}$  in this shared sub-interval is negligible, so that the characteristic of voltage plateau is observed in  $v_{DS}$ .



**Figure 15.** The simulation results about mechanism of drain-source voltage plateau under 100 V/100 A: (a) plateau  $di_{DS}/dt$ , (b) comparison of  $v_{L''D}$  and  $v_{DS}$ .

During the shared sub-interval by  $\tau_1(on)$  and GP, SiC-MOSFET dies operate in saturation region, where  $v_{gs} > V_{TH}$  and  $v_{DS} > (v_{gs} - V_{TH})$ , the drain-source current of SiC-MOSFET dies is given by

$$i_{DS} = g_{fs}(v_{gs} - V_{TH}) \quad (4)$$

where  $g_{fs}$  is trans-conductance of SiC-MOSFET dies. Derivate the Equation (4) from time, we can get

$$\frac{di_{DS}}{dt} = g_{fs} \frac{dv_{gs}}{dt} \quad (5)$$

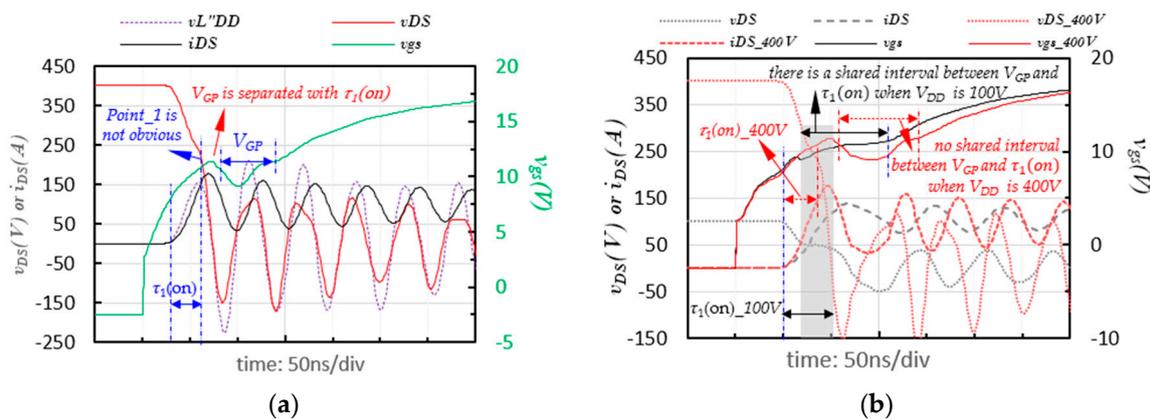
During the GP interval, the miller capacitance discharges firstly, then charges reversely by gate current, the most of gate current goes through  $C_{gd}$  instead of  $C_{gs}$ , hence, the voltage of  $C_{gs}$  rise so slowly and voltage plateau appears in  $v_{gs}$ , so that the  $dv_{gs}/dt$  varies little.

According to Equation (5), the  $di_{DS}/dt$  is determined by  $dv_{gs}/dt$  during the shared sub-interval by  $\tau_1(on)$  and GP, therefore, the  $di_{DS}/dt$  changes little and appear the characteristic of voltage plateau in  $v_{DS}$ .

After the moment corresponding to Point\_1, the freewheeling diodes enter the reverse recovery process and start to regain the reverse voltage blocking capability. Consequently, the voltage is clamped to the freewheeling diodes, so that the effect of  $V_{GP}$  on the  $di_{DS}/dt$  is not reflected on  $v_{DS}$ , therefore, the characteristics of drain-source voltage plateau will end at the moment when  $i_{DS}$  rises to  $I_O$ . However, if the  $I_O$  increases, this shared sub-interval will be extended, accordingly, the characteristics of voltage plateau in  $v_{DS}$  will also be prolonged.

As shown in Figure 15b, when approaching to the end of interval  $\tau_1(on)$ , with the change of  $di_{DS}/dt$  rises, the rise in voltage over  $L''_D$  results in the voltage over  $L'_D$  reduces, as a result that the characteristic of Point\_1 is weakened.

Figure 16 shows the simulation results about the influence of the increased  $V_{DD}$  on characteristics of voltage plateau in  $v_{DS}$ , where  $V_{DD}$  is set to be 400 V,  $R_{gext}$  is set to be 2.4  $\Omega$ , and  $I_O$  is set to be 100 A. The increased  $V_{DD}$  generates the higher  $di_{DS}/dt$  over the  $L_D$  during the conduction of freewheeling diodes, the freewheeling current in loop\_① transfer faster to loop\_②, on the other hand, the increased  $V_{DD}$  accelerates the turn-on, due to the smaller input parasitic capacitance under high  $v_{DS}$ , the  $v_{gs}$  can rise to a higher voltage then falls to miller plateau, this higher  $v_{gs}$  cause the current of SiC-MOSFETs rises in a higher speed. As shown in Figure 16b, the  $\tau_1(on)$  is shortened and  $V_{GP}$  is delayed, so that the interval of  $V_{GP}$  is separated with  $\tau_1(on)$ . As a result, the effect of miller plateau of  $v_{gs}$  on  $di_{DS}/dt$  is not reflected in characteristics of  $v_{DS}$ , the characteristics of voltage plateau is not developed in  $v_{DS}$ , furthermore, the characteristic of Point\_1 becomes less obvious.

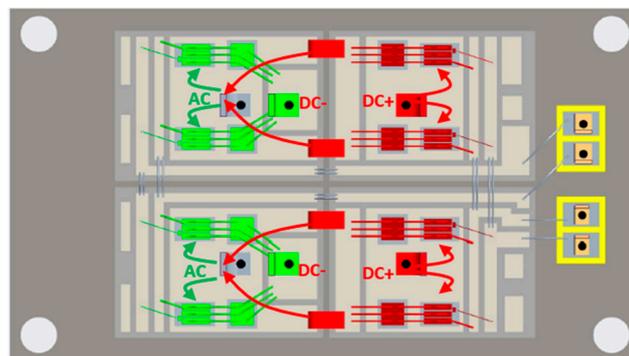


**Figure 16.** The simulation results about the influence of the increased  $V_{DD}$  on characteristics of drain-source voltage plateau: (a) voltage waveforms under condition of 400 V/100 A, (b) comparison between  $V_{DD}$  of 400 V (in red color) and 100 V (in black color).

#### 4.2. Mechanism for Difference of Drain-Source Voltage Plateau between Upper-Side and Lower-Side

The previous experimental results show us that the measured  $v_{DS}$  in voltage plateau for the upper-side is higher than that of lower-side by 50 V in  $V_{DD}$  of 200 V, and 25 V in  $V_{DD}$  of 100 V. This difference is related to the distinct parasitic inductance in measuring the  $v_{DS}$ . The physical outline and locations of power terminals for the developed module are fixed as shown in Figure 1. When measuring the  $v_{DS}$  of upper-side the test probe is connected to the power terminals of “DC+” and “AC”, while, when measuring the  $v_{DS}$  of the lower-side, the probe is connected to the terminals of “AC” and “DC-” in the DPT experiment.

Figure 17 illustrates the design of inner routings of the developed module\_D, the red-color indicated routings from terminal of “DC+” to terminal of “AC” and the related DBC (direct bonding copper) form the path of upper-side, while the green-color indicated routings from terminal of “AC” to terminal of “DC-” and the related DBC form the path of lower-side when measuring  $v_{DS}$ . The path of upper-side is significantly different from the one of the lower-side inside the module when measuring  $v_{DS}$ .

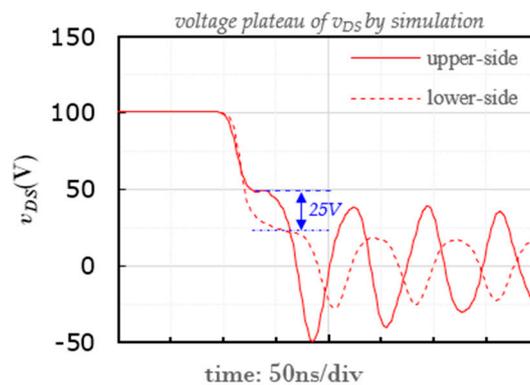


**Figure 17.** Design of routings inside in module\_D (red lines for upper-side; green line for lower-side).

The path of drain circuit loop inside module\_D consists of the routings from terminal of “DC+” to terminal of “DC-” and the related DBC. It is obvious that the partial path of drain circuit loop shared with the path of upper-side is different from the one shared with the path of lower-side inside the module. The parasitic inductance of these shared paths between upper-side and lower-side are also different from each other, which is denoted by the  $L'_{D\_upper}$  and  $L'_{D\_lower}$ , respectively. The value of the  $L'_{D\_upper}$  and  $L'_{D\_lower}$  were extracted by Q3D software, as shown in Table 4, in which the value of  $L'_{D\_upper}$  is higher than that of  $L'_{D\_lower}$ .

Based on the circuit schematic shown in Figure 12 and the distinct  $L'_D$  which is the  $L'_{D\_upper}$  for upper-side and  $L'_{D\_lower}$  for lower-side, the turn-on transient waveforms of  $v_{DS}$  for module\_D are simulated by LTspice under the condition that the  $V_{DD}$  is set to be 100 V, the  $I_O$  is set to be 100 A, and the  $R_{gext}$  is set to be 2.4  $\Omega$ . The other parameters for simulation are the same as that of the experiments shown in Figure 10 and Table 2, as well as Table 4.

Figure 18 shows the simulation result about the difference of characteristics of drain-source voltage between upper-side and lower-side caused by the special structure of the module. The characteristics of voltage plateau in  $v_{DS}$  are observed in both the upper-side and lower-side. The simulation results about the difference in the values of drain-source voltage plateau between the upper-side and lower-side is very near to the experimental result of 25 V shown in Figure 10b.



**Figure 18.** The simulation results about difference of drain-source voltage plateau between upper-side and lower-side by LTspice.

Though the voltage plateau of  $v_{DS}$  in the lower-side is not as flat as that of the upper-side and has a slow downward trend, there is difference of characteristics of  $v_{DS}$  in the lower-side between experiment and simulation. We can see the similar characteristic in previous experiment shown in dash line in black color for lower-side under condition of  $R_{gext}$  equals to 5  $\Omega$  in Figure 10b. Therefore, the characteristic of voltage plateau in  $v_{DS}$  for the lower-side in simulation is normal, while the discrepancy in voltage plateau characteristic for  $v_{DS}$  of the lower-side between the experiment and simulation is probably attributed to the difference of test conditions caused by the simplification of the simulation.

In summary, the experimental results are confirmed by simulation that the combined impacts of fast turn-on speed and low  $V_{DD}$  causes characteristic of voltage plateau in  $v_{DS}$  at turn-on transient. Moreover, the special structure design of the developed module with the standard 62 mm package outline between upper-side and lower-side lead to different characteristics of characteristic of voltage plateau in  $v_{DS}$  of each other. The characteristic that the rise of  $I_O$  does not change the value of voltage plateau and just prolongs the voltage plateau is also confirmed by simulation.

The voltage plateau happens at different  $v_{DS}$  values for the upper-side and lower-side, which is verified by simulation. The difference is attributed to the discrepancy of structure in the corresponding partial path of drain circuit loop inside SiC high-power module with the standard 62 mm package outline when measuring  $v_{DS}$  of upper-side and lower-side.

## 5. Conclusions

In this work, the characteristics of drain-source voltage at turn-on transient for the fabricated SiC high power modules are investigated under various test conditions (i.e., various DC bus voltages and turn-on speeds), and the characteristic of the drain-source voltage plateau is observed under the combined condition of fast turn-on speed and low DC bus voltage. The mechanisms behind the voltage plateau characteristics are studied via experiments and simulations.

Under the condition of fast turn-on speed and low DC bus voltage, there is a shared sub-interval by the interval of miller plateau for gate-source voltage and the interval of  $\tau_1(on)$  for drain-source voltage,

the effect of miller plateau of gate-source voltage on  $di_{DS}/dt$  can be reflected in the characteristics of the drain-source voltage, so that the characteristic of the voltage plateau is generated in the drain-source voltage during  $\tau_1(on)$ . After  $\tau_1(on)$ , the voltage is clamped to the freewheeling diodes, the  $v_{DS}$  falls dramatically, the characteristic of voltage plateau in drain-source voltage disappears. In addition, with the load current ( $I_O$ ) increases, the shared sub-interval is prolonged, accordingly, the lasting time for the characteristics of voltage plateau in drain-source voltage is also increased.

When the turn-on speed is slow, the miller plateau of gate-source voltage ( $V_{GP}$ ) appears after  $\tau_1(on)$ , there is no any overlap between them. The effect of miller plateau of gate-source voltage on  $di_{DS}/dt$  is not reflected on the characteristics of drain-source voltage, therefore, the characteristics of the voltage plateau are not developed in the drain-source voltage.

When the DC bus voltage is high, the increased  $V_{DD}$  shortens the interval of  $\tau_1(on)$  and delays the interval for the miller plateau of gate-source voltage, so that the interval for the miller plateau of gate-source voltage is separated with  $\tau_1(on)$ , as a result that the characteristic of voltage plateau is not developed in drain-source voltage.

In summary, the experimental results are confirmed by simulation that the combined impacts of fast turn-on speed and low DC bus voltage causes the characteristic of voltage plateau in the drain-source voltage at the turn-on transient. Moreover, the different structure designs of the developed module with the standard 62 mm package outline between the upper-side and lower-side lead to different values of  $v_{DS}$  from each other in the voltage plateau.

**Author Contributions:** Conceptualization, M.Z.; funding acquisition, Q.G. and K.S.; project administration, Q.G.; supervision, K.S.; writing—original draft, M.Z.; writing—review and editing, M.Z., and N.R.; All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was supported in part by the National Key Research and Development Program of China under Grant 2018YFB0905700, and in part by the National Natural Science Foundation of China under Grant 51777187 and U1766222.

**Conflicts of Interest:** The authors declare no conflict of interest.

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