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Research on the Equivalent Virtual Space Vector Modulation Output of Diode Clamped *N*-level Converter under Multi-Modulation Carrier Modulation

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Abstract: Diode-clamped multi-level converters have DC-side capacitors in series, which will lead to the unbalance of DC-side capacitor voltage, the distortion of the output waveform, the increase of total harmonic distortion (THD), and even the damage of switching devices, which will make the system inoperable. The proposal of virtual space vector pulse-width modulation (VSVPWM) realizes the balanced control of the capacitor voltage, but when the output level of converter increases, the implementation of VSVPWM becomes very complicated, and the amount of calculation also increases greatly, thus hindering its application in the multi-level circuit. Compared with VSVPWM, the carrier-based pulse-width modulation (CBPWM) is simple to operate and easy to implement. If the equivalent relationship between CBPWM and VSVPWM can be found, the application of VSVPWM can be generalized to any level, and the advantages of VSVPWM can be fully utilized. This paper aims to study the inner relationship of VSVPWM and the multi-modulation carrier CBPWM (MCBPWM). After strict theoretical analysis, the equivalent relationship of VSVPWM and MCBPWM in the three-level and four-level and converter is realized by injecting the zero-sequence component into the modulation waves. Furthermore, the equivalent relationship between VSVPWM and MCBPWM is deduced to the *N*-level converter. Finally, the correctness of the relevant theoretical analysis is verified by the experiment.

Keywords: virtual space vector modulation (VSVPWM); decomposing modulation wave; zero-sequence component

1. Introduction

In recent years, the diode-clamped multi-level converter has been widely used in many fields due to its low switching stress and low harmonic distortion rates [1], such as power system DC transmission [2], reactive power compensation [3], active power filter and frequency conversion speed regulation of high-voltage high-power AC motor, etc. However, because the DC side capacitors of the converter are connected in series, the DC side voltage will be unbalanced [4]. Virtual space vector pulse-width modulation (VSVPWM) was first proposed for the capacitor voltage balance of three-level neutral-point-clamped (NPC) converters [5]. Through VSVPWM, the neutral current of the DC side is zero during the switching cycle, and the voltage of the capacitor can be well balanced within the range of full modulation and load power factor [6–8]. However, when the levels of diode-clamped multi-level converters increase, the implementation of VSVPWM is very complicated, and the amount of calculation will greatly increase, hindering its application in multi-level circuits.

Therefore, VSVPWM is mainly used in three-level converter and when the level of the converter is greater than three levels, VSVPWM is rarely used. Compared with VSVPWM, the carrier-based pulse-width modulation (CBPWM) method appears earlier, it is easy to operate and implement [9,10], which is convenient for use in multi-level converters with greater than five levels, the theoretical and practical research has been relatively mature and widely used in practice. If the equivalent relationship between CBPWM and VSVPWM can be found, the modulation effect of VSVPWM can be realized by a simple and easy-to-implement CBPWM method, the application of VSVPWM can be extended to any level, and the advantages of VSVPWM can be fully utilized.

Reference [10] first proposed the three-phase three-level VSVPWM to realize the inverter neutral line non-current. In references [11,12], the realization of four-level and five-level VSVPWM are mainly deduced based on three-level. It is not difficult to find that with the increase of levels, the VSVPWM becomes particularly complex and difficult to be applied in higher-level situations. In references [13,14], the equivalent relationship between the CBPWM and SVPWM modulation strategies is preliminarily analyzed, and the three-level eight-segment modulation sequence is derived. By injecting a zero-sequence voltage into each phase modulation voltage under CBPWM, the modulation effect of the two is equivalent. However, this method is limited to eight-segment modulation, and the output level of each phase can only be two levels. Reference [15] achieves the equivalent relationship between space vector pulse-width modulation (SVPWM) and CBPWM of single-phase three-level NPC converters by injecting offset voltage, however, it only studies the single-phase three-level converter and there is no study on three-phase or higher-level converters. Reference [16] proposed a brand-new modulation wave decomposition strategy, which makes the decomposition of more than eight-segment space vector output sequences possible, perfecting the realization of the equivalent relationship. However, it only studies a three-level converter and does not study higher-level output converters. Reference [17] studies an equivalent relationship between SVPWM and CBPWM of the n-level converter, it assumes the DC side voltage of the converter is constant and does not consider the unbalance of DC side capacitors. Therefore, there is no modulation strategy used to solve the neutral current generated by the voltage vector. References [18,19] analyzed the three-phase three-level virtual space vectors. By solving the volt-second balance and the boundary condition equations, the equivalence between the three-phase dual-modulated wave CBPWM and VSVPWM 10-segment sequences was realized. However, it does not study how the command voltage modulated wave is decomposed into double modulated waves and does not give the expression of the zero-sequence component of the equivalent relationship. Moreover, the equivalent relationship between VSVPWM and CBPWM above three levels has not been studied. In addition, as the number of levels increases, the number and difficulty of solving equations will greatly increase, which is not conducive to promotion to multiple levels. Therefore, through the analysis of domestic and foreign references, there is no reference to study the equivalent relationship between CBPWM and VSVPWM of NPC multi-level converter with arbitrary output levels. Once the equivalent relationship of two is found, the equivalent output of VSVPWM can be realized by CBPWM, which can not only simplify the complex calculation but is also easy to implement in higher-level converters with low switching stress and low harmonic distortion rates.

In this paper, the relationship between VSVPWM and multi-modulation carrier CBPWM (MCBPWM) of NPC three-level, four-level, and five-level converters is analyzed in detail. After strict theoretical derivation, the zero-sequence components that achieve the equivalent of VSVPWM and MCBPWM are obtained, and the equivalence of VSVPWM and MCBPWM at any level is deduced. Finally, through the experiment, the correctness of the research on the equivalent relationship between VSVPWM and MCBPWM modulation is verified.

2. VSVPWM Modulation Principle of Diode Clamped Multi-Level Converter

Taking $n = 3$ as an example to introduce the implementation process of VSVPWM. Figure 1 shows a three-level space vector diagram with six sectors, the total output of the converter is 27 switching

states with 19 voltage vectors, which are divided into zero vector (V_0), small vector (V_{S1}~V_{S6}), medium vector (V_{M1}~V_{M6}) and large vector (V_{L1}~V_{L6}). The neutral current generated by each switch state of each voltage vector as shown in [], and it can be seen that the zero vector and the large vector do not affect the midpoint voltage of the DC side capacitor, while the two switches of the small vector have the opposite effect on it. Besides, the medium vector will also generate a neutral current. In order to realize the voltage balanced control of the midpoint of the DC-side capacitor during the stable state, the new virtual medium vector and virtual small vector are defined. Take the A-sector as an example, as shown in Figure 2, the sector is re-divided into five sub-sectors, i.e., A_1~A_5. The corresponding relationship between the virtual vectors in Figure 2 and vectors in Figure 1 is as follows:

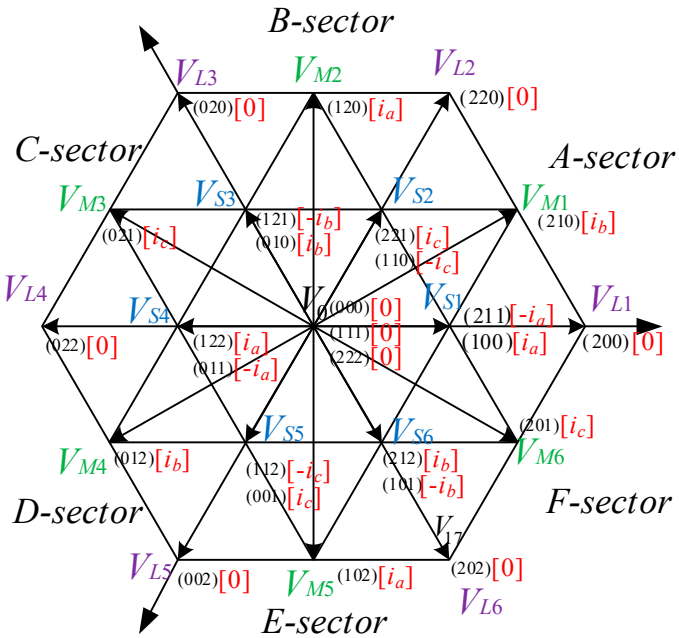


Figure 1. Space vector distribution of three-level converter.

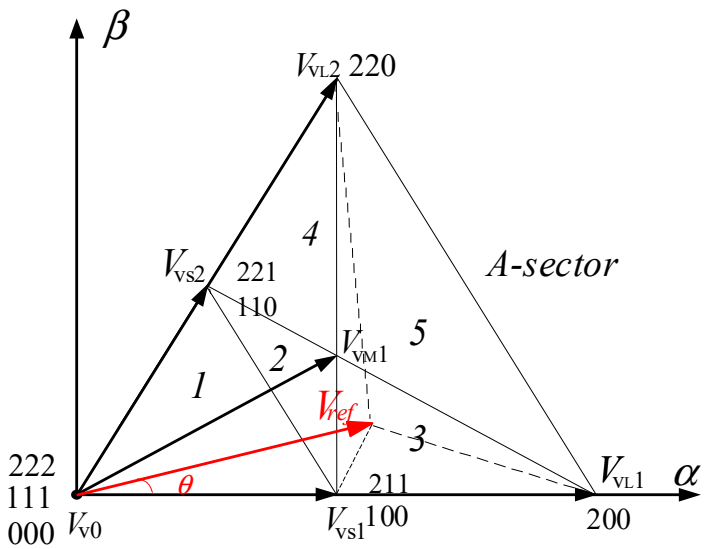


Figure 2. Space vector distribution of the three-level virtual space vector A sector.

(1) Virtual small vector. The virtual small vector is composed of a pair of redundant small vectors in the basic vector. The positive and negative small vectors each occupy half of the length and have the same action time. The virtual small vectors are constructed as follows:

$$\begin{cases} V_{VS1} = 1/2 \times (V_{S1(211)} + V_{S1(100)}) \\ V_{VS2} = 1/2 \times (V_{S2(221)} + V_{S2(110)}) \end{cases} \tag{1}$$

(2) Virtual medium vector. The virtual medium vector is composed of one medium vector in the basic vector and two different small vectors adjacent to the medium vector. Each length is 1/3, and the action time is equal. In this way, as shown in Figure 1, the currents (i_a + i_c) generated by the switch state (100) and (221) of small vector and the current i_b generated by the switch state (210) of medium vector cancel each other, the neutral current is zero, thereby achieving balanced control of the midpoint voltage of the capacitor. The construction equation of the virtual medium vector is:

$$V_{VM1} = 1/3 \times (V_{S1(100)} + V_{S2(221)} + V_{M1(210)}) \tag{2}$$

(3) Virtual large vector and virtual zero vector. The large and zero vectors in Figure 1 will not affect the midpoint current, so the virtual large and zero vectors can be directly replaced with the large and zero vectors in the basic vector.

Using the synthesized virtual medium vector instead of the medium vector in the original space vector diagram, the average neutral current of the multi-level topology converter in the unit switching cycle is zero when the connected load or grid is symmetrical, which will not cause the imbalance of the DC side capacitor voltage.

Similarly, for the four-level virtual space vector, as shown in Figure 3, the A sector is divided into 13 small sub-sectors, 11 new virtual vectors V_1~V_{11} are defined. All these virtual vectors do not affect the midpoint voltage of the DC side capacitor, among which V_5, V_6, and V_9 have two redundant states:

$$\begin{cases} V_{5,1} = 1/2 \times (V_{311} + V_{100}) \\ V_{5,2} = 1/2 \times (V_{322} + V_{200}) \end{cases} \tag{3}$$

$$\begin{cases} V_{6,1} = 1/2 \times (V_{331} + V_{110}) \\ V_{6,2} = 1/2 \times (V_{332} + V_{220}) \end{cases} \tag{4}$$

$$\begin{cases} V_{9,1} = \frac{1}{3}V_{331} + \frac{1}{3}V_{310} + \frac{1}{3}V_{100} \\ V_{9,2} = \frac{1}{3}V_{332} + \frac{1}{3}V_{320} + \frac{1}{3}V_{200} \end{cases} \tag{5}$$

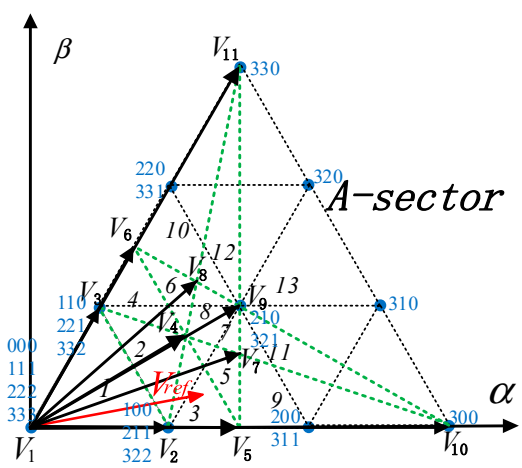


Figure 3. Space vector distribution of four-level virtual space vector A sector.

Define three variables x_5, x_6 and x_9 as the redundant state allocation coefficients of the virtual space vectors V_5, V_6 and V_9. The value range is [0, 1]. Then:

$$\begin{cases} V_5(x_5) = x_5 \cdot V_{5,1} + (1 - x_5) \cdot V_{5,2} \\ V_6(x_6) = x_6 \cdot V_{6,1} + (1 - x_6) \cdot V_{6,2} \\ V_9(x_9) = x_9 \cdot V_{9,1} + (1 - x_9) \cdot V_{9,2} \end{cases} \tag{6}$$

The definition of a multi-level virtual space vector above four levels is the same as that of four levels, which defines more virtual space vectors and more redundant states, but all of them meet the basic requirement that the neutral current of the converter is zero. The division of the first sector of the virtual space vector graph of five-level and N-level is shown in Figures 4 and 5.

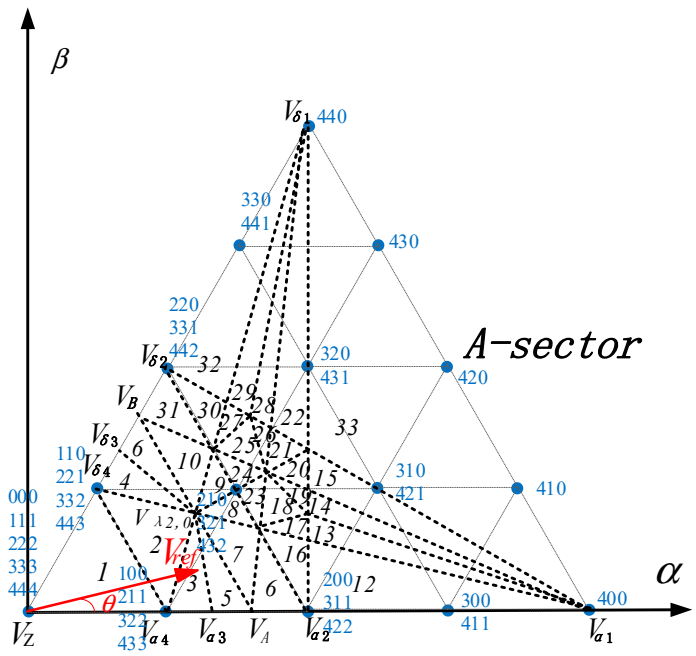


Figure 4. Space vector distribution of five-level virtual space vector A sector.

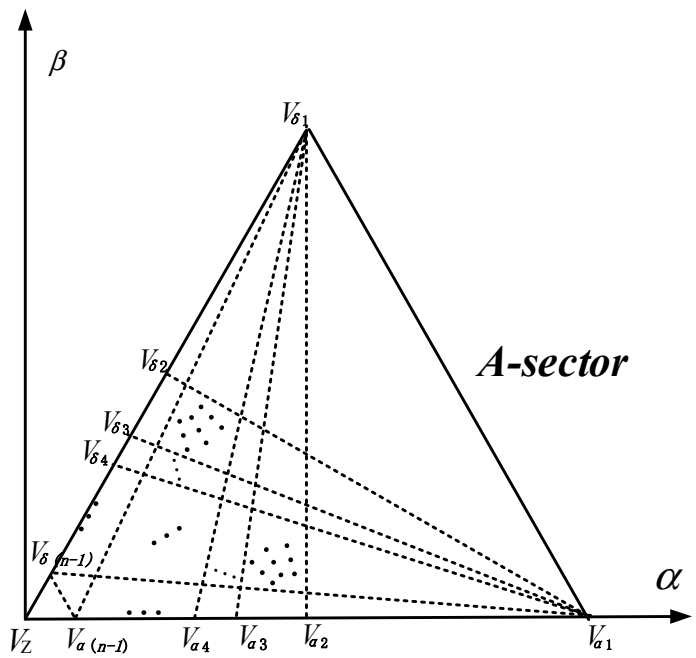


Figure 5. Space vector distribution of n-level virtual space vector A sector.

In Figure 2, firstly, according to the command voltage vector to determine the number of the sub-sector, then using the adjacent three virtual vectors to compose the command voltage vector. Taking the three-level topology as an example, since the switch state of each virtual vector is determined, the modulation sequence and action time within the unit switch cycle are also determined, as shown in Table 1.

Table 1. Three-level A-sector virtual space vector modulation sequence.

Sector	Modulation Sequence
A1	100→110→111→211→221→221→211→111→110→100
A2	100→110→210→211→221→221→211→210→110→100
A3	100→200→210→211→221→221→211→210→200→100
A4	100→110→210→220→221→221→220→210→110→100
A5	100→200→210→220→221→221→220→210→200→100

For the implementation of n-level VSVPWM, as the number of levels increases, the redundant switching states of some virtual voltage vectors also increases, so the switching sequence of the modulation output is not unique. If all switching states are used, i.e., the redundant state allocation coefficients x_i of virtual space vectors V_i are not equal to 0 or 1, the sequence of the n-level converter modulated with VSVPWM method in any sub-sector is $2(3n-4)$ segments. Taking the A_3 sub-sector as an example, the final output symmetric modulation sequence is: 100→200→210→211→ . . . $\rightarrow m(m-2)(m-2)\rightarrow m(m-1)(m-2)\rightarrow m(m-1)(m-1)\rightarrow$ . . . $\rightarrow n(n-2)(n-2)\rightarrow n(n-1)(n-2)\rightarrow n(n-1)(n-1)\rightarrow nn(n-1)\rightarrow n(n-1)(-1)\rightarrow n(n-1)(n-2)\rightarrow n(n-2)(n-2)\rightarrow$ . . . $\rightarrow m(m-1)(m-1)\rightarrow m(m-1)(m-2)\rightarrow m(m-2)(m-2)\rightarrow$ . . . →211→210→200→100.

3. The Essential Relationship between Diode Clamp Multi-Level Converter VSVPWM and MCBPWM

3.1. The Equivalent of Three-Level VSVPWM Modulation and MCBPWM Modulation

It can be seen from Table 1 that the modulation sequence of three-level VSVPWM in each sub-sector is 10 segments, but the traditional CBPWM can only output two levels per phase, and three-phase can output up to eight segments in the modulation sequence, so the traditional CBPWM modulation method cannot solve the above problem. This paper refers to the principle of modulation wave decomposition in reference [16] and decomposes n-level modulation waves into $(n-1)$ sub-modulation waves, so as to realize the output of multiple voltage states per phase. Assuming that the initial value of the modulated wave is V_a*, and the number of levels is $n = 5$, four conventional CBPWM modulated waves V_{a1}*, V_{a2}*, V_{a3}* and V_{a4}* are obtained after decomposition, as shown in Figure 6. Then the same output as the modulated wave V_a* can be achieved by the superposition of the output of the four conventional CBPWM modulation waves. Each sub-modulation wave intersects with the four in-phase stacked carriers respectively. After the superposition, the voltage of each phase contains five levels.

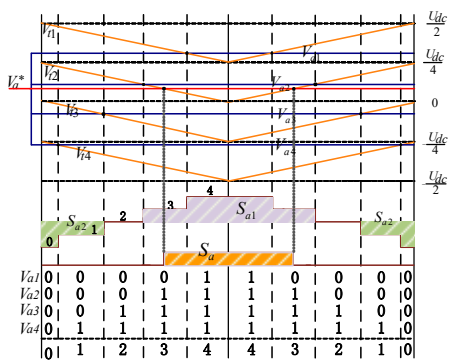


Figure 6. Obtaining of the sub-modulation waves.

Taking the three-level VSVPWM sub-sector A_3 as an example, in one switching cycle, phase A and phase C output two levels respectively, and phase B output three-level states of 0, 1, and 2, so it is necessary to decompose the B-phase modulation wave. Set the initial value of the B-phase modulation wave is V_b, and the values after decomposition are V^*_{b1} and V^*_{b2}. In Figure 7, the effect of the three-level output of the B-phase modulation wave within one switching cycle can be achieved by the superposition of conventional CBPWM sub-modulation waves V^*_{b1} and V^*_{b1}, through the modulation wave decomposition strategy, the output of multiple levels per switching period is realized.

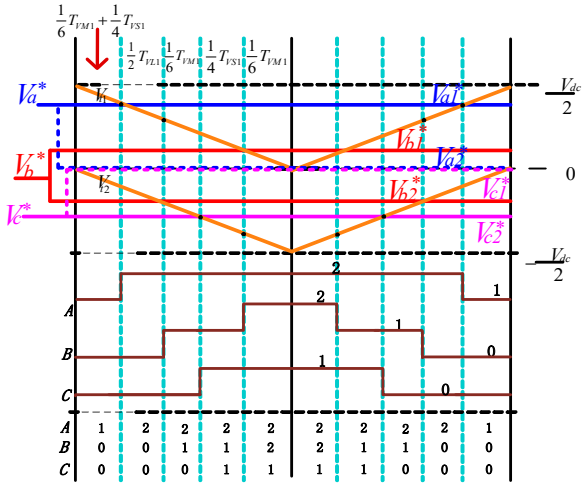


Figure 7. Relationship between three-level virtual space vector pulse-width modulation (VSVPWM) modulation sequence and multi-modulation carrier-based pulse-width modulation (MCBPWM) modulation.

VSVPWM is equivalent to injecting the zero-sequence component into the Multi-modulation carrier CBPWM (MCBPWM) to obtain the same output waveform as VSVPWM. By obtaining the zero-sequence component, the equivalent relationship of the switching sequence between the VSVPWM and the MCBPWM can be obtained. At this time, the sub-modulation waves obtained by the decomposition of the B-phase initial modulation waves can directly control the on-off state of the B-phase switch tubes. It can be seen from Table 1 that the VSVPWM modulation output in sector A_3 is a 10-segment symmetric modulation sequence: 100→200→210→211→221→221→211→210→200→100. The action time of each switch state of the virtual space vector is shown in Figure 7, where, V^*_a, V^*_b and V^*_c are three-phase MCBPWM modulation waves, V^*_{t1} and V^*_{t2} are triangular carrier waves. Next, the relationship between MCBPWM and VSVPWM is derived through strict theoretical calculation.

In Figure 2, the vectors in the A_3 area can be synthesized by the adjacent virtual vectors V_{VS1}, V_{VM1} and V_{VL1}, the virtual vector action times are T_{VS1}, T_{VM1}, and T_{VL1}, respectively, which satisfy $T_S = T_{VS1} + T_{VM1} + T_{VL1}$. According to Equations (1) and (2), the small vector V_{S1} (100) constitutes the virtual vector V_{VS1} and V_{VM1}, then the action time of the small vector V_{S1} (100) in a switching cycle is: $T_{S1} = T_{VS1}/2 + T_{VM1}/3$. Considering the symmetry of the space vector modulation sequence in a switching cycle, the action time of the small vector V_{S1} (100) in the first half of the switching cycle in Figure 7 is: $T_{S1} = T_{VS1}/4 + T_{VM1}/6$, the action time analysis of other vectors is similar.

In Figure 7, in a switching cycle, according to the volt-second balance principle:

$$\begin{cases} \left(\frac{1}{2}T_{VS1} + \frac{1}{3}T_{VM1} + 2T_{VL1} + \frac{1}{3}T_{VM1} + \frac{1}{2}T_{VS1}\right)\frac{V_{dc}}{2} = T_s \cdot V_{ab} \\ \left(\frac{1}{3}T_{VM1} + \frac{1}{3}T_{VM1}\right)\frac{V_{dc}}{2} = T_s \cdot V_{bc} \end{cases} \tag{7}$$

Considering $T_{VS1} + T_{VM1} + T_{VL1} = T_S$:

$$\begin{cases} T_{VL1} = (\frac{V_{bc}/2+V_{ab}}{V_{dc}/2} - 1) \cdot T_S \\ T_{VM1} = \frac{3}{2}\frac{V_{bc}}{V_{dc}/2} \cdot T_S \\ T_{VS1} = (2 - \frac{2V_{bc}+V_{ab}}{V_{dc}/2}) \cdot T_S \end{cases} \tag{8}$$

According to the relevant characteristic of similar triangles, there are:

$$\begin{cases} \frac{\frac{V_{dc}}{2}-V^*_{a1}}{\frac{V_{dc}}{2}} = \frac{\frac{1}{3}T_{VM1}+\frac{1}{2}T_{VS1}}{T_S} \\ V^*_{a2} = 0 \\ \frac{V^*_{b1}}{\frac{V_{dc}}{2}} = \frac{\frac{1}{3}T_{VM1}}{T_S} \\ \frac{0-V^*_{b2}}{\frac{V_{dc}}{2}} = \frac{\frac{1}{3}T_{VM1}+\frac{1}{2}T_{VS1}+T_{VL1}}{T_S} \\ V^*_{c1} = 0 \\ \frac{V^*_{c2}+\frac{V_{dc}}{2}}{\frac{V_{dc}}{2}} = \frac{\frac{1}{3}T_{VM1}+\frac{1}{2}T_{VS1}}{T_S} \end{cases} \tag{9}$$

The value of the two sub-modulated waves in each phase of the three phases is as follows:

$$\begin{cases} V^*_{a1} = \frac{1}{2} \times V_a - \frac{1}{2} \times V_c \\ V^*_{a2} = 0 \\ V^*_{b1} = \frac{1}{2} \times V_b - \frac{1}{2} \times V_c \\ V^*_{b2} = -\frac{1}{2} \times V_a + \frac{1}{2} \times V_b \\ V^*_{c1} = 0 \\ V^*_{c2} = \frac{1}{2} \times V_c - \frac{1}{2} \times V_a \end{cases} \tag{10}$$

Substituting Equation (10) into equation $V^*_x = V^*_{x1} + V^*_{x2} (x = a, b, c)$:

$$\begin{cases} V^*_a = V_a + V_z \\ V^*_b = V_b + V_z \\ V^*_c = V_c + V_z \\ V_z = -\frac{1}{2} \times V_a - \frac{1}{2} \times V_c \end{cases} \tag{11}$$

Based on the equivalent relationship of the three-level VSVPWM and MCBPWM, three-phase multiple sub-modulation waves of Equation (10) with the CBPWM method can achieve the same output effect as VSVPWM. By comparing each sub-modulated wave and the corresponding triangular carrier directly to determine the on-off status of each switch tube, MCBPWM modulation strategy simplifies the modulation process and reduces the amount of calculation.

In the other sub-sectors of A-sector, the same zero-sequence component as in Equation (11) is obtained. Let V_{max}, V_{mid}, and V_{min} represent the maximum, middle, and minimum of the modulation waves in the original phase A, B, and C respectively. Through the same derivation method, in other large sectors (B~F) of the diode clamped multi-level hexagonal space vector diagram, injecting the zero-sequence component obtained by the decomposition of the modulation wave into the three-phase modulation wave, the equivalent relationship of the three-level 10-segment VSVPWM and MCBPWM can be achieved. The expression of the zero-sequence component can be simplified as follows:

$$V_z = -\frac{1}{2}(V_{\max} + V_{\min}). \tag{12}$$

The expressions sub-modulation waves of each phase are as follows:

$$\begin{cases} V^*_{\max 1} = \frac{1}{2} \times V_{\max} - \frac{1}{2} \times V_{\min} \\ V^*_{\max 2} = 0 \\ V^*_{mid1} = \frac{1}{2} \times V_{mid} - \frac{1}{2} \times V_{\min} \\ V^*_{mid2} = -\frac{1}{2} \times V_{\max} + \frac{1}{2} \times V_{mid} \\ V^*_{\min 1} = 0 \\ V^*_{\min 2} = \frac{1}{2} \times V_{\min} - \frac{1}{2} \times V_{\max} \end{cases} \tag{13}$$

3.2. The Equivalent of Four-Level VSVPWM Modulation and MCBPWM Modulation

When n = 4, the four-level virtual space vector diagram is divided into 13 small sectors in the first sector. Unlike the three-level, there is more than one synthesis method for the newly synthesized four-level virtual space vector. As mentioned above, take the A_3 sub-sector in the first sector of the four-level virtual space vector diagram as an example, the required reference vector V_{ref} is synthesized by V_2, V_4 and V_5, and V_5 contains a redundant state whose allocation factor is represented by x_5, so the output 16-segment modulation sequence is: 100→200→210→211→311→321→322→332→332→322→321→311→211→210→200→100, as shown in Figure 8.

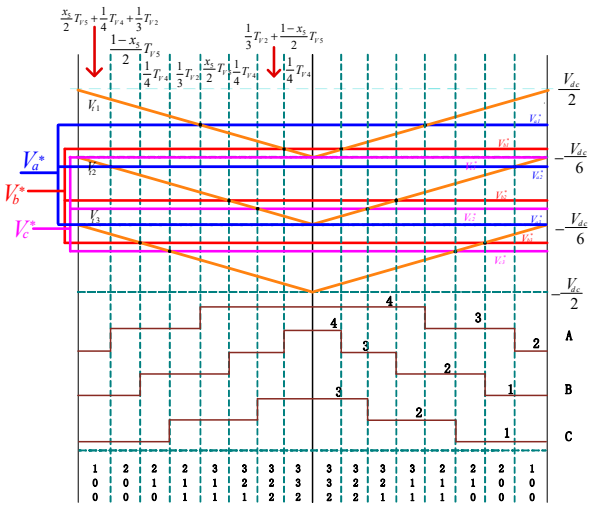


Figure 8. The relationship between the four-level A3 sector space vector pulse-width modulation (SVPWM) full switching sequence and the MCBPWM modulation.

Similar to the analysis in Section A, the expressions of three-phase four sub-modulated waves can be obtained as follows:

$$\begin{cases} V^*_{a1} = \frac{1}{3}V_{ac} + \frac{1}{6}V_{dc} \\ V^*_{a2} = \frac{2}{3}V_{ac} - \frac{1}{3}(x_5+1)V_{bc} - x_5 V_{ab} + \frac{2x_5-1}{6}V_{dc} \\ V^*_{a3} = -\frac{1}{6}V_{dc} \end{cases} \\ \begin{cases} V^*_{b1} = \frac{1}{3}V_{bc} + \frac{1}{6}V_{dc} \\ V^*_{b2} = -\frac{2}{3}V_{ac} + (1-x_5)V_{ab} + \frac{1}{3}(3-x_5)V_{bc} + \frac{2x_5-1}{6}V_{dc} \\ V^*_{b3} = -\frac{1}{3}V_{ab} - \frac{1}{6}V_{dc} \end{cases} \\ \begin{cases} V^*_{c1} = \frac{1}{6}V_{dc} \\ V^*_{c2} = -\frac{2}{3}V_{ac} + (1-x_5)V_{ab} + \frac{2-x_5}{3}V_{bc} + \frac{2x_5-1}{6}V_{dc} \\ V^*_{c3} = -\frac{1}{3}V_{ac} - \frac{1}{6}V_{dc} \end{cases} \tag{14}$$

According to $V_x^* = V_{x1}^* + V_{x2}^* + V_{x3}^* (x = a, b, c)$, Equation (14) can be solved as:

$$\begin{cases} V_a^* = V_a + V_z \\ V_b^* = V_b + V_z \\ V_c^* = V_c + V_z \\ V_z = -x_5 V_a + (\frac{2}{3}x_5 - \frac{1}{3})V_b + \frac{x_5-2}{3}V_c + \frac{2x_5-1}{6}V_{dc} \end{cases} \tag{15}$$

It can be seen that the expression of the zero-sequence component and the duty cycle of the redundant state are related, but when the redundant switching state is used on average, that is, x_5 = 1/2, the expression of the zero-sequence component can be simplified as:

$$V_z = -\frac{1}{2}(V_a + V_c). \tag{16}$$

According to the same derivation, when the other sectors respectively set $x_5 = x_6 = x_9 = 1/2$, the same expression of the zero-sequence component can be obtained:

$$V_z = -\frac{1}{2}(V_{\max} + V_{\min}). \tag{17}$$

Correspondingly, the value of each phase sub-modulation wave modulated by MCBPWM is:

$$\begin{cases} V_{\max 1}^* = \frac{1}{3}V_{\max} - \frac{1}{3}V_{\min} + \frac{1}{6}V_{dc} \\ V_{\max 2}^* = \frac{1}{6}V_{\max} - \frac{1}{6}V_{\min} \\ V_{\max 3}^* = -\frac{1}{6}V_{dc} \end{cases} \\ \begin{cases} V_{mid1}^* = \frac{1}{3}V_{mid} - \frac{1}{3}V_{\min} + \frac{1}{6}V_{dc} \\ V_{mid2}^* = -\frac{1}{6}V_{\max} + \frac{1}{3}V_{mid} - \frac{1}{6}V_{\min} \\ V_{mid3}^* = -\frac{1}{3}V_{\max} + \frac{1}{3}V_{mid} - \frac{1}{6}V_{dc} \end{cases} \\ \begin{cases} V_{\min 1}^* = \frac{1}{6}V_{dc} \\ V_{\min 2}^* = -\frac{1}{6}V_{\max} + \frac{1}{6}V_{\min} \\ V_{\min 3}^* = -\frac{1}{3}V_{\max} + \frac{1}{3}V_{\min} - \frac{1}{6}V_{dc} \end{cases} \tag{18}$$

3.3. Equivalence of N-Level VSVPWM Modulation and MCBPWM Modulation

Similarly, taking the five-level A_3 sector as an example, as shown in Figure 9, the virtual vectors $V_{\alpha 3}$, $V_{\alpha 4}$ and $V_{\lambda 2,0}$ are used to synthesize the reference vector, and the corresponding action times are T_2, T_1 and T_0 respectively. $V_{\alpha 3}$ has three redundant states, the duty cycles of the redundant states are represented by x_1, x_2 and (1-x_1-x_2). Same as four levels, the modulation wave is divided into four sub-modulation waves, and the same 22 segment symmetrical switching sequence as VSVPWM modulation can be obtained: 100→200→210→211→311→321→322→422→432→433→443→443→433→432→422→322→321→311 →211→210→200→100. As shown in Figure 9, the expression of zero-sequence component is:

$$\begin{aligned} V_z = (x_1 + 2x_2 - \tfrac{3}{2})V_a + \tfrac{3}{4}(1 - x_1 - 2x_2)V_b \\ -\tfrac{1}{4}(1 + x_1 + 2x_2)V_c + \tfrac{1-x_1-2x_2}{4}V_{dc} \end{aligned} \tag{19}$$

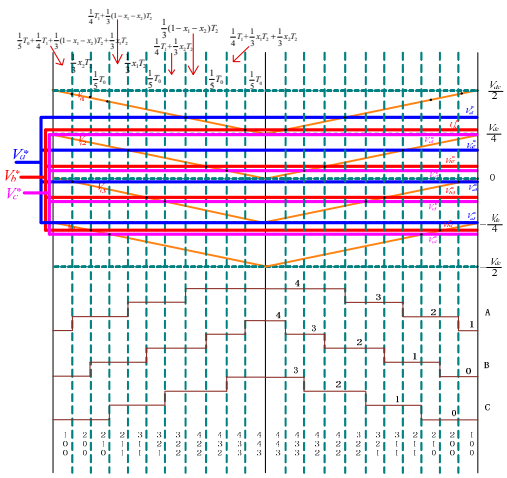


Figure 9. The relationship between the five-level A3 sector SVPWM full switching sequence and the MCBPWM modulation.

Based on this equivalence relation, the values of each phase of each sub-modulation wave of MCBPWM modulation strategy are obtained as follows:

$$\begin{cases} V_{a1}^* = \frac{1}{4}V_{ac} + \frac{1}{4}V_{dc} \\ V_{a2}^* = \frac{1}{4}(x_1 + x_2)V_{bc} - \frac{1}{4}(2 - 4x_1 - 4x_2)V_{ab} + \frac{1-x_1-x_2}{4}V_{dc} \\ V_{a3}^* = \frac{1}{4}(4x_2 - 1)V_{ab} + \frac{1}{4}x_2V_{bc} - \frac{x_2}{4}V_{dc} \\ V_{a4}^* = -\frac{V_{dc}}{4} \end{cases}$$
$$\begin{cases} V_{b1}^* = \frac{1}{4}V_{bc} + \frac{1}{4}V_{dc} \\ V_{b2}^* = \frac{1}{4}(4x_1 + 4x_2 - 3)V_{ab} + \frac{1}{4}(x_1 + x_2)V_{bc} + \frac{1-x_1-x_2}{4}V_{dc} \\ V_{b3}^* = \frac{1}{4}(4x_2 - 2)V_{ab} + \frac{1}{4}x_2V_{bc} - \frac{x_2}{4}V_{dc} \\ V_{b4}^* = -\frac{1}{4}V_{ab} - \frac{1}{4}V_{dc} \end{cases} \tag{20}$$
$$\begin{cases} V_{c1}^* = \frac{V_{dc}}{4} \\ V_{c2}^* = \frac{1}{4}(4x_1 + 4x_2 - 3)V_{ab} + \frac{1}{4}(x_1 + x_2 - 1)V_{bc} + \frac{1-x_1-x_2}{4}V_{dc} \\ V_{c3}^* = \frac{1}{4}(4x_2 - 2)V_{ab} + \frac{1}{4}(x_2 - 1)V_{bc} - \frac{x_2}{4}V_{dc} \\ V_{c4}^* = -\frac{1}{4}V_{ac} - \frac{1}{4}V_{dc} \end{cases}$$

According to Equation (19), the expression of the zero-sequence component and the duty cycle of the redundant state are related, but when the redundant switching state is used on average, i.e., $x_1 = x_2 = 1/3$. The expression of the zero-sequence can be simplified as:

$$V_z = -\frac{1}{2}(V_a + V_c). \tag{21}$$

According to the same derivation, when $x_i = 1/3$ in other sectors, the same expression of zero sequence component can be obtained:

$$V_z = -\frac{1}{2}(V_{\max} + V_{\min}). \tag{22}$$

The corresponding values of each phase sub-modulated wave are:

$$\begin{cases} V^*_{\max 1} = \frac{1}{4}V_{\max} - \frac{1}{4}V_{\min} + \frac{1}{4}V_{dc} \\ V^*_{\max 2} = \frac{1}{6}V_{\max} - \frac{1}{6}V_{\min} + \frac{1}{12}V_{dc} \\ V^*_{\max 3} = \frac{1}{12}V_{\max} - \frac{1}{12}V_{\min} - \frac{1}{12}V_{dc} \\ V^*_{\max 4} = -\frac{V_{dc}}{4} \end{cases}$$
$$\begin{cases} V^*_{mid1} = \frac{1}{4}V_{mid} - \frac{1}{4}V_{\min} + \frac{1}{4}V_{dc} \\ V^*_{mid2} = -\frac{1}{12}V_{\max} + \frac{1}{4}V_{mid} - \frac{1}{6}V_{\min} + \frac{1}{12}V_{dc} \\ V^*_{mid3} = -\frac{1}{6}V_{\max} + \frac{1}{4}V_{mid} - \frac{1}{12}V_{\min} - \frac{1}{12}V_{dc} \\ V^*_{mid4} = -\frac{1}{4}V_{\max} + \frac{1}{4}V_{mid} - \frac{1}{4}V_{dc} \end{cases} \tag{23}$$
$$\begin{cases} V^*_{\min 1} = \frac{V_{dc}}{4} \\ V^*_{\min 2} = -\frac{1}{12}V_{\max} + \frac{1}{12}V_{\min} + \frac{1}{12}V_{dc} \\ V^*_{\min 3} = -\frac{1}{6}V_{\max} + \frac{1}{6}V_{\min} - \frac{1}{12}V_{dc} \\ V^*_{\min 4} = -\frac{1}{4}V_{\max} + \frac{1}{4}V_{\min} - \frac{1}{4}V_{dc} \end{cases}$$

For the n-level main circuit, each phase can output n levels. In the first sector of the virtual space vector diagram in Figure 5, there are ($n_2 - 2n + 3$) virtual vectors in total, some virtual vectors contain ($n - 2$) switch states. If the switch states of these redundant vectors are used on average, the modulation sequence of the $2 \times (3n - 4)$ segment will be formed. Finally, the zero-sequence component superimposed of each phase is obtained as follows:

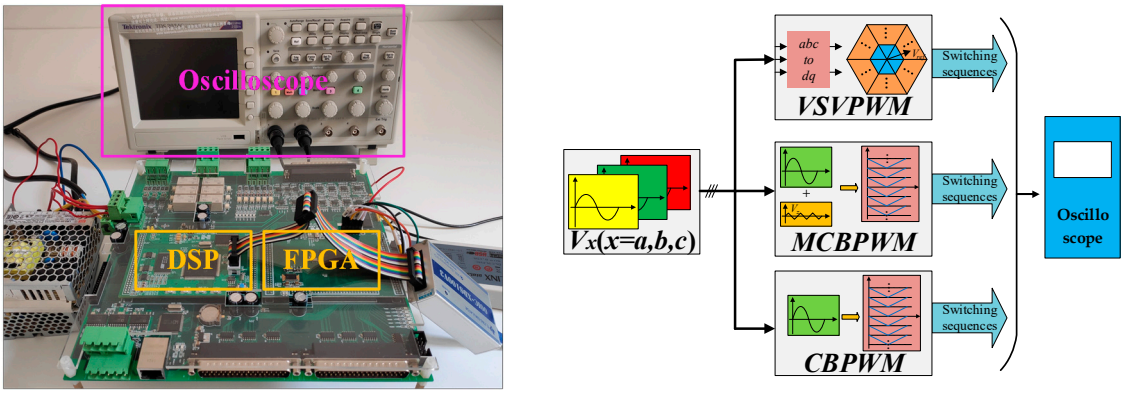
$$V_z = -\frac{1}{2}(V_{\max} + V_{\min})n = 3, 4, 5....n. \tag{24}$$

When $n = 3, 5, 7, \ldots$, or $n = 4, 6, 8, \ldots$, the equation expressions of ($n - 1$) sub-modulation waves as shown in the Appendix A section.

In this way, the two can be connected by the zero-sequence component to achieve the equivalent of any level VSVPWM sequence and the MCBPWM sequence. Based on this equivalent relationship, the MCBPWM method is proposed to realize the same output as VSVPWM by multiple sub-modulated waves obtained by the decomposition of modulated waves. In the virtual space vector of any level, by adopting the MCBPWM modulation strategy, the control of the midpoint voltage of the DC side capacitor can be achieved, and the modulation effect of the virtual space vector is realized by the simple and easy MCBPWM method, which greatly simplifies the modulation process and reduces the calculation amount and CPU occupation rate.

4. Experiment and Result Analysis

In order to verify the correctness of the equivalent relationship between two, the VSVPWM and MCBPWM modulation sequence output of the open-loop inverter under a certain modulation ratio is realized on the experimental platform of digital signal processing + field-programmable gate array (DSP + FPGA). Among them, DSP selects TMS320F28335 of the TI company, which mainly realizes control and calculation of the entire system, the output of DSP is sent to FPGA. FPGA chooses EP2C35F484C8 of Altera Company's Cyclone II series, which mainly generates pulse-width modulation (PWM) signals. The FPGA does not send gate signals to drive any power electronic switches but sends the switching states generated by the modulation algorithms to the oscilloscope for observation [20,21]. The other parts are used for power supply, communication and protection. The experimental system is shown in Figure 10.



(**a**) (**b**)

Figure 10. Experimental system. (**a**) Experimental device; (**b**) schematic diagram of the experimental process.

When the number of levels is $n = 3$ and the modulation ratio is 0.3. Given VSVPWM modulation sequence, the zero-sequence component injected into the MCBPWM sine wave can be obtained through the equivalent relationship.

Figure 11 shows A-phase sub-modulation waves $V_{a1}{}^*$ and $V_{a2}{}^*$ modulated by MCBPWM that output the same 10-segment modulation sequence as VSVPWM. $V_a{}^*$ is the sum of two sub-modulation waves of phase A.

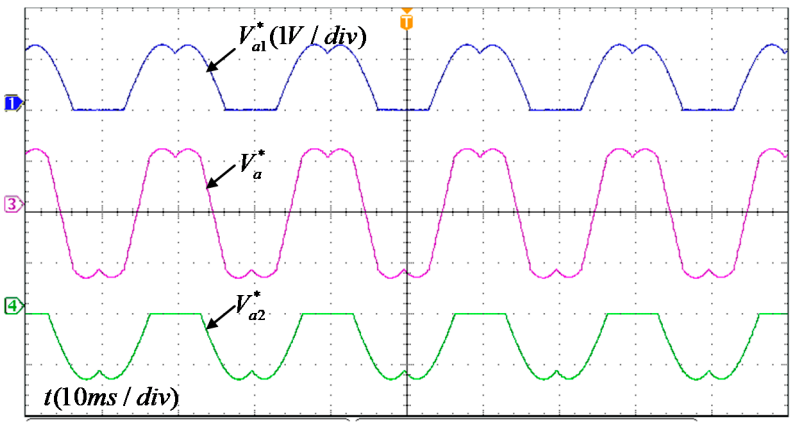


Figure 11. Waveforms of V_a*, V_{a1}* and V_{a2}* under three-level single-frequency MCBPWM modulation.

In Figure 12, V_Z represents the zero-sequence component required to achieve the equivalent of MCBPWM and VSVPWM. It can be seen that the zero-sequence component V_Z is superimposed on the A-phase sinusoidal modulation wave, and the same modulation wave V_a* as the double modulation wave MCBPWM can be obtained. This proves the correctness of the modulation wave decomposition.

Figure 13 shows the switching states of the two switching tubes S_{a1} and S_{a2} above the A-bridge arm of three-level diode clamp converter, and the output switching state of phase A is S_a. When the VSVPWM method is used to output the 10-segment switching sequence, some switching cycles can output the three-level switching state.

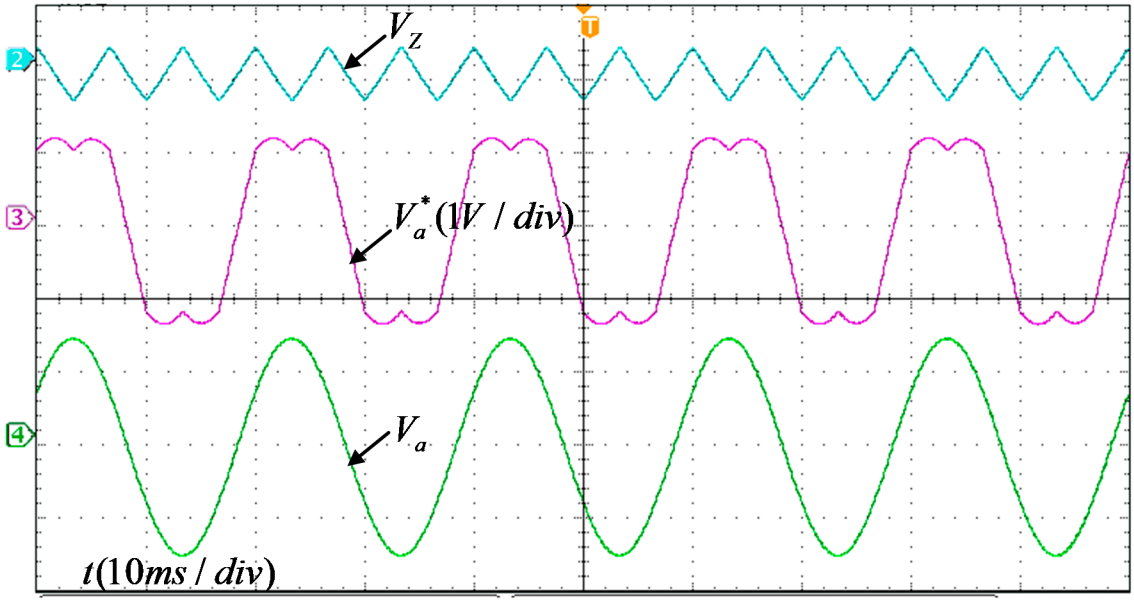


Figure 12. Waveforms of V_a, V_Z and V_a* in three-level MCBPWM modulation.

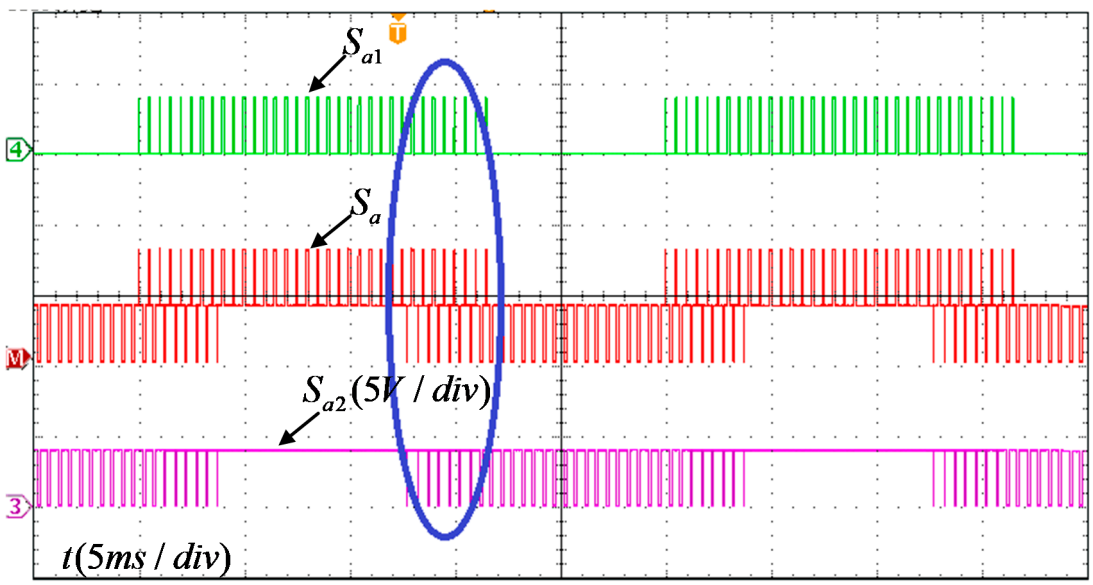


Figure 13. Switch state and output level state of upper tube S_{a1}, S_{a2} of A-phase H-bridge arm under three-level single-frequency MCBPWM modulation.

Figure 14 shows the switching state of A-phase S_{a1} under three modulation modes of VSVPWM, MCBPWM and CBPWM. The switching state of VSVPWM and MCBPWM are exactly the same, indicating that the MCBPWM can realize the same modulation effect as VSVPWM. It can be seen from the above experimental waveform that the total output results and the results of each switch state under the two modulation methods are exactly the same, which proves the correctness of the equivalence relationship between VSVPWM and MCBPWM.

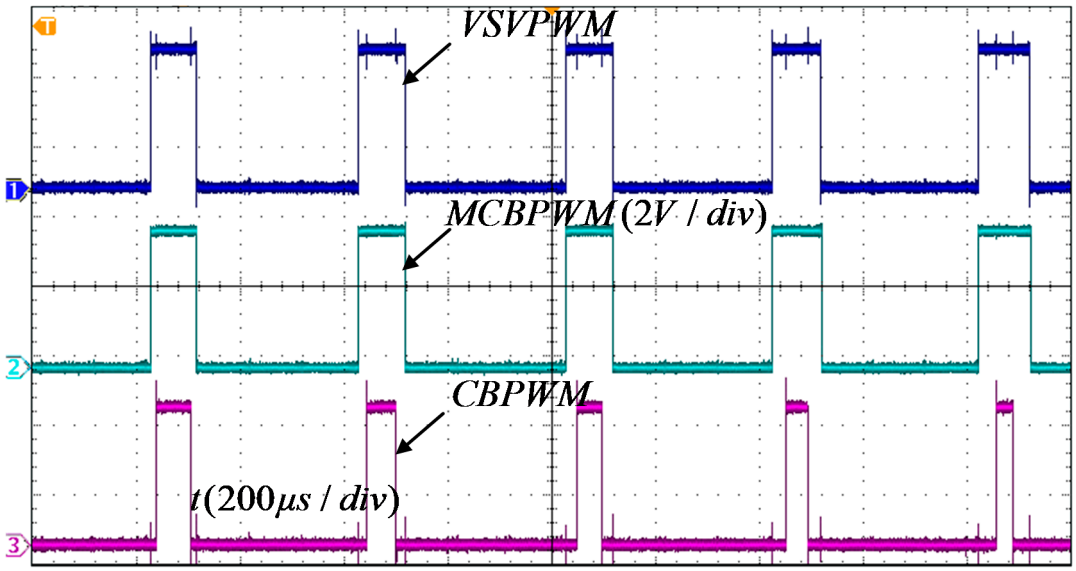


Figure 14. Switching state of A phase S_{a1} under 3 modulation modes.

5. Discussion

This paper mainly conducted an in-depth study on the equivalent relationship between the VSVPWM and MCBPWM. By decomposing each phase modulation wave, through strict theoretical derivation and mathematical calculation, the zero-sequence component to be injected in the three-phase sinusoidal modulation wave is obtained, and the in-phase stacked CBPWM is performed using each decomposed sub-modulation wave. It has the same control effect as VSVPWM, successfully achieves the equivalent of VSVPWM and MCBPWM with any level and any number of segments, simplifies the analysis of VSVPWM, solves the voltage imbalance problem on the DC side of three-phase NPC, and perfects the weakness of three-phase NPC multi-level converter. In this paper, the equivalent relationship between VSVPWM and MCBPWM is deduced to the n-th level, which solves the difficulty of VSVPWM caused by the increase in the number of levels. It has important significance for the application of multi-level NPC converters.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

Abbreviation	**Full Name**
THD	Total harmonic distortion
PWM	Pulse-width modulation
VSVPWM	Virtual space vector pulse-width modulation
CBPWM	Carrier-based pulse-width modulation
SVPWM	Space vector pulse-width modulation
MCBPWM	Multi-modulation carrier CBPWM
NPC	Neutral-point-clamped
DSP	Digital signal processing
FPGA	Field programmable gate array

Appendix A

When $n = 3, 5, 7, \ldots$, the values of $(n-1)$ sub-modulation waves are:

$$
\begin{cases}
V^*_{\max 1} = \frac{1}{n-1}V_{\max} - \frac{1}{n-1}V_{\min} + \left[\frac{1}{2} - \frac{1}{n-1}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\max i} = \frac{n-i-1}{(n-1)(n-2)}V_{\max} - \frac{n-i-1}{(n-1)(n-2)}V_{\min} + \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\max(\frac{n-1}{2})} = \frac{1}{2(n-2)}V_{\max} - \frac{1}{2(n-2)}V_{\min} + \frac{n-3}{2(n-1)(n-2)}V_{dc} \\
V^*_{\max(\frac{n+1}{2})} = \frac{n-3}{2(n-1)(n-2)}V_{\max} - \frac{n-3}{2(n-1)(n-2)}V_{\min} - \frac{n-3}{2(n-1)(n-2)}V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\max(n-i)} = \frac{i-1}{(n-1)(n-2)}V_{\max} - \frac{i-1}{(n-1)(n-2)}V_{\min} - \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\max(n-1)} = -(\frac{1}{2} - \frac{1}{n-1})V_{dc}
\end{cases}
$$

$$
\begin{cases}
V^*_{mid1} = \frac{1}{n-1}V_{mid} - \frac{1}{n-1}V_{\min} + \left[\frac{1}{2} - \frac{1}{n-1}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{midi} = -\frac{i-1}{(n-1)(n-2)}V_{\max} + \frac{1}{n-1}V_{mid} - \frac{n-i-1}{(n-1)(n-2)}V_{\min} + \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{mid(\frac{n-1}{2})} = -\frac{n-3}{2(n-1)(n-2)}V_{\max} + \frac{1}{n-1}V_{mid} - \frac{1}{2(n-2)}V_{\min} + \frac{n-3}{2(n-1)(n-2)}V_{dc} \\
V^*_{mid(\frac{n+1}{2})} = -\frac{1}{2(n-2)}V_{\max} + \frac{1}{n-1}V_{mid} - \frac{n-3}{2(n-1)(n-2)}V_{\min} - \frac{n-3}{2(n-1)(n-2)}V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{mid(n-i)} = -\frac{n-i-1}{(n-1)(n-2)}V_{\max} + \frac{1}{n-1}V_{mid} - \frac{i-1}{(n-1)(n-2)}V_{\min} - \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{mid(n-1)} = -\frac{1}{n-1}V_{\max} + \frac{1}{n-1}V_{mid} - (\frac{1}{2} - \frac{1}{n-1})V_{dc}
\end{cases}
$$

$$
\begin{cases}
V^*_{\min 1} = (\frac{1}{2} - \frac{1}{n-1})V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\min i} = -\frac{i-1}{(n-1)(n-2)}V_{\max} + \frac{i-1}{(n-1)(n-2)}V_{\min} + \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\min(\frac{n-1}{2})} = -\frac{n-3}{2(n-1)(n-2)}V_{\max} + \frac{n-3}{2(n-1)(n-2)}V_{\min} + \frac{n-3}{2(n-1)(n-2)}V_{dc} \\
V^*_{\min(\frac{n+1}{2})} = -\frac{1}{2(n-2)}V_{\max} + \frac{1}{2(n-2)}V_{\min} - \frac{n-3}{2(n-1)(n-2)}V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\min(n-i)} = -\frac{n-i-1}{(n-1)(n-2)}V_{\max} + \frac{n-i-1}{(n-1)(n-2)}V_{\min} - \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\
\qquad\qquad\qquad\qquad \cdots\cdots \qquad\qquad \cdots\cdots \\
V^*_{\min(n-1)} = -\frac{1}{n-1}V_{\max} + \frac{1}{n-1}V_{\min} - \left[\frac{1}{2} - \frac{1}{n-1}\right]V_{dc}
\end{cases}
\tag{A1}
$$

When $n = 4, 6, 8, \ldots$, the values of $(n-1)$ sub-modulated wave are:

$$\begin{cases} V^*_{\max 1} = \frac{1}{n-1}V_{\max} - \frac{1}{n-1}V_{\min} + \left[\frac{1}{2} - \frac{1}{n-1}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\max i} = \frac{n-i-1}{(n-1)(n-2)}V_{\max} - \frac{n-i-1}{(n-1)(n-2)}V_{\min} + \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\max(\frac{n}{2})} = \frac{n-2}{2(n-1)(n-2)}V_{\max} - \frac{n-2}{2(n-1)(n-2)}V_{\min} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\max(n-i)} = \frac{i-1}{(n-1)(n-2)}V_{\max} - \frac{i-1}{(n-1)(n-2)}V_{\min} - \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\max(n-1)} = -(\frac{1}{2} - \frac{1}{n-1})V_{dc} \end{cases}$$

$$\begin{cases} V^*_{mid1} = \frac{1}{n-1}V_{mid} - \frac{1}{n-1}V_{\min} + \left[\frac{1}{2} - \frac{1}{n-1}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{midi} = -\frac{i-1}{(n-1)(n-2)}V_{\max} + \frac{1}{n-1}V_{mid} - \frac{n-i-1}{(n-1)(n-2)}V_{\min} + \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{mid(\frac{n}{2})} = -\frac{n-2}{2(n-1)(n-2)}V_{\max} + \frac{1}{n-1}V_{mid} - \frac{1}{2(n-2)}V_{\min} + \frac{n-2}{2(n-1)(n-2)}V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{mid(n-i)} = -\frac{n-i-1}{(n-1)(n-2)}V_{\max} + \frac{1}{n-1}V_{mid} - \frac{i-1}{(n-1)(n-2)}V_{\min} - \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{mid(n-1)} = -\frac{1}{n-1}V_{\max} + \frac{1}{n-1}V_{mid} - (\frac{1}{2} - \frac{1}{n-1})V_{dc} \end{cases} \tag{A2}$$

$$\begin{cases} V^*_{\min 1} = (\frac{1}{2} - \frac{1}{n-1})V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\min i} = -\frac{i-1}{(n-1)(n-2)}V_{\max} + \frac{i-1}{(n-1)(n-2)}V_{\min} + \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\min(\frac{n}{2})} = -\frac{n-2}{2(n-1)(n-2)}V_{\max} + \frac{n-2}{2(n-1)(n-2)}V_{\min} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\min(n-i)} = -\frac{n-i-1}{(n-1)(n-2)}V_{\max} + \frac{n-i-1}{(n-1)(n-2)}V_{\min} - \left[\frac{1}{2} - \frac{i-1}{n-1} - \frac{n-i-1}{(n-1)(n-2)}\right]V_{dc} \\ \cdots\cdots \qquad \cdots\cdots \\ V^*_{\min(n-1)} = -\frac{1}{n-1}V_{\max} + \frac{1}{n-1}V_{\min} - \left[\frac{1}{2} - \frac{1}{n-1}\right]V_{dc} \end{cases}$$

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