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A Limited Common-Mode Current Switched-Capacitor Multilevel Inverter Topology and Its Performance and Lifetime Evaluation in Grid-Connected Photovoltaic Applications

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Abstract: In this paper, a switched-capacitor multilevel inverter with voltage boosting and common-mode-voltage reduction capabilities is put forth. The proposed inverter is synthesized with one-half bridge and several switched-capacitor cells. Due to the voltage boosting and common-mode current reduction features, the proposed multilevel inverter is suitable for grid-connected PV applications. In addition, an analytical lifetime evaluation based on mission profile of the proposed inverter has been presented to derive lifetime distribution of semiconductors. Whereas in the proposed inverter, any components failure can bring the whole system to a shutdown. The series reliability model is used to estimate the lifetime of the overall system. The performance of the suggested multilevel inverter in grid-connected applications is verified through the simulation results using the grid-tied model in Matlab/Simulink. Moreover, the viability and feasibility of the presented inverter are proven by using a one kW lab-scaled prototype.

Keywords: grid-tied PV; common-mode current; switched capacitor multilevel

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1. Introduction

Recently solar energy has gained more attention since it is clean, emission-free, and easy to install. However, the voltage produced by these resources is low and requires a voltage booster stage, either a dc-dc stage or a transformer [1]. Conventionally in photovoltaic (PV) grid-connected inverters for safety issues, a line frequency transformer or a high-frequency transformer is used to ensure the galvanic isolation within the utility grid and PV array and also to boost the input voltage. The line frequency transformers are bulky and have low efficiency and high cost. High-frequency transformers have lower volume, weight, and cost but require extra power stages and extra elements that complicate the system and, more importantly, impair inverter efficiency [2]. To increase efficiency and power density and reduce cost and weight, transformers are excluded from PV systems. Elimination of the transformer may lead to some consequences such as requiring high voltage in the input of the inverter and ground leakage current that flow through parasitic capacitors between the PV terminals and grounded panel frame [3]. The leakage current leads to some anomalies such as the increment of output current total harmonic distortion (THD), increment of power losses, PV panel degradation, and electric shock. In order to use transformer-less inverters in industrial applications and ensure system safety, several solutions to suppress the leakage current have been investigated, which are generally based on two main ideas. The first one is based on the idea of decoupling PV and grid during freewheeling operation modes that result in eliminating high frequency (switching

frequency) variant common-mode voltage. Derivations of the H-bridge inverter such as H5 [4], OH5 [5], H6 with ac bypass [6], H6 with dc bypass [7], and HERIC [8] inverters, use the power decoupling concept in the ac or dc side. However, the decoupling solution cannot be completely executed due to the parasitic capacitors of active switches. Thus, the leakage current still exists in the mentioned solutions. Furthermore, in the mentioned solution, two identical filter inductors with independent cores are needed that causes an increase in the size and cost [9]. The second solution is to directly clamp the voltage of PV terminals, which is more successful at mitigating the leakage current. Topologies like half-bridge inverter, NPC, and ANPC [10] inverters suppress current flow in parasitic capacitors by grounding the middle point of the dc-link. Doubly grounded topologies, which are also known as common-ground inverters, also clamp parasitic PV capacitors by connecting one terminal of PV array to the ground of the utility grid in order to eliminate leakage current completely [11].

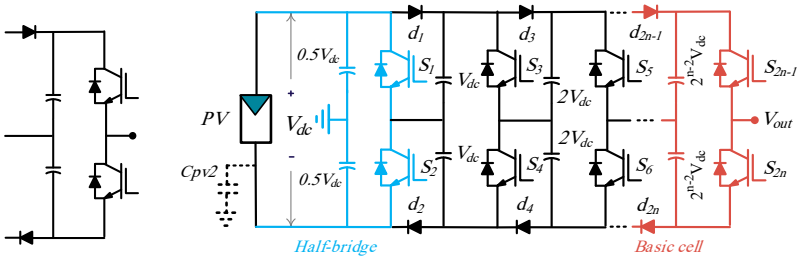
Multilevel converters surpass two-level or three-level converters on account of better output quality. Moreover, the multilevel converters have low voltage stress on components, smaller filter requirement, low EMI, and lower switching loss [12–14]. In addition, these converters are used when voltage matching is required. Many multilevel topologies have been presented in the literature. Although they offer many advantages in some industrial applications, usually they cannot mitigate the leakage current and are not suitable for grid-connected PV applications.

In this paper, a switched-capacitor multilevel inverter (SC-MI) for PV application is put forth. The proposed topology is composed of several basic modules. Each basic module is synthesized with two capacitors, two switches, and two diodes. The topology uses solely one dc source as the input source. The common mode current in the proposed topology oscillates with the grid frequency thus the leakage current is effectively alleviated in grid-tied applications with the suggested multilevel inverter. Since the proposed inverter is synthesized with switched-capacitor cells, the voltages of the capacitors are balanced spontaneously without using any auxiliary circuit. The other advantage of the proposed inverter is that it draws a continuous current from the input. Detection of the weakest components in the suggested inverter using the presented reliability analyses is an indispensable part of the reliability-based design to lower the risks of semiconductor devices during operation [15–17]. Since the electrical and thermal stresses of the semiconductor devices change through the inverter, a method is required to consider the variable stresses on the semiconductor devices, which is called mission-profile based lifetime estimation [18,19]. Detail of the used lifetime estimation approaches is discussed in the following parts of this paper.

2. Structure and Operational Principle

2.1. Proposed Topology with N Stages

The presented inverter was composed of one half-bridge and several basic modules. The basic module, which was combined with a pair of capacitors, switches, and diodes, is illustrated in Figure 1a,b, and shows the general configuration of the proposed SC-MI.



(**a**) (**b**)

Figure 1. Proposed switched-capacitor (SC)—based multilevel inverter (MI): (**a**) Basic cell; (**b**) general configuration.

2.2. Operational Principle

An eight-level structure of the proposed multilevel inverter topology illustrated in Figure 2 was taken into consideration to define how various voltage levels were created and capacitors voltage were balanced. To this end, the on and off status of the semiconductor components and charging/discharging states of the capacitors were indicated in Table 1. In this table, "*C*", "*D*", and "*F*" indicated the charging, discharging, and floating states of the capacitors, respectively. Moreover, "1" and "0" show the on and off states of the semiconductors, accordingly.

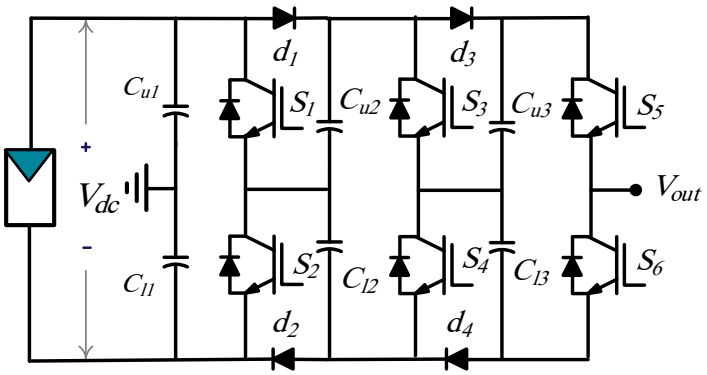


Figure 2. Eight−level configuration of the proposed topology.

Table 1. Operational states of the inverter.

Level	Switches States	Diodes States	Capacitors States	V_{out}
	S_1,S_2,S_3,S_4,S_5,S_6	d_1,d_2,d_3,d_4	C_{u2}, C_{l2}, C_{u3}, C_{l4}	
4	101010	0101	D, C, D, C	3.5 V_{dc}
3	011010	1001	C, F, D, C	2.5 V_{dc}
2	100110	0110	F, C, C, F	1.5 V_{dc}
1	010110	1010	C, N, C, F	0.5 V_{dc}
−1	101001	0101	N, C, F, C	−0.5 V_{dc}
−2	011001	1001	C, F, F, C	−1.5 V_{dc}
−3	100101	0110	F, C, C, D	−2.5 V_{dc}
−4	010101	1010	C, D, C, D	−3.5 V_{dc}

For the sake of more clarity, the current paths of the voltage levels must be derived. In addition, the charging paths of the capacitors can prove that the capacitors are charging and discharging equally. Figure 3 can cover the mentioned aims. In these figures, the output current paths are shown in black, and the charging current paths of the capacitors are colored in red.

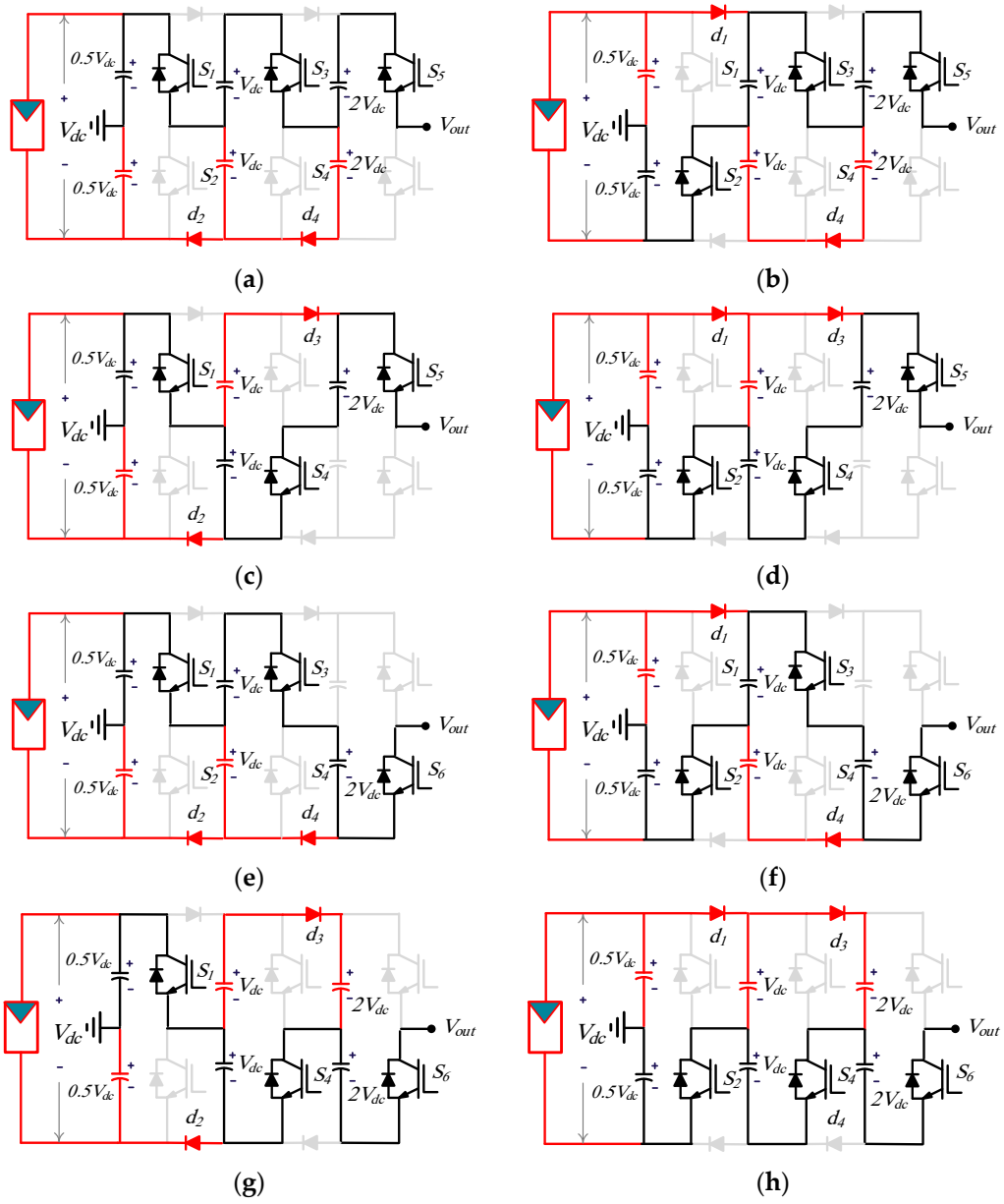


Figure 3. Switching patterns to develop different voltage levels: (**a**) 3.5 V_{dc}; (**b**) 2.5 V_{dc}; (**c**) 1.5 V_{dc}; (**d**) 0.5 V_{dc}; (**e**) −0.5 V_{dc}; (**f**) −1.5 V_{dc}; (**g**) −2.5 V_{dc}; (**h**) −3.5 V_{dc}.

3. Voltage Boosting and Leakage Current Suppression Features

As mentioned before, the proposed multilevel inverter can boost the output voltage through the switched-capacitor cells. Assuming the input voltage is V_{dc} and n is the switch legs count, the peak value of the output of the proposed inverter can be given as:

$$V_{peak} = V_{dc} \sum_{k=1}^{n} 2^{k-2}, \quad (1)$$

Because the input cell (half-bridge) in the proposed topology provides a mid-point, the capacitance of the parasitic capacitance of the input dc source (PV panel) was added to the input capacitors, as shown in Figure 4. Whereas the voltages across the input capacitors (C_{u1} and C_{l1}) oscillate with the grid frequency, which was a low frequency, the common-mode voltage across these capacitors was low. Thus, the common-mode current (leakage current) that stems from the common-mode voltage oscillation was insignificant in the

proposed inverter topology. The voltages across the input capacitors include some dc and ac content, these components are as follows:

$$V_{C_{u1}} = \frac{V_{dc}}{2} + \Delta V_{ac}, \tag{2}$$

$$V_{C_{l1}} = \frac{V_{dc}}{2} - \Delta V_{ac}, \tag{3}$$

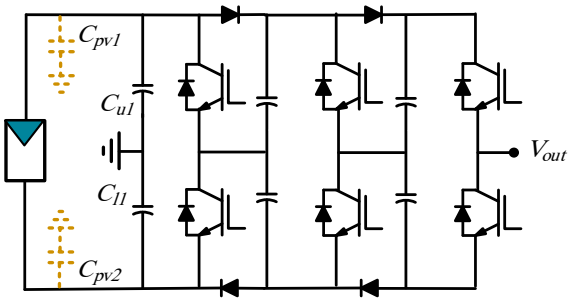


Figure 4. Stray capacitor in the proposed topology.

Considering that the input capacitors are the same ($C_{u1} = C_{l1} = C$) and knowing that the load current is a pure sinusoidal current with the peak value, angular frequency, and lagging phase delay of I_m, ω, and φ, accordingly, the oscillation content of the input capacitors voltage is obtained as

$$\Delta V_{ac} = -\frac{I_m}{C\omega}\cos(\omega t - \varphi), \tag{4}$$

Whereas the common-mode current stems from the voltage oscillation across the parasitic capacitors, this current is given as:

$$I_{cm} = (C_{pv1} + C_{pv2})\frac{dV_{C_{u1(l1)}}}{dt}, \tag{5}$$

where C_{pv1} and C_{pv2} are the parasitic capacitors of the input dc source (PV panel).

Through Equations (4) and (5), the common-mode current is obtained as

$$I_{leakage} = \frac{I_m(C_{pv1} + C_{pv2})}{2C}\sin(\omega t - \varphi), \tag{6}$$

Referring to the latter equation and knowing that the parasitic capacitors are so tiny in comparison with the input capacitors, the common-mode current was insignificant in the proposed multilevel converter.

The voltage across the capacitors varies, thus; the output voltage can experience a voltage drop at the output side. In order to provide precise voltage amplitude, a front-end boost converter can be used at the input side. This boost converter can compensate for the voltage drop, filter out the input current harmonics, and facilitate the MPPT. This point should be mentioned that, whereas the mentioned voltage drop is low, the front-end boost converter will only operate with a tiny duty cycle to make up the voltage drop and facilitate the MPPT. Figure 5 illustrates the suggested inverter, which is integrated with a front-end boost converter. The output voltage of such a configuration is obtained as

$$V_{peak} = \frac{V_{dc}}{1-d}\sum_{k=1}^{n} 2^{k-2}, \tag{7}$$

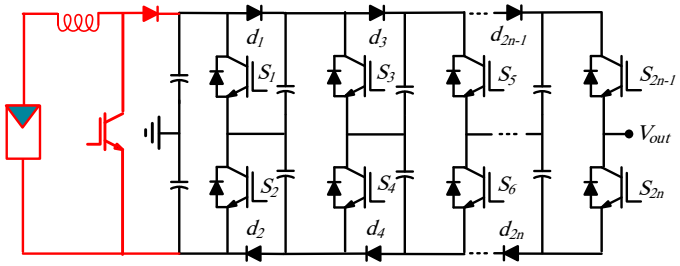


Figure 5. Proposed topology integrated with a front−end boost converter.

As shown in Equation (7), the peak value of the output voltage can be modulated by manipulating the duty cycle (d).

4. Power Loss Calculation

In this section, the power losses of the presented converter are investigated. Generally, the power losses of the converters mainly consisted of conduction losses and switching losses. Conduction power loss occurs as a result of on-state resistance and semiconductors voltage and also the capacitors' equivalent series resistance (ESR).

For an eight-level configuration, considering the power factor of unity, the on-state voltage and resistance per level are equal to:

$$R_n = \begin{cases} R_1 = R_d + ESR + R_{sw} & l = 0.5V_{dc} \\ R_2 = R_d + 2ESR + 2R_{sw} & l = 1.5V_{dc} \\ R_3 = R_d + 2ESR + 2R_{sw} & l = 2.5V_{dc} \\ R_4 = 3ESR + 3R_{sw} & l = 3.5V_{dc} \end{cases} \quad (8)$$

$$V_{on,s} = \begin{cases} V_{on1} = 2V_{os,d} + V_{os,sw} & l = 0.5V_{dc} \\ V_{on2} = V_{os,d} + 2V_{os,sw} & l = 1.5V_{dc} \\ V_{on3} = V_{os,d} + 2V_{os,sw} & l = 2.5V_{dc} \\ V_{on4} = 3V_{os,sw} & l = 3.5V_{dc} \end{cases} \quad (9)$$

The total conduction loss of the converter can be figured out by:

$$P_{loss\_conduction} = f\left(\sum_{n-1}^{4} 4R_n \int i(t)^2 dt + \sum_{n-1}^{4} 4V_{on,n} \int i(t) dt\right), \quad (10)$$

where, R_d, R_{sw}, ESR, l, V_{dc}, f, $i(t)$, $V_{on,d}$ and $V_{on,sw}$ are the diode on-state resistance, diode switch on-state resistance, diode capacitor equal series resistance, diode voltage level, diode input voltage, diode frequency of output voltage, diode instantaneous load current, diode voltage drop value of a diode in conduction mode, and diode voltage drop value of a switch in conduction mode, respectively.

The switching losses, as its name suggests, appear during turning on and off of the semiconductors due to the overlap of voltage and current of the switch. For an eight-level configuration, the switching power loss of each switch is given as

$$P_{s_{1,2}} = 0.5C_s V_{dc}^2 f_s, \quad (11)$$

$$P_{s_{3,4}} = 2C_s V_{dc}^2 f_s, \quad (12)$$

$$P_{s_{5,6}} = \frac{8}{\pi} C_s V_{dc}^2 f_s \sin^{-1}\left(\frac{1}{7}\right), \quad (13)$$

Thus, the total switching loss of an eight-level configuration is achieved as:

$$P_s = C_s V_{dc}^2 f_s \left(5 + \frac{8}{\pi} \sin^{-1}\left(\frac{1}{7}\right)\right), \quad (14)$$

where C_s and f_s are output capacitance of a switch and switching frequency, respectively.

5. Simulation Results of Grid-Tied Mode

In order to assess the performance of the suggested structure in grid-tied PV application, considering the characteristic that is reported in Table 2, it was tested in Matlab/Simulink by assuming various loading conditions. In this investigation, several scenarios were considered for reactive power.

Table 2. Characteristics of the grid-tied model.

Parameters	Values
Input voltage	135 V
C_{u1},C_{l1},C_{u2},C_{l2},C_{u3},C_{l3}	2200 µF
Switching strategy	Ls-SPWM
Grid voltage & frequency	20 kHz
Base apparent power	6.5 kVA
Base voltage (peak)	320 V
L (grid voltage)	1.7 mH
Number of cells	2

In order to inject the active power and exchange the reactive power in grid-tied mode, the ac components of the grid were transferred to the d-q axis components. The MPPT unit gives the reference of DC-link voltage. A Proportional Integral (PI) controller was used to keep the DC voltage into the desired value and develop the reference for the active power. The reactive power reference can be adjusted according to specialized control approaches. By using the active and reactive power references and obtaining the d- and q-axis voltages, the references of the output current can be ascertained. By having the parameters at hand, the reference output voltage was obtained. The reference voltage was used to derive the switching signal of the switches. The described control approach is shown in Figure 6.

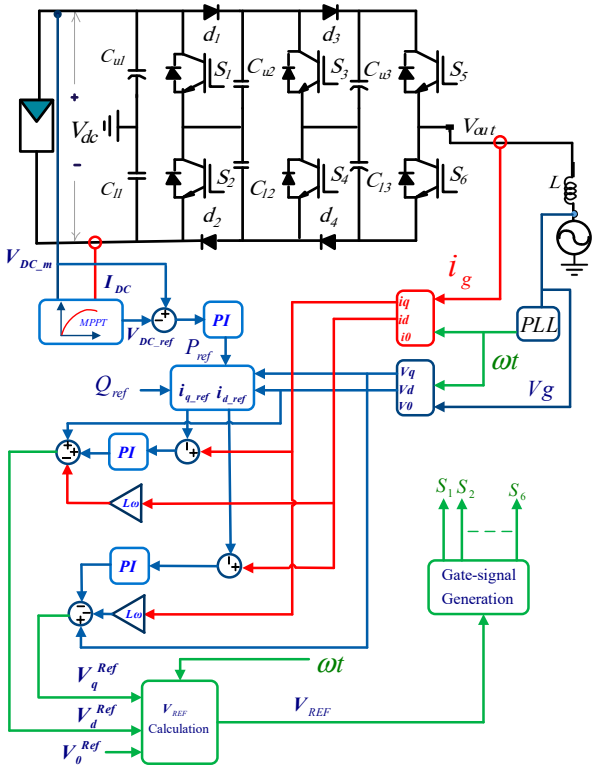


Figure 6. Control diagram of the proposed inverter in grid-tied photovoltaic (PV) system.

The provided active and reactive powers are shown in Figure 7. As is depicted in Figure 7, the gate signals were blocked to allow the capacitors to be charged through the grid up to t = 80 ms. The active power of 0.77 p.u. (5 kW) was injected into the grid from t = 80 ms to t = 2.5 s. The injected power decreased to 0.46 p.u (3 kW) at t = 2.5 s. Moreover, three scenarios were considered for the reactive power. In the first scenario, the reactive power was considered 0.55 p.u. from t = 8 ms to t = 1.8 s. It decreased to zero and −0.5 p.u at t = 1.8 s and t = 3 s, respectively. As evident in Figure 7, the suggested converter had successfully operated in lagging and leading power factors.

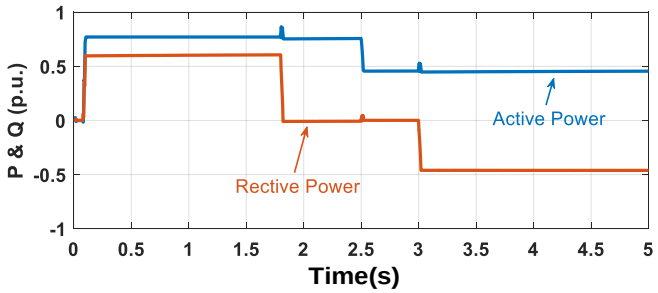


Figure 7. Active and reactive power provided in grid−tied mode.

The output voltage should be shown together with the injected current under the indicated conditions. Thus, the mentioned parameters are illustrated in Figure 8. As shown, the inverter developed a boosted high-quality ac voltage (Vg_peak 325 V) from a low voltage PV module (135 V). According to Figure 8, since the inverter operated in lagging power factor, the current was 35.57 degrees behind the output voltage from t = 80 ms to t = 1.8 s. The inverter operates in purely resistive loading conditions from t = 1.8 s to t = 2.5 s, thus the current was in phase with the output voltage. The active power decreased to 0.5 p.u. at t = 2.5 s, thus the amplitude of the injected current decreased. The reactive power decreased to −0.5 p.u. at t = 3 s. Thus the inverter operated at the leading power factor, and the injected current was ahead of the output voltage by 45 phase degree.

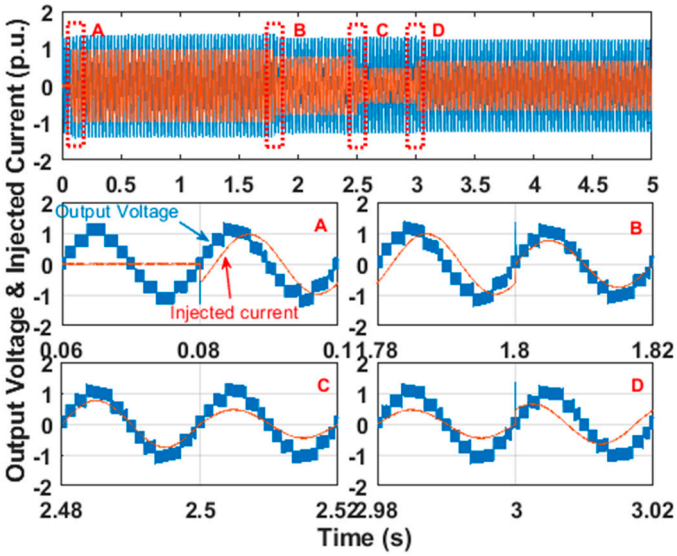


Figure 8. Output voltage of the inverter and the grid−side current.

In order to evaluate the quality of the injected current, the fast Fourier transform (FFT) technique was employed to derive Figure 9. As illustrated, the THD of the injected current was under the rated value (according to the IEEE 4715 the maximum measured THD of the injected current is to be under 5%).

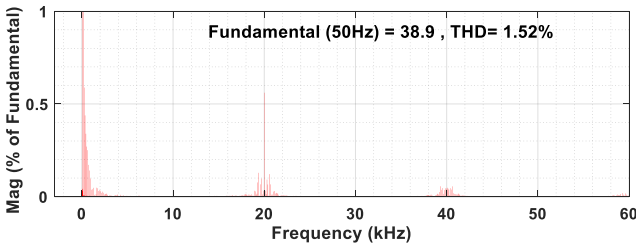


Figure 9. Fast Fourier transform (FFT) analysis of the grid current.

For completing the single-phase grid-tied investigations, the capability of the converter to mitigate the leakage current was also tested. To this end, a 300 nF stray capacitor was connected within the PV module and grid ground. The results are exhibited in Figure 10. As shown, the Root Mean Squire (RMS) value was around 20 mA, which was distinctly lower than the assigned value (according to VDE 0126-0101 standard, the leakage current should be under 300 mA).

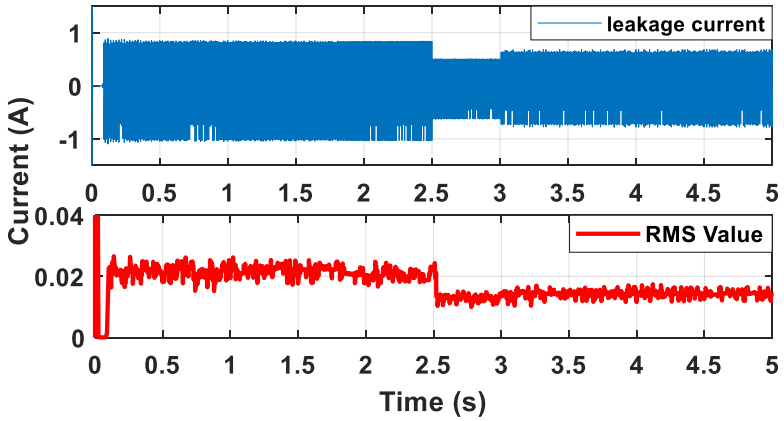


Figure 10. Leakage current in grid−tied mode.

The viability of the three-phase eight-level structure of the proposed topology in grid-connected mode was also investigated in this section. The base apparent power was considered 15 kVA, and the base phase voltage (peak value) was considered 320.

The provided active and reactive powers are exhibited in Figure 11. As shown, the presented converter had successfully supplied the reactive while transferred active power. Thus, the three-phase configuration can properly satisfy the VDE-AR-N 4105 standard. Figure 12a,b, respectively, shows the output voltage and injected current to the grid. As shown, the terminal voltage of the inverter varied slightly to provide the required reactive power.

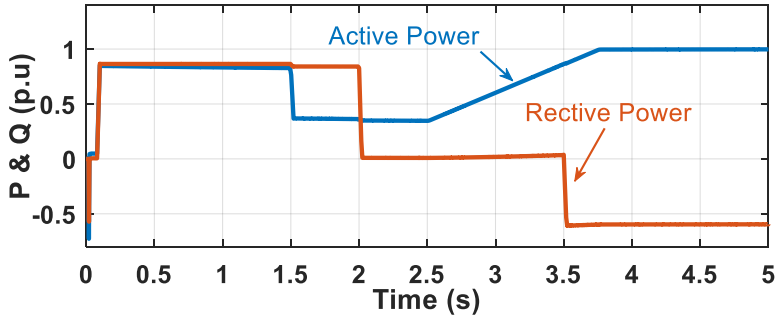
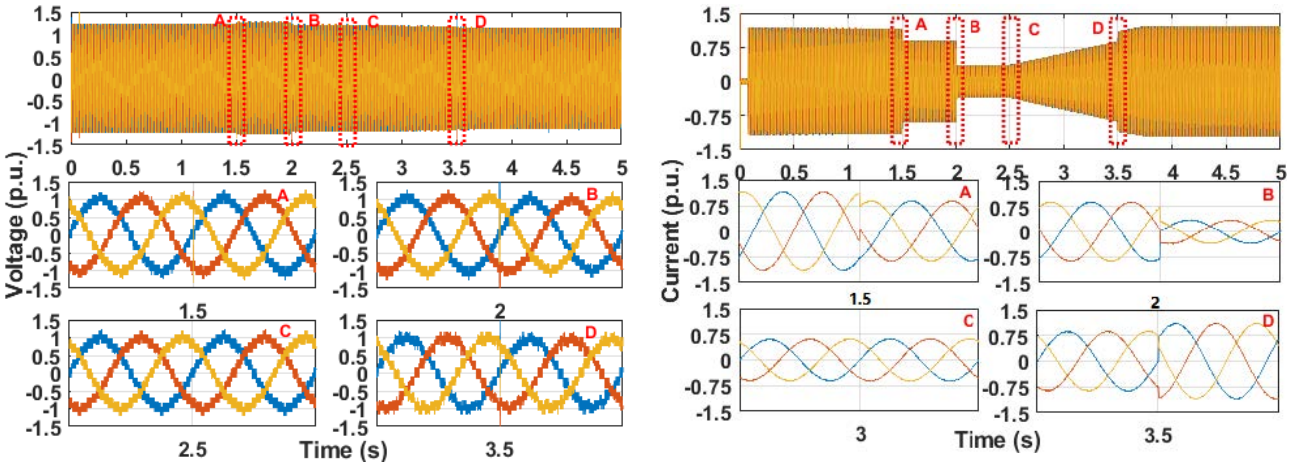


Figure 11. Active and reactive power variations of the three−phase configuration.

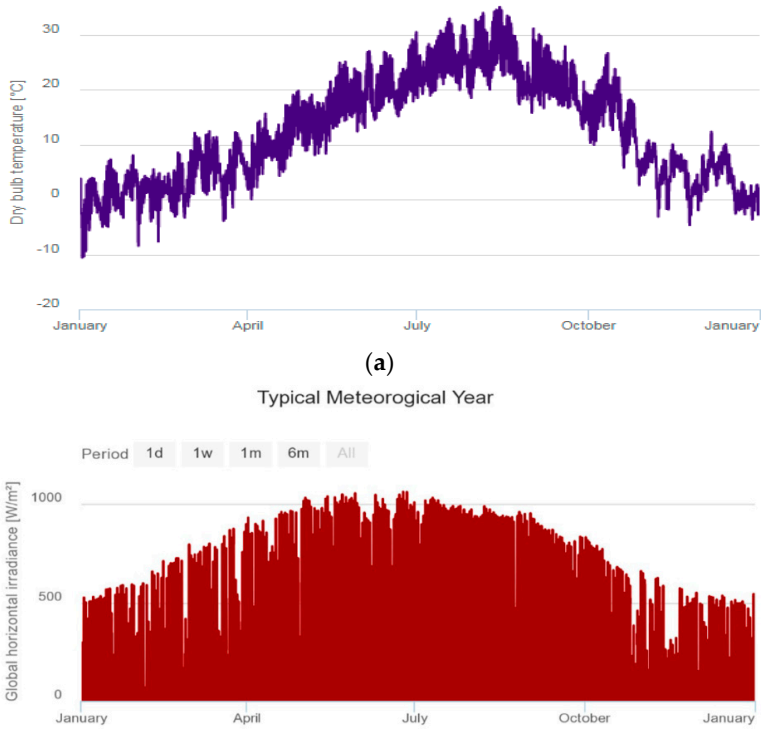


(**a**) (**b**)

Figure 12. Voltage and current in grid−tied mode of the three-phase structure: (**a**) Voltage waveforms of the inverter output; (**b**) injected current.

6. Lifetime Evaluation of the Proposed Inverter

Reliability evaluation of power converters to investigate maintenance cost and predictive lifetime is an effective step in design procedures [20–24]. In order to extract the probability lifetime distribution of the proposed converter, the mission-profile-based analysis, which is the modern reliability evaluation method, is employed [25–27]. The feasible reliable operation of the proposed inverter topology, considering the annual environmental conditions recorded by The Photovoltaic Geographical Information System (PVGIS) [28] for a site near north of Urmia lake that is depicted in Figure 13, was used.



(**a**)

(**b**)

Figure 13. Yearly mission profiles in north of Lake Urmia: (**a**) Solar irradiance level; (**b**) ambient temperature.

Junction temperatures of all the semiconductor devices of the proposed inverter must be obtained during a year by considering the annual weather conditions (provided in Figure 13). To this end, by adopting the mentioned annual weather condition, the junction temperature of six power switches and four diodes utilized in the proposed topology was extracted. The results are shown in Figure 14.

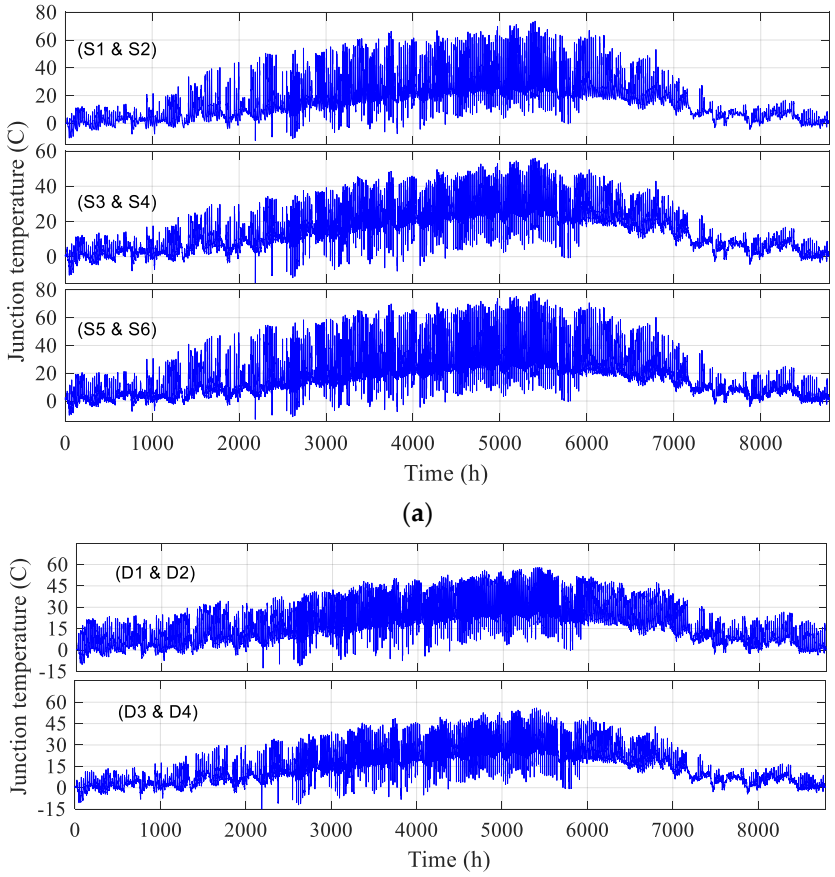


Figure 14. Junction temperatures of: (**a**) Switches (S_1 to S_6); (**b**) diodes (D_1 to D_4) in grid−connected PV inverter under the yearly mission profile.

After applying the mission profile, the junction temperatures of the power device were derived. The junction temperatures of semiconductor devices of the PV inverter have similar variations as the solar irradiance profile in Figure 13a and the ambient temperature in Figure 13b. It can be seen that the mean junction temperatures of the semiconductor devices are mostly affected by the ambient temperature profile.

A procedure is needed to clarify the lifetime estimation steps of the proposed inverter under the given weather profiles. To do so, the configuration of the PV system (the converter topology along with the control strategy) should be defined. In doing so, the power losses of the power switches and diodes, using different simulation tools, calculations, or historical-based lookup tables, can be easily derived. Subsequently, the estimation of the junction temperature of devices by considering their electro-thermal models and ambient temperature would be needed. A cycle counting method is also necessary to translate the junction temperatures of the switches to determine the parameters of the lifetime model.

Different lifetime models are conducted thus far. For simplicity, we use the lifetime model suggested in [25]. This model is one of the useful and popular models in the field. This model gives a certain lifetime value; however, due to different uncertainties in the construction process of the semiconductor devices, the Monte-Carlo method is

used to cover all possible uncertainties. In this paper, 1% variation is applied to the parameters of the mentioned lifetime model. By doing so, the lifetime distribution of the utilized semiconductor device can be derived. In the next step, unreliability curves of the semiconductor devices are obtained to indicate the weakest components. Finally, the system-level unreliability curve is derived. Therefore, the B_x index (depicted in Figure 15) as a popular reliability index can be determined easily to obtain the unreliable operation percentage of the proposed inverter duration its operation. The mentioned steps are meticulously exhibited in Figure 15.

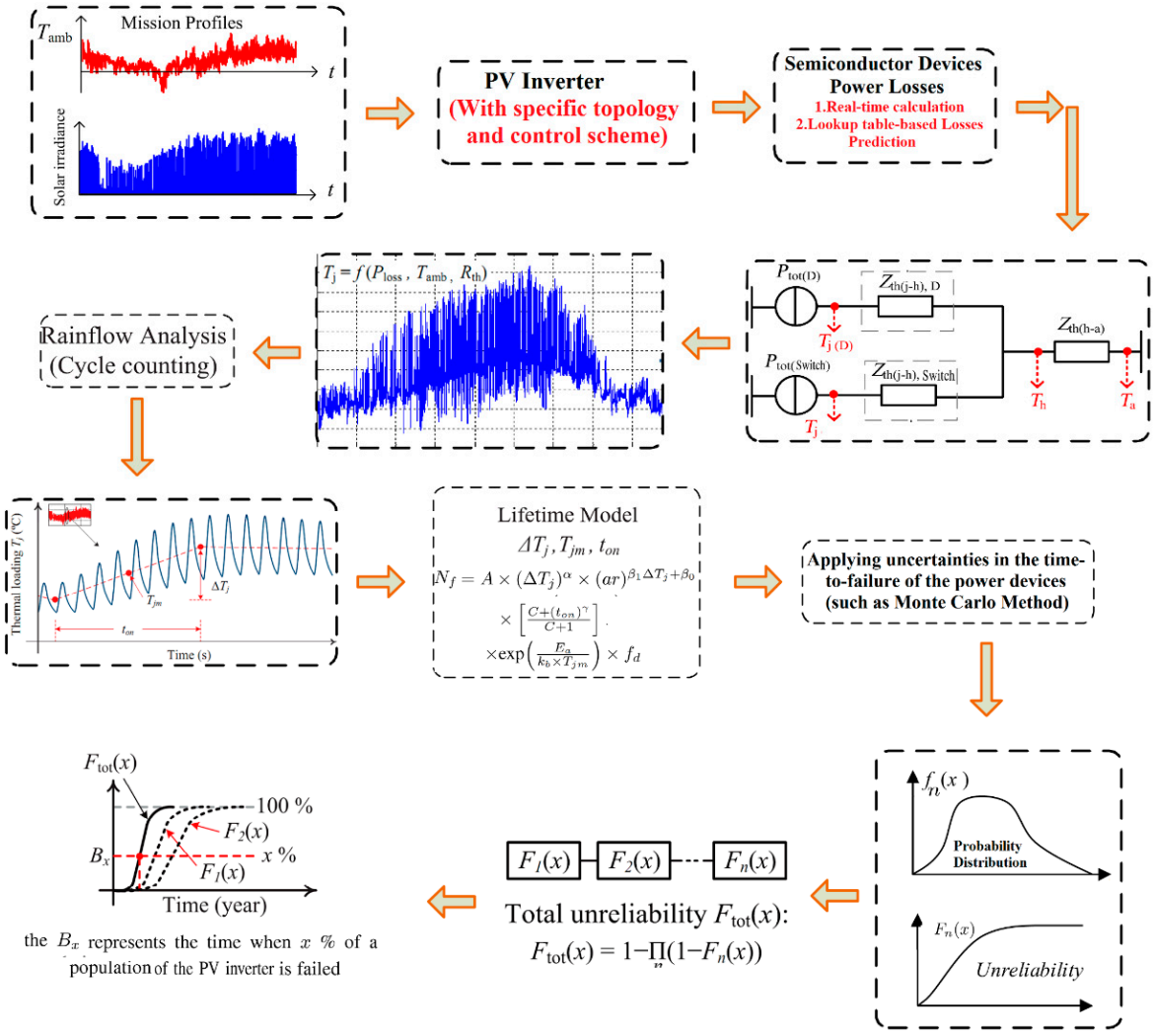


Figure 15. Lifetime profile derivation process for the proposed PV inverter with the reliability block diagrams.

Unreliability curves of the semiconductor devices by using the process in Figure 15 are shown in Figure 16. According to this figure, the diodes are more reliable than the power switches. In addition, the switches S_3 and S_5 are less likely to be failed in comparison to the other power switches. Thus, to derive the unreliability of the proposed inverter, only the unreliability curves of Figure 16a,c are sufficient to be taken into account. The overall unreliability can be obtained through Equation (15).

$$F_{tot(x)} \approx 1 - (1 - F_{S1(x)}) \cdot (1 - F_{S3(x)}) \cdot (1 - F_{S5(x)}) \cdot (1 - F_{S6(x)}), \quad (15)$$

where $F_{S1(x)}$ to $F_{S6(x)}$ are unreliability functions of switches S_1 to S_6, accordingly.

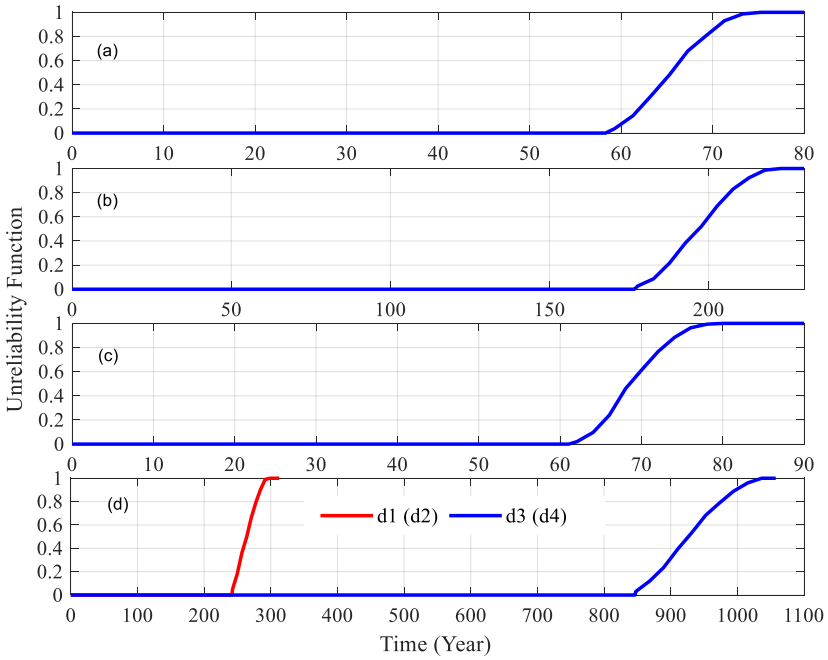


Figure 16. Unreliability results from the Monte Carlo simulation: (**a**–**c**) Switches (S_1 to S_6); (**d**) power diodes (d_1 to d_4).

The total unreliability of the proposed inverter is presented in Figure 17, and the corresponding system-level B_{10} lifetime is determined in this figure. It is expected that the out-of-reach probability of the proposed inverters at the 61st year is 10%.

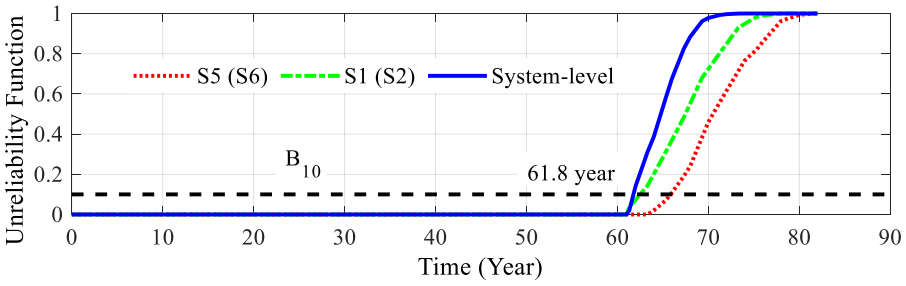


Figure 17. System level unreliability curve.

7. Comparison and Discussion

For evaluating the merits and demerits of the suggested topology, a comparison with state-of-the-art switched-capacitor multilevel inverter topologies that are presented in [29–32]. In this study, only an eight-level structure of the proposed inverter is considered. The result is listed in Table 3. In this table, N_{switch}, N_{diode}, $N_{capacitor}$, G_V, and $T_{Stand\_voltage}$ are indicative of the number of semiconductor switches, power diodes, capacitors, voltage ratio, and total standing voltage of the utilized semiconductor devices, respectively.

Table 3. Comparison.

Topology	N_{switch}	N_{diode}	$N_{capacitor}$	G_V	$T_{Stand\_voltage}$	Leakage Current Limiting Capability
[29]	12	-	2	2	5.5	no
[30]	10	-	2	0.5	8	yes
[31]	8	3	3	4	5.75	no
[32]	12	-	3	4	5.25	no
[Proposed]	6	4	6	3.5	4.86	yes

At grid voltage sags, the proposed inverter experiences abnormal conditions. Thus, the proposed inverter must tolerate transient of the DC-side voltage and grid-side current [33]. A supplementary control section should be added to the control unit to keep the inverter connected during abnormal conditions [34]. In addition, the proposed inverter components must be designed to guarantee safe operation in abnormal conditions. The proposed inverter can change its reference active and reactive power to meet different standard grid codes.

In the case of the non-sinusoidal voltage conditions on the grid side, the injected current to the grid may contain harmonic components, and thus, the THD index of the injected current may not meet the power quality standard. In these cases, different compensators must be designed to prevent high total harmonic distortions [35].

8. Experimental Results

For evaluating the viability of the suggested topology, using a prototype, its performances were investigated under different loading conditions. The characteristics of the prototype are listed in Table 4. The peak value of the output voltage to be developed was considered 320 V and the frequency was 50 Hz. The level-shifted sinusoidal pulse width modulation (SPWM) was used to control power switches. 10 kHz was the switching frequency of the converter. Figure 18 shows the prototype.

Table 4. Components utilized in the prototype.

Components	Type
Switches	IRFP450
Opto-coupler	TLP250
Microprocessor	DSP-F28335
Capacitors	3300 µF
Switching power supply	iS0515s
Diodes	FFPF20UP40S

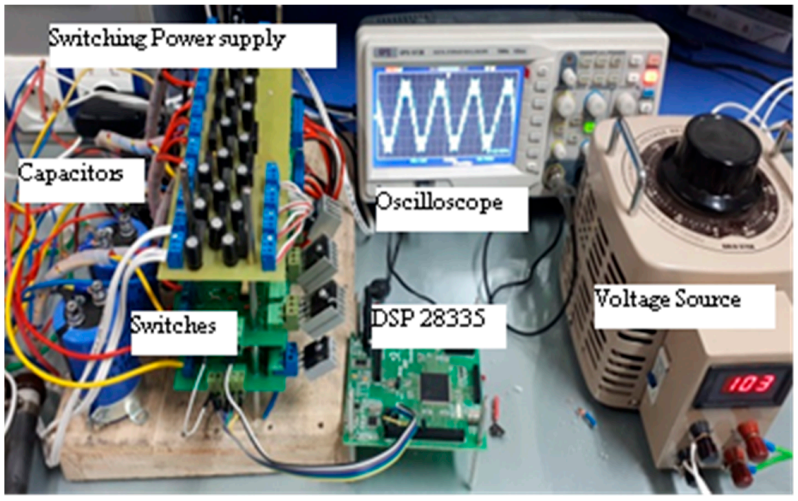
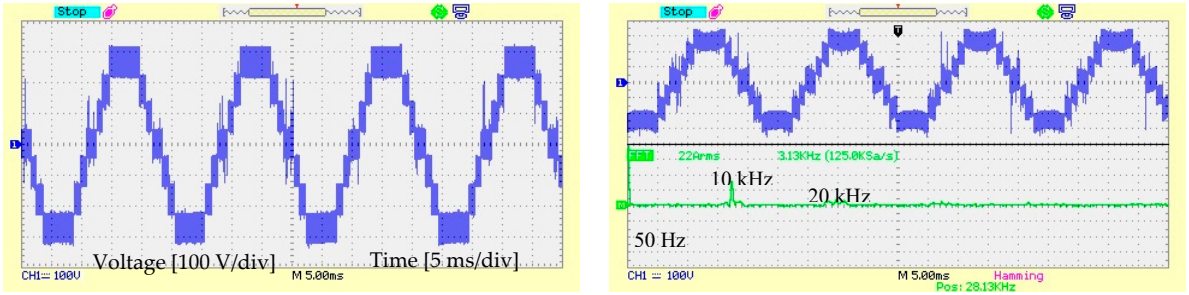


Figure 18. Eight-level laboratory-scaled prototype.

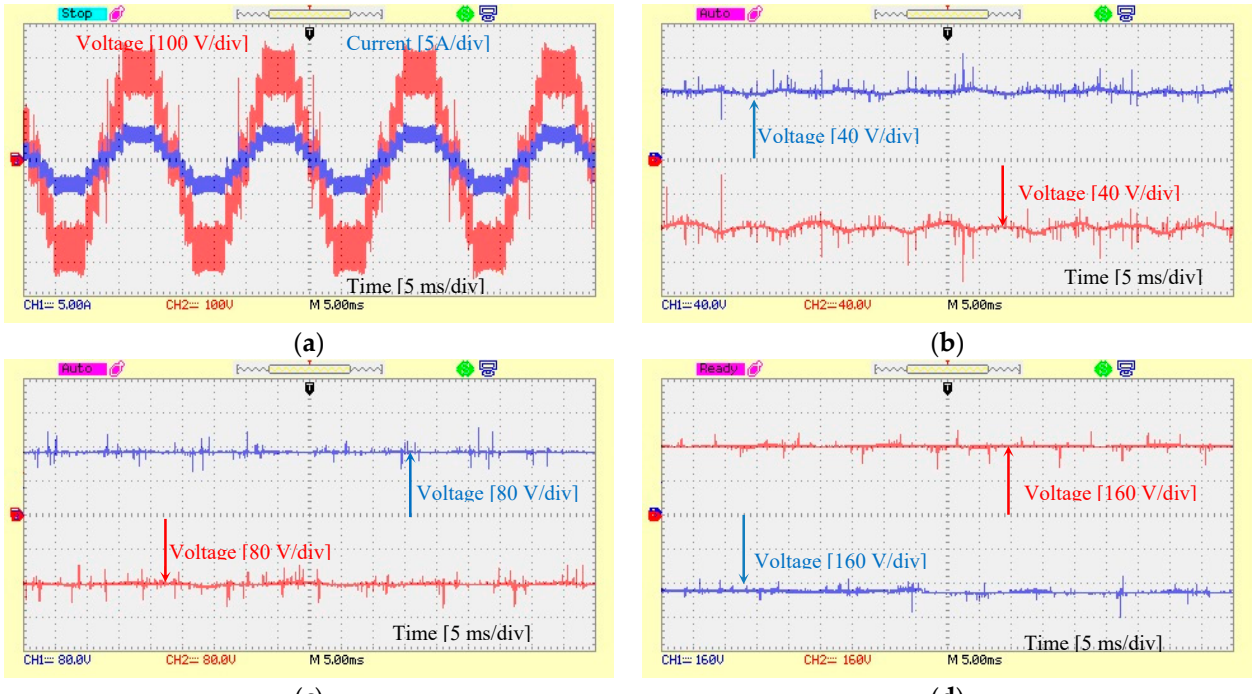
Notably, to do FFT analysis, the output voltage should be obtained in the absence of a filter. The developed output voltage under no-load condition is shown in Figure 19a. Meantime, to the end of assessing the quality of the output voltage, the FFT analysis was also illustrated in Figure 19b. Whereas the harmonics mostly appeared around the switching frequency, which can be readily canceled out by virtue of some small filters.



(**a**) (**b**)

Figure 19. Performance of the proposed inverter: (**a**) Output voltage under no-load conditions; (**b**) FFT analysis of the voltage signal.

Considering a resistive load of 0.8 kW, the output voltage, input current, and capacitor voltages were scrutinized. The developed output voltage and load current during the abovementioned condition is exhibited in Figure 20a. Moreover, the capacitor voltages are shown in Figure 20b–d. Due to the load current that discharges the capacitors in discharging modes, a voltage ripple appeared on the capacitor voltages. This caused some small ripple on each voltage level, as seen in Figure 20b. Since these voltage ripples were insignificant, they cannot cause a problem.

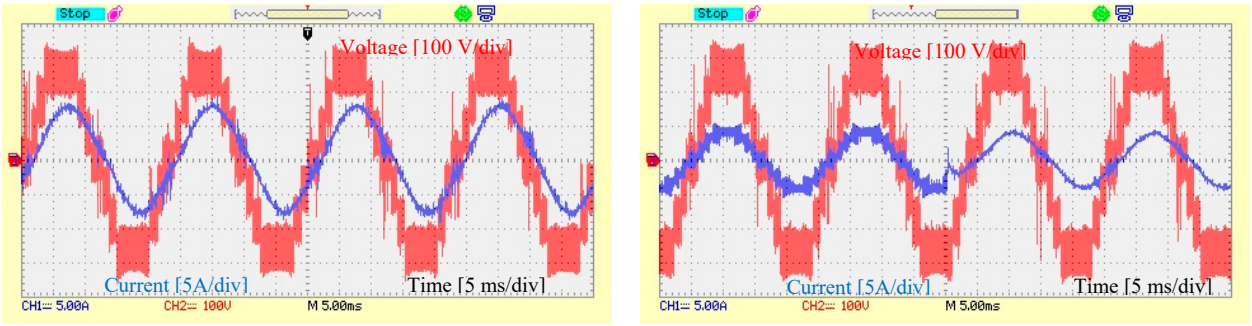


(**a**) (**b**)

(**c**) (**d**)

Figure 20. Performance of the inverter while feeding purely resistive load: (**a**) Load-side voltage and output current of the inverter (**b**–**d**) voltages of the capacitor in the first, second, and third cells, respectively.

Inverters are required to supply reactive power upon demand. For investigating the viability of the suggested inverter to supply the reactive power, two scenarios are considered. In the first scenario, the output load was considered 1.2 kVA with lagging PF of 0.94. The output current and voltage at this condition is depicted in Figure 21a. In the second scenario, the dynamic behavior of the inverter was investigated. In this scenario, the prototype was firstly loaded by a resistive load of 0.8 kW, then it was switched to another type of load, which consumed 0.75 kW + 0.28 kVar. The result is illustrated in Figure 21b. The results prove that the proposed inverter can deal with different loading conditions.



(**a**) (**b**)

Figure 21. Performance under different loading conditions: (**a**) Output voltage and load current under resistive-inductive load; (**b**) output voltage and load current under dynamic loading condition.

9. Conclusions and Future Works

In this study, a SC-based MI for PV applications was suggested. The presented topology is composed of one half-bridge and several basic cells. The leakage current is one of the concerns of PV systems. In addition, the other concern is the low amplitude of the voltage of PV modules. This topology can eradicate the leakage current and provide high-quality boosted ac voltage. In the proposed high step-up MI, the common mode voltage (CMV) oscillates with grid frequency and so does the leakage current, resulting in a mitigated leakage current. The capacitors utilized in the proposed topology are charged spontaneously without any active switch and complicated control approach. Another challenge of modern PV grid-connected systems is their lifetime distribution and identifying the weakest components in a reliability point of view. In this regard, the unreliability curves of the semiconductor devices and the overall system are derived to determine the *Bx* index. This reliability index showed the worst predicted lifetime of the proposed inverter. The presented lifetime evaluation showed that the switches S1 (or S2) and S5 (or S6) in the proposed inverter have a dominant share in failure. Thus, the proper design of these switches and their cooling system can improve the overall lifetime.

Considering a grid-tied PV system in Matlab/Simulink, the performance of the proposed topology was investigated by assuming various active and reactive powers injecting into the grid. Moreover, the performance of the suggested topology was validated by a laboratory-scaled prototype. The exhibited results in Simulink and experimental results validated the ability of the presented topology to develop high-quality voltage, limiting the leakage current and providing reactive power.

For future work, it is recommended to assess the performance of the proposed inverter under grid voltage sags, non-sinusoidal voltage, and grid voltage distortion conditions. Another interesting research topic is to improve the performance of the proposed inverter by optimizing the design and control parameters to increase efficiency and stability under abnormal conditions.

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Conflicts of Interest: The authors declare that they have no known competing financial interests or personal relationships.

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