

Article

Analysis of Internal Signal Perturbations in DC/DC and DC/AC Converters under Arc Fault

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Abstract: The constant increase in electrical energy consumption has led to a growth of photovoltaic installations (PV) along with the corresponding power converters for proper operation. Power electronics converters represent a challenge to maintain the system's performance and safety; one such problem is series DC Arc Fault (AF). DC AFs lead to fire risk, damaging the main bus and the loads when not detected and interrupted in time. Therefore, research about DC AFs in power electronics converters must be carried out to predict the behavior and help avoid damage to the system. In this work, an innovative hybrid multilevel inverter for PV applications is used to explore the effect of series DC AFs in the converters' internal signals, with the aims of setting the bases for the development of a detection system for power electronics. Both stages of conversion (DC/DC and DC/AC) are presented. In addition, the placement of the MPPT converter was considered for the tests. The AF experimental tests were performed with a generator based on the UL1699B specifications. The measurements of signals were performed in strategic points of the DC side, and changes and how to exploit them are discussed. This study contributes to a better understanding of the DC AF phenomenon and provides new insights for the development of new PV system protections.

Keywords: series DC Arc Faults; hybrid converter; direct current converter (DC/DC); direct to alternative current converter (DC/AC); multilevel inverter; photovoltaic (PV) systems



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1. Introduction

In recent years, PV generation systems are becoming one of the main technologies that will guarantee zero emission energy generation. In 2020, the Energy Information Administration (EIA) published the Annual Energy Outlook (AEO), a projection of energy demand for the US. This study predicted with a certain grade of certitude the energy demand from now to 2050. It is based on the AEO National Energy Modeling System (NEMS), an integrated model that captures interactions of economic changes and energy supply, demand and prices [1].

According to this study, the generation of energy utilizing renewable sources such as wind or solar PV is going to be the main energy source of the future: solar PV will represent 46 % of the total production and wind generation 33% by the year 2050.

Investments in renewable energies are made many other countries. Considering the continuous increase in power and size of PV systems, continuous and safe operation needs to be assured, as discussed in [2].

PV systems deterioration is linked to exposure to the elements such as weather, salinity, etc., which lead them to fail over the years. In this case scenario, insulator deterioration is likely to happen, causing various problems including DC AF [3]. It is estimated that the annual power loss due to faults is around 18.9%.

The temperature of an AF oscillates around 3000–8000 °C in some cases, which is enough to melt glass, copper, aluminum and start combustion of the surrounding materials. In addition, fire incidents may result and cause casualties [4]. To predict the future needs for PV systems protection, among the possible types of faults in PV panels, this work focuses particularly on the DC arc fault phenomenon. The most common types of DC AFs are series and parallel [5]. The challenge for Arc Fault Detectors (AFD) is that, in DC series AFs, the post-arc current is smaller since the AF is in series with the load.

Regulation standards such as the NEC690.11 of the National Electrical Code (NEC) and UL 1699B by Underwriters Laboratories Inc (UL) have become the basis for many PV AFD and Arc Fault Circuit Interrupter (AFCI) approaches proposed in the literature.

Since the AF behavior can be easily influenced by external factors such as antenna effects, crosstalk, inverter noise, inverter switching harmonics, PV cell, PV system topology and the health of the modules [6], the challenge of developing a detection system that can function properly despite the aforementioned disturbances is a constantly evolving field of development.

A PV system is mainly built as presented in Figure 1; however, the fundamental block of energy production is the power converter (DC/AC inverter). The various architectures proposed in the literature to achieve this conversion have been greatly influenced by industrial needs. This is reflected in the first-ever publication on a three-level inverter [7]. The Multilevel Converters (MLCs) was first intended to overcome the power limitation of the switching devices of that time. The concept of employing a series of low power cells to perform the conversion was presented 40 years ago [8,9].

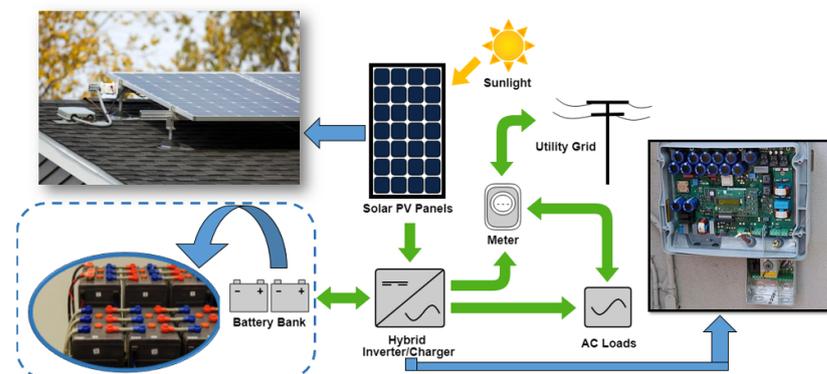


Figure 1. Main structure of a PV installation.

The first-ever patent for three-level inverters and Multilevel Inverter (MLIs) was in 1983.

The original idea of MLIs was to multiply the power performance by employing multiple cells in series and clamp the voltages between them. A patent appeared in 1975 [10], in which the term “cascaded inverter” was first defined, which was formed by an arrangement of full H bridge cells connected in series fed by independent DC sources [11]. Since all PV installations use a DC/AC converter to exploit the energy produced, it is fundamental to have a deep understanding of the effects of the AF in them, as well as in the main conversion and regulation blocks.

Conventional AF detection techniques are based on specially conceived algorithms that exploit the frequency signature of strategic measured signals; depending on the approach, the harmonic content of the signals can be used as a base for detection [12]. Based on the variations, the results can be compared to reference harmonics to recognize whether an AF is present in the DC system. This method was proposed by J. Johnson and F. Schimpf [5,13,14]. Other factors such as the inverter noise injected into the PV string has to be considered. This due to the fact that inverter switching can generate harmonics from 1 to 100 kHz [15]. In the early base bands of frequency, the identification of changes caused

by an arc is optimal. Nonetheless, F. Schimpf stated that a current frequency signature with a magnitude of around -70 dB can be modified depending on the converter type. Two different power inverters are used in his study, which caused magnitude changes of around -40 and -20 dB, respectively. It is important to note that, in this comparison, the AF event is not yet considered in the analysis, and the changes in the very low- and low-frequency bands are noticeable. Depending on the PV system topology, the impacts of AFs may vary. In a single string test, the DC V/I will suffer a drop, due to the sudden increase in impedance from the AF event; this characteristic was proposed and explored to evaluate its potential for detection AFs in DC by L. Mackay [16]. In these related works, and as presented by Madeti and Singh [12], no particular approach that uses the converter behavior as a base for detection is considered.

This work contributes with an in-deep study of the behavior of experimental signals on both DC/DC and DC/AC converters in an DC AF scenario. An MPPT module and the location of the AF are also considered. To obtain these results, the protocol followed for AF generation and the main schematic configuration and values are described in Section 2. In Section 3, justification for the converter selection and its functioning is detailed, followed by the study of both DC/DC and DC/AC converters facing an AF in Section 4. In Section 5, the AF effect in the behavior of MPPT regulation is detailed for two cases: AF before the MPPT and after the module. Section 6 discusses the contributions of this work and how this sets the basis for future works.

2. DC Arc Fault Generation Protocol

In this section, the protocol to study the DC AF phenomenon is described. The specifications are based on the UL 1699B norm [5], where the main outlines for the study of different AF types in PV systems such as series and parallel, the types of loads involved, detection times and the proper method for generation of AF are presented. In this work, the series arcing test is studied. The Arc Fault Generator (AFG) presented in Figure 2 is used to analyze the effect of series AFs in power converters. This mechanism is based on the Electrode Distancing Ignition (EDI) technique.

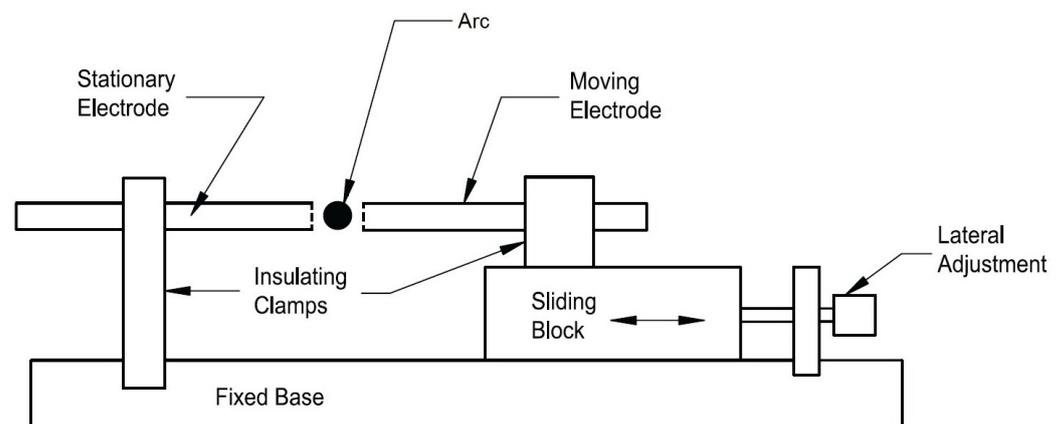


Figure 2. UL1699B AF generator mechanism schematic.

The electrodes can be separated by using the lateral adjustment mechanism, placing the movable electrode at the desired gap. The electrode material employed for the tests is graphite and copper, of 6 mm diameter. Two adjustable fixing knobs are added to the apparatus at the end of the graphite electrodes, as presented in Figure 3.

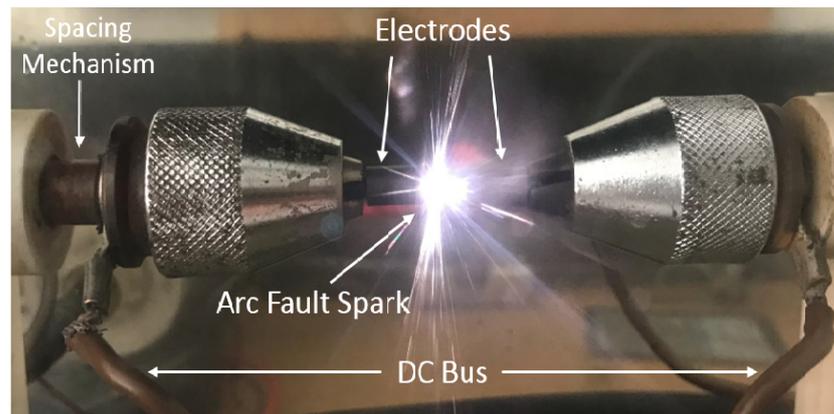


Figure 3. UL1699B-based AF generator mechanism.

The PV power source can be either PV panels or a DC conventional source that possesses similar characteristics to a PV array in normal conditions. In this study, we adopted the use of ideal DC sources to supply the converter topology chosen. The block diagram presented in Figure 4 is an optimal circuit that permits analyzing the internal voltage and current fluctuations caused by the apparition of the series AF. Figure 5 shows the experimental test bench used during the totality of tests. Table 1 lists all the component values, switching frequencies, and input voltage for the experiments.

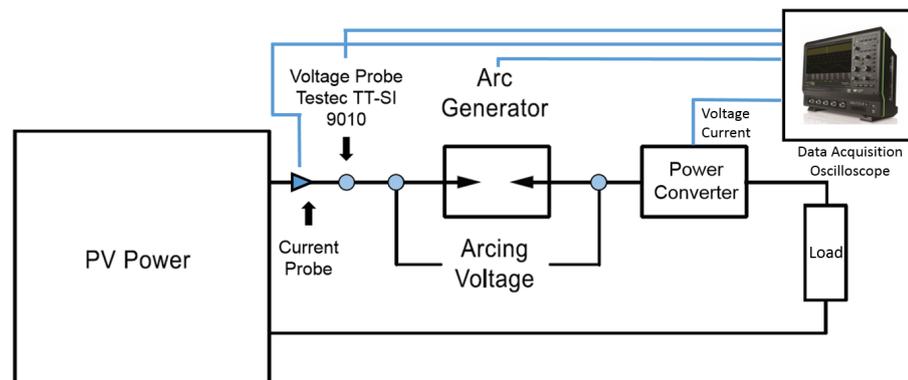


Figure 4. AF load study schematic diagram.

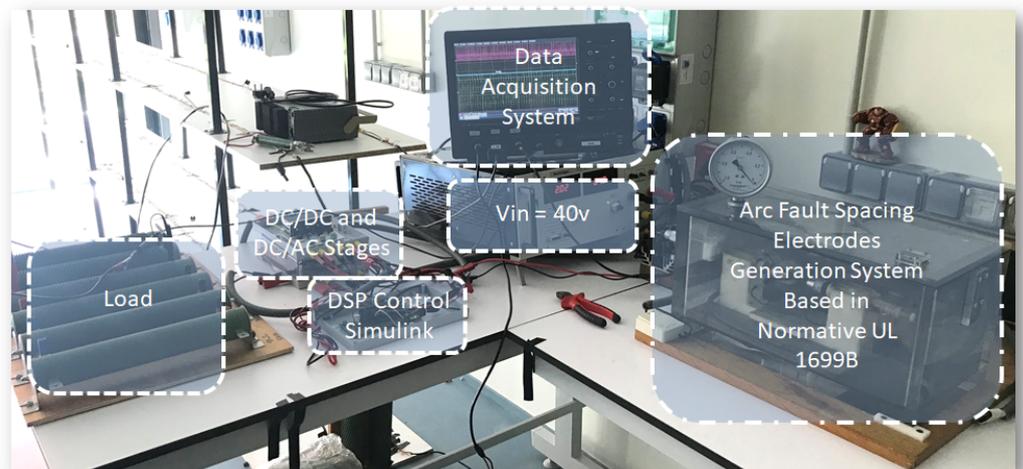


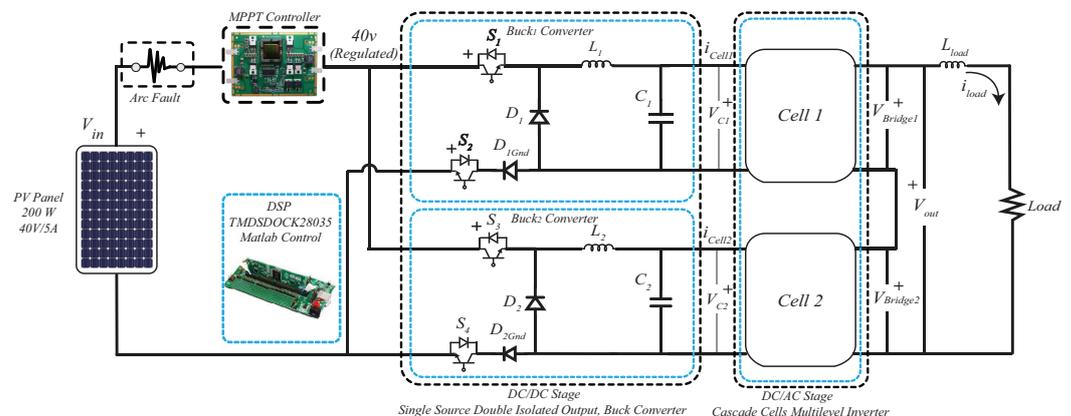
Figure 5. Experimental test prototype.

Table 1. Simulation and implementation values.

Components	Values
Frequency	2 kHz
Duty Cycle 1	45%
Duty Cycle 2	32%
L1	438 μ H
L2	438 μ H
C1	2200 μ F
C2	2200 μ F
Load	47 μ
V_{in}	40 V
V_{out}	50 V_p (100 V_{pp})

Converter Configuration for Arcing Test

The overall schematic diagram of the converter employed in this study is presented in Figure 6. The nominal MPPT operational voltage is 40 V, also corresponding to the MPPT controller maximum operating voltage. The prototype is based on the information in Table 1, where all the component values, switching frequencies and input voltage are cited. The AF generator is immediately connected after the DC source in series with the main converter circuit, and then both DC/DC and DC/AC conversion stages are connected and controlled by using Matlab/Simulink rapid prototyping board developed by Texas Instruments (Model TMDSDOCK28035). The experiments were performed at an ambience temperature of 20 °C and the gap between electrodes when the arc occurs was set to 1 mm.

**Figure 6.** Overall converter diagram for arc fault test.

3. Converter Topology Selection and Functioning

Across this section, the background of the selected converter is presented. In Figure 6, the main structure of the employed converter is presented, and each of the function blocks is also highlighted. This converter was employed to study AFs due to the characteristics and advantages it possesses compared to other converters discussed in this section. A second reason is that there are multiple strategic V/I internal signal points of measure available, which would contribute to a better understanding of the AF phenomenon in power converters.

To commence with the analysis of the converter selected, the main features used as criteria on each converter are the numbers of switching devices, diodes, inductors and capacitors. Other key factors are the achievable number of levels generated at the output, the regulation capabilities of the converter (if applicable) and whether galvanic transformers are used.

The converter in [17] achieves a low-distorted nine-level output using twelve switching devices; a downside to be considered is that this converter needs to be feed with a higher voltage input than the desired output. The authors of [17–19] produced the same

nine levels at the output, which is a positive feature, but the development in [20] is also able to achieve nine levels by using fewer components. This last feature is highly priced in the actual trend of power converter development since it helps to increase power density and reliability. The converter in [21] generates seven levels by only using ten switching devices, which is possible by connecting in series two three-level flying capacitor topologies divided by half bridge cell; the only required condition for it to work properly is to pre-charge the capacitors at $V_{dc}/2$, $V_{dc}/3$ and $V_{dc}/6$. This arrangement is possible thanks to the innovative balancing control proposed in the work. The converter in [22] presents an attractive option since it uses a low number of components and possesses a voltage elevation feature; unfortunately, the converter makes use of a galvanic transformer. The elevation and reduction of voltage is a feature that is less common in converters that generate multiple voltage sources from a single source; four examples of these converters are presented in [20,22–24]. The next converter, presented in [25], uses a clever arrangement of replacing one of the DC sources by a large capacitor. The downside of this converter is that the voltage of the DC source and the capacitor needs to be carefully controlled, otherwise the output generated will be distorted. The converters proposed in [21,26,27] also generate only five levels at the output, decreasing the performance of the proposals compared to the rest of the cited converters. Focusing in the converters found in [23,24], both remain strong proposals since no transformer is used and the output generates a relatively high number of levels. However, the authors of [17,18,20] could achieve a better output using fewer components. Two converters that replace the input source with a capacitor are presented in [27,28], but the problem related to stable capacitor balancing can be challenging in high-power applications, as explained in both works. Similarly, in [21], a five-level converter with a lower number of components compared to those in [25,27,28] is proposed, but it also has the balance control problem. The design techniques in [19,22] also stay behind the other cited works due to the use of transformers compared to the rest of the converters [18,21,23–31]. Thanks to the review of the related single sourced converters, we can conclude that the double buck converter used in this study possesses strong features and will allow a proper characterization of the variations found with the apparition of an AF on the DC side.

The next section briefly explains the functioning analysis of the converter selected for this study. In addition, the detailed functioning and V/I signals for each switching state are presented in [17,20] for the buck and boost variants, respectably.

3.1. Operational Principle of Selected Double Buck Converter

In the converter architecture of Figure 6, $buck_1$ and $buck_2$ blocks have two possible switching states each, first when S_1 and S_2 (S_3 and S_4 for $buck_2$) are in conduction state (*on*) ($S_1 = 1, S_2 = 1$) and a second state when *open* (*off*) ($S_1 = 0, S_2 = 0$). The four possible topological combinations that can be achieved for this configuration of parallel connected converters are presented in Table 2. The strategy is to alternate the power extraction from the DC sources, which is possible by the phase delay of 50% applied between m_1 and m_2 , as described in Equations (1) and (2). The states $S_1 = 1, S_2 = 1$ and $S_3 = 1, S_4 = 1$, where both converters will be (*on*) at the same time, have to be avoided to conserve the isolation between $buck_1$ and $buck_2$. This is one limitation of this parallel buck topology since the maximum duty cycle is of 50%.

State 3 in Table 2, where $S_1 = 1$ and $S_2 = 1$, is presented in Figure 7, considering that i_{DC1} follows its path from V_{in} to the series circuit given by S_1, L_1, C_1, D_{1Gnd} and S_2 . In this case, diode D_1 is not polarized. In this same state, $buck_2$ converter is in state $i_{L2_{off}}$, which means that the current is only dependent on V_{C1} , as described in Equation (4), and, when S_1 is in logical State 1, i_{L1} is obtained with Equation (3).

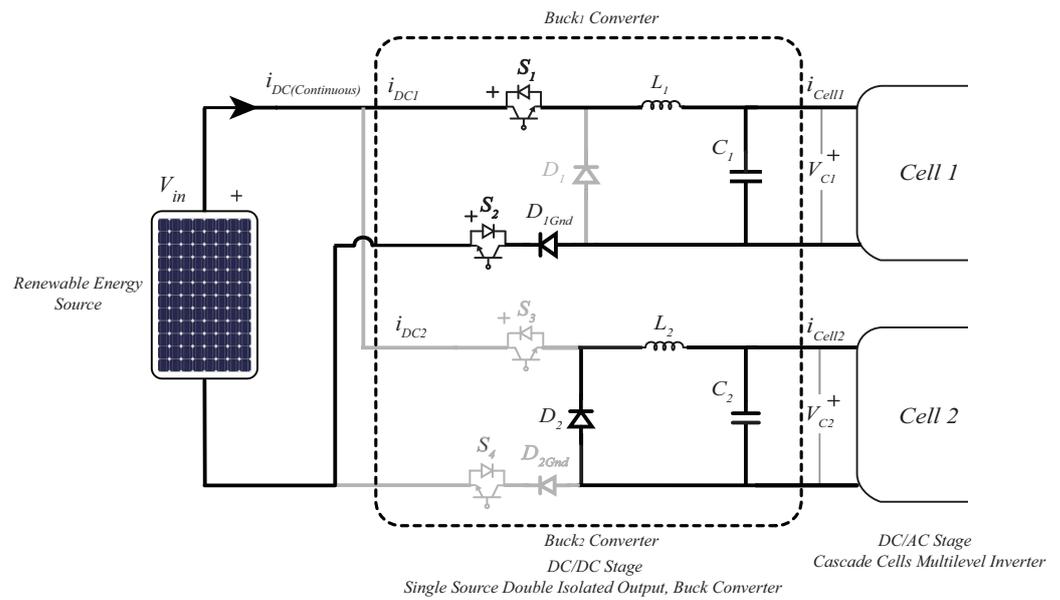


Figure 7. Proposed buck variant topology in switching state $S_1=1, S_2=0$ with highlighted currents paths.

Table 2. Buck combinational states.

States	S_1	S_2	iL_1	iL_2	iD_1	iD_2
1	0	0	$\frac{V_{C1}}{L_1} \frac{t_{1off}}{T}$	$\frac{V_{C2}}{L_2} \frac{t_{2off}}{T}$	on	on
2	0	1	$\frac{V_{C1}}{L_1} \frac{t_{1off}}{T}$	$\frac{(V_{in}-V_{C2})}{L_2} \frac{t_{2on}}{T}$	on	on
3	1	0	$\frac{(V_{in}-V_{C1})}{L_1} \frac{t_{1on}}{T}$	$\frac{V_{C2}}{L_2} \frac{t_{2off}}{T}$	off	off
4	1	1	Prohibited	Prohibited	off	off

Considering that:

$$m_1 = \begin{cases} 1 & \text{when } Duty_1 > Carry_1 \\ 0 & \text{when } Duty_1 < Carry_1 \end{cases} \quad (1)$$

$$m_2 = \begin{cases} 1 & \text{when } Duty_2 > Carry_2 \\ 0 & \text{when } Duty_2 < Carry_2 \end{cases} \quad (2)$$

$$\Delta i_{L1on} = \frac{1}{T} \int_0^{Duty_1 T} \frac{(V_{in} - V_{C1})}{L_1} dt = \frac{(V_{in} - V_{C1})}{L_1} \frac{t_{1on}}{T} \quad (3)$$

When S_1 is in logical State 0, the current through the inductor L_1 is expressed as,

$$\Delta i_{L1off} = \frac{1}{T} \int_{Duty_1 T}^T \frac{-V_{C1}}{L_1} dt = \frac{-V_{C1}}{L_1} \frac{t_{1off}}{T} \quad (4)$$

State 2 in Table 2, where $S_1 = 0$ and $S_2 = 1$, is presented in Figure 8, considering that i_{DC2} follows the path from V_{DC} , through S_3 and L_2 , to end in C_2 , closing the circuit to ground (D_{2GND}) and S_4 . In this current mesh, D_2 does not get polarized. Parallel to this process, the buck₁ switching state is i_{L1off} , meaning that current is only dependent of voltage V_{C2} .

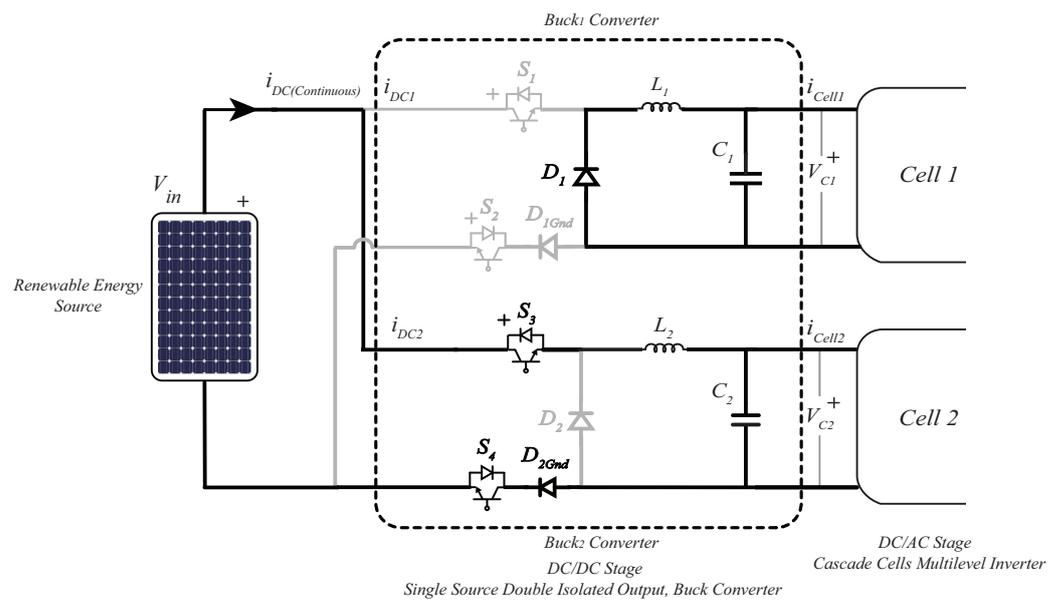


Figure 8. Proposed buck variant topology in switching state $S_1 = 0, S_2 = 1$ with highlighted currents paths.

In Table 2, the conduction state of the diodes in each switching combination is also presented. In any moment, switch *buck*₁ or *buck*₂ holds a logical State 0.

This novel DC/DC topology with the two variants boost and buck is ideal for use with multilevel DC/AC inverters as an elevation stage capable of generating two isolated DC outputs from a single source and elevating up to 1:10 the input voltage by using no extreme duty cycles.

3.2. Simulation Results of Double Buck Converter

With the theoretical bases that rule the functioning of the double buck converter presented in the previous section, we can proceed with the analysis of the simulation results of the converter variant used for this study. To obtain these results, the schematic diagram of Figure 6 was employed as reference and Matlab Simulink software was used for simulations.

The required duty cycle of *m*₁ and *m*₂ can be adjusted depending of the desired output voltage; for this study, we selected $V_{C1} = 30$ V and $V_{C2} = 20$ V. With the selected parameters, the simulation waveforms of $V_{Bridge1}$, $V_{Bridge2}$, V_{out} and i_{out} are presented in Figure 9.

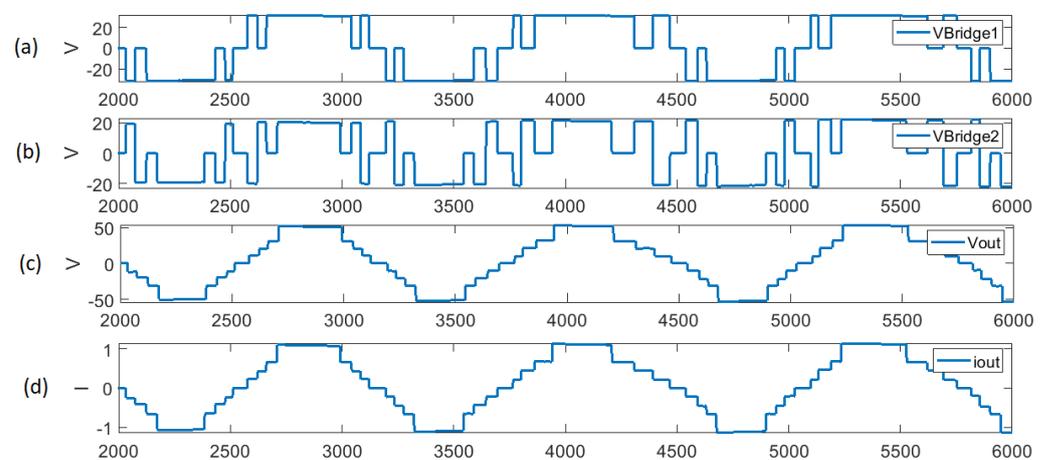


Figure 9. Simulation results of the proposed DC/AC topology: (a) $V_{Bridge1}$; (b) $V_{Bridge2}$; (c) V_{out} ; and (d) I_{out} .

With these results obtained, the correct functioning of the converters under normal conditions was validated. To characterize the converters behavior in a simulation scenario, an AF model is needed, but, since each mode of the arc has advantages and disadvantages, in this study, we adopted the approach of characterize the behavior of DC/DC and DC/AC converters facing a real AF. Thus no modeling of the AF was performed; instead, each converter configuration was set to face the AF in the experimental test bench.

4. Power Converter under AF-DC/DC Converter

To begin the study, a fundamental understanding of the waveforms involved in each stage of the PV inverter is crucial to conceptualize an innovative DC AFD strategy. Additionally, a deep comprehension of changes involved with the AF apparition is essential. This observatory stage of the development aimed to evaluate possible exploits for an effective detection criterion. For this reason, the AF study was separated in two parts, first by generating the fault only in the DC/DC converter and second in the DC/AC stage. The first test was performed by generating an AF located on the DC bus and measuring the values V_{C1} , i_{C1} , V_{arc} and i_{DC} highlighted in the schematic diagram of Figure 10. DC/DC converters are well known for their effect on the input current waveform due to their switching behavior, which modifies the constant input current i_{DC} . When the AF appears, an aleatory drain of current is produced, perturbing the extraction of energy of the DC/DC stage, which in turns alters the typical waveform of the converter.

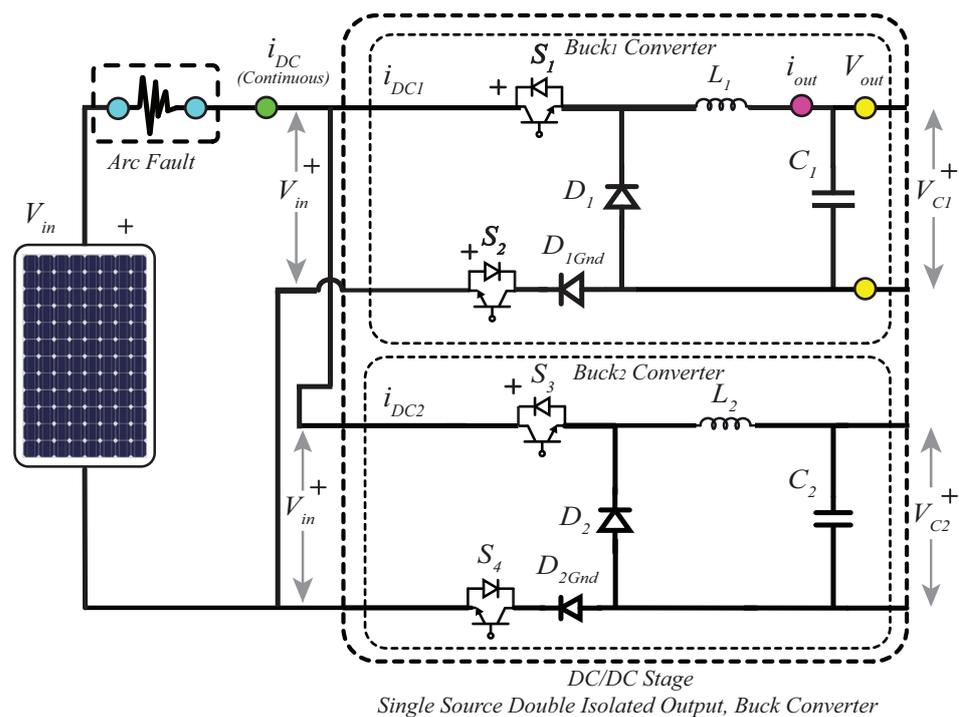


Figure 10. Highlighted DC/DC stage measurements.

The response of the DC/DC converter is presented in Figure 11. The output voltage V_{out} (C1) and current i_{out} (C2) are correctly regulated just before the apparition of the AF. Once the AF ignites, both voltage and current are affected. During the initial 1.8 s, the arc current consumption remains low, but, when the arc reaches a fully sustained state, both voltage and current are severely affected (3 s after the AF) and strong perturbations are visible. In this experiment, we can appreciate how the AF continues to produce aleatory changes in V_{out} and i_{out} until it disappears from the system. Signals V_{arc} (C3) and i_{DC} (C4) help in the interpretation of signals. Since no closed-loop control regulation is implemented, the DC/DC converter follows the arc fluctuations as long as the arc persists. The signals V_{arc} and i_{DC} , as also presented in Figure 11, help determine if the disturbances

present in V_{out} and i_{out} are truly caused by the presence of an AF, which is achieved by verifying whether V_{arc} is different from zero during the time t under study. This experiment allowed us to conclude that the DC/DC stage converter in an open-loop control will limit its functioning to follow the fluctuations of an AF. To analyze the signals, in the next experiments, the same protocol was followed.

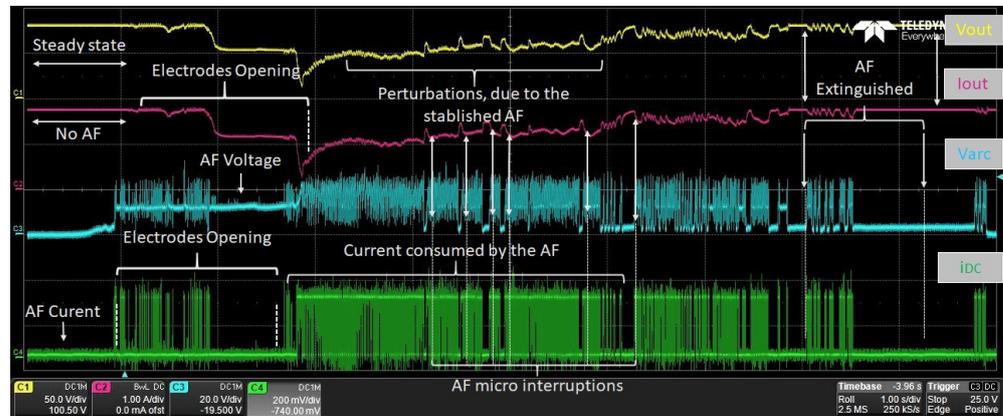


Figure 11. Conventional DC/DC boost converter behavior, before and after an AF.

Power Converter under AF-DC/AC Converter

As observed previously, the AF perturbations produce fast random voltage and current variations in the DC/DC output. With those results obtained, we proceeded to study the cascade cells DC/AC converter behavior under the AF presented in Figure 12. The strategic point of measurement for this case are V_{arc} , i_{Cell1} , i_{out} and V_{out} highlighted in Figure 12.

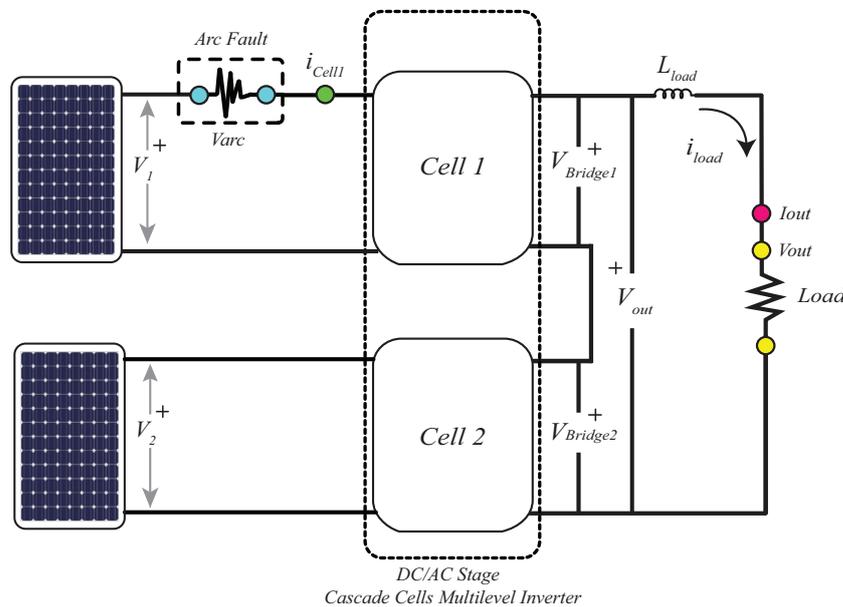


Figure 12. DC/AC Cascade cells configuration for AF testing.

Figure 13 shows the results for the AF DC/AC test. The left side of the figure shows a near perfect nine-level waveform measured in V_{out} (C1) and I_{out} (C2), respectively, and the arc voltage V_{arc} (C3) and the supplied current i_{Cell1} (C4). With the AF apparition, the signal V_{out} suffers an important deformation, which is due to the fast variations not handled by the precedent DC/DC converter. The perturbations of the arc affect the voltage balance ratio needed between $V_{Bridge1}$ and $V_{Bridge2}$ for a correct operation. The phenomenon is present in both V_{out} and I_{out} , where the number of levels generated is reduced randomly, causing a lost of symmetry.

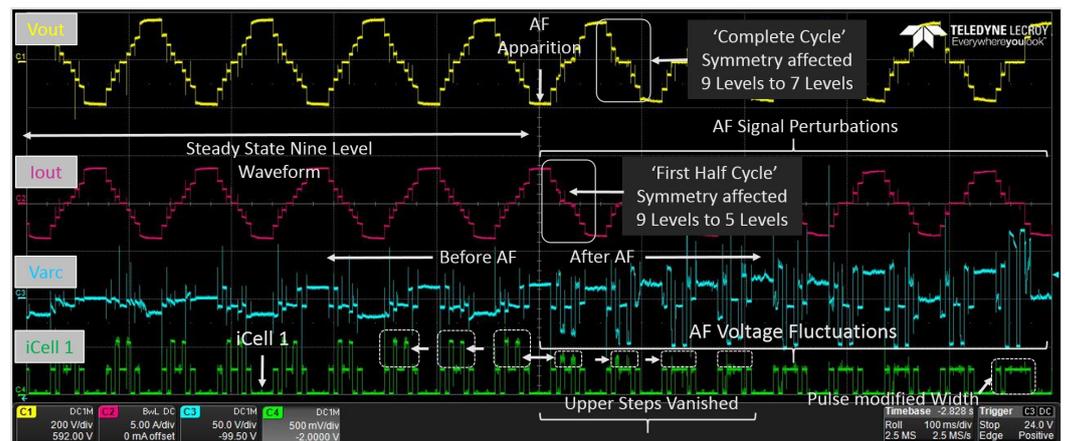


Figure 13. DC/AC cascade cells' configuration for AF testing.

During the AF, V_{out} and I_{out} are perturbed and the nine-level generation is altered, causing the magnitude of each voltage step to vary randomly, also causing the number of levels to drop from nine to only five. Then, a complete cycle after the AF apparition, it passes to seven levels. The current i_{Cell_1} (C4) has similar changes when the AF is established, as shown in Figure 13. In this case, the most noticeable change is that the current signal loses the totality of the upper switching steps, and, during the last cycle, a width step change is observed. This effect is directly proportional to V_{arc} variations amplitude, and it is also observed that i_{Cell_1} loses its periodic behavior with the AF. With these two cases of AF tested, it is possible to conclude that the changes in voltage and current at the strategic points of measure can be exploited to achieve the detection of AFs, as will be studied in a future work. Nonetheless, in the two cases presented, the maximum power point tracking (MPPT) converter influence is not yet considered. For this reason, its functioning when facing an AF is presented in the next section.

5. Arc Fault Influence in a MPPT Tracking System

To ensure the optimum power extraction from the solar installation, an additional DC/DC MPPT converter is commonly added to the systems. In the following experimental tests, the same equipment described in Section 2 was used, with the addition of the MPPT control module 'SM72445' produced by Texas Instruments. In Figure 14, the physical module is presented, which is capable of a constant regulation of up to 40 V. The study of the MPPT influence was divided into two cases, generating the AF after and before the MPPT controller. Each case is described in detail in the following two subsections.



Figure 14. Texas Instruments MPPT prototyping board and typical application circuit.

5.1. Single Phase Arcing before MPPT Module

Figure 15 is used to analyze the influence of an AF when the arc is located before the MPPT converter.

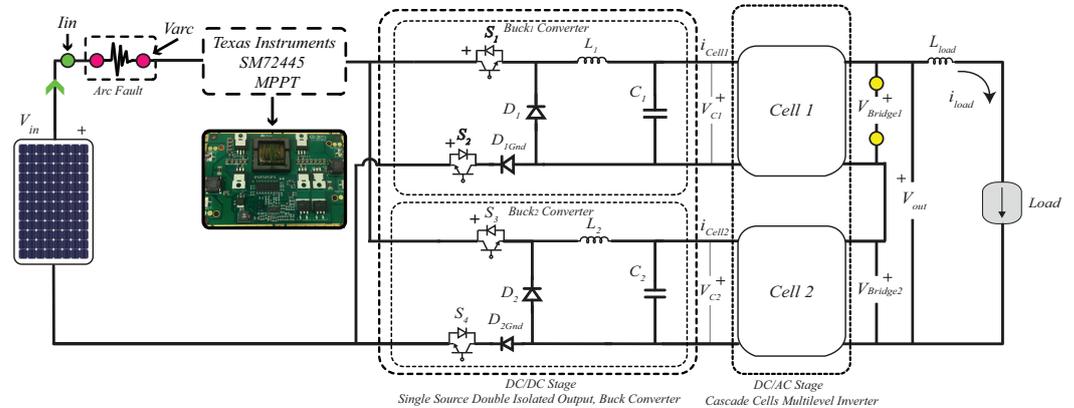


Figure 15. Schematic diagram for AF testing with the AF before the MPPT module.

In this test, the data acquisition of three waveforms ($V_{Bridge1}$ (C1), V_{arc} (C2) and I_{in} (C3)) was performed, as shown in Figure 16. V_{arc} is an essential signal to confirm if the fluctuations in C1 and C3 are related to the AF appearance.

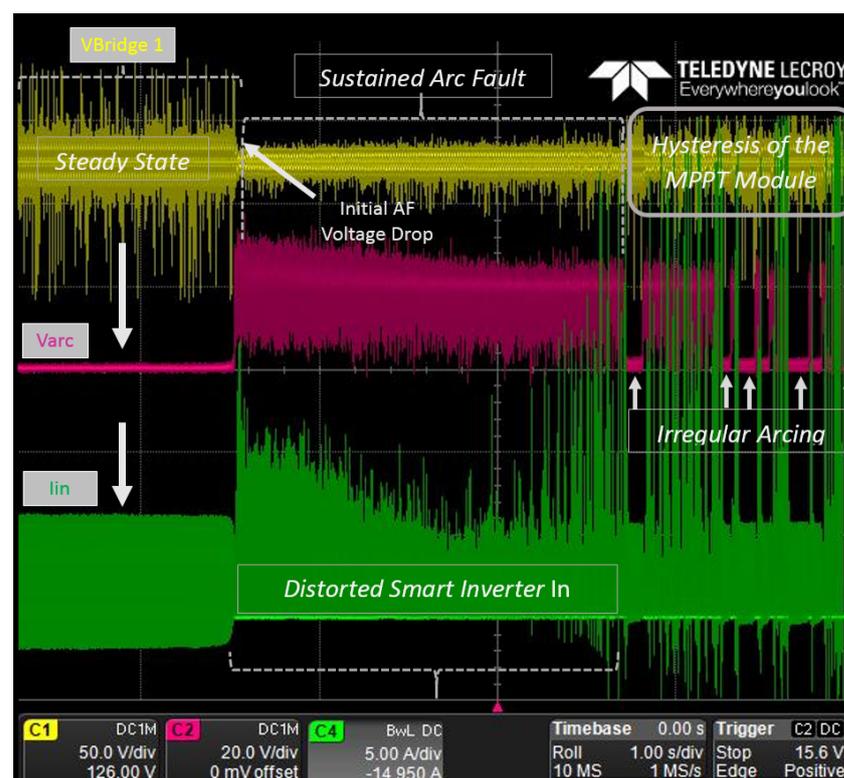


Figure 16. Experimental results of arcing before the MPPT module.

The AF esd generated in the main DC bus and signals were acquired across a time length of 5 s. In $V_{Bridge1}$, an initial drop in voltage is observed when the AF ignites; this drop is proportional to the AF sustained voltage. V_{arc} remains constant until the MPPT controller begins to compensate the loss in $V_{Bridge1}$ caused by the arc. Although the MPPT control module will attempt to keep the output at the nominal 40 V, the regulation is not successful since the fault surpasses the elevation capabilities of the converter. This means that, after reaching the MPPT operation limit, it will follow the aleatory fluctuation

generated by the arc. Even when the arc is extinguished from the system, the MPPT converter algorithm is not capable of recovering its steady state functioning, so the voltage starts to distort even when the fault has stopped. This phenomenon can be observed in the current I_{in} presented in C4.

5.2. Single Phase Arcing after MPPT Module

The schematic for the next experiment is presented in Figure 17. The signal measurements are V_{out} , V_{arc} and I_{out} . In this case, the MPPT behaves similarly to the previous case, as can be seen in Figure 18.

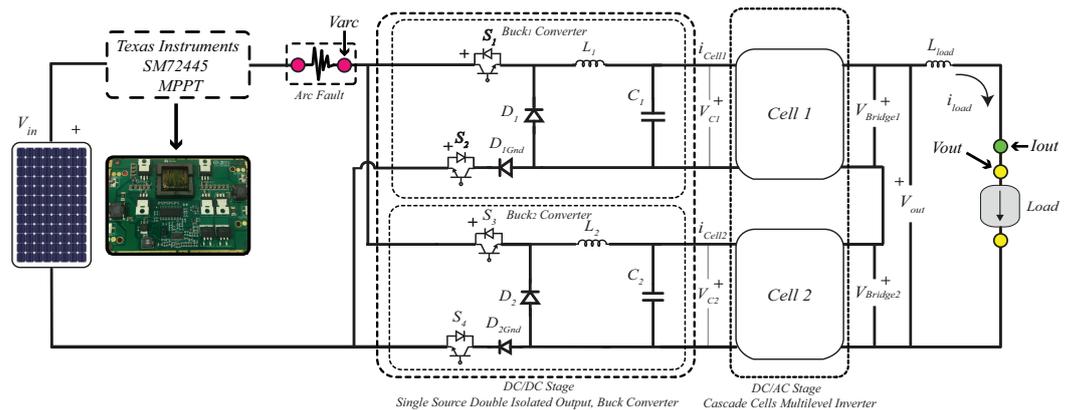


Figure 17. Schematic diagram for AF testing with the AF after the MPPT module.

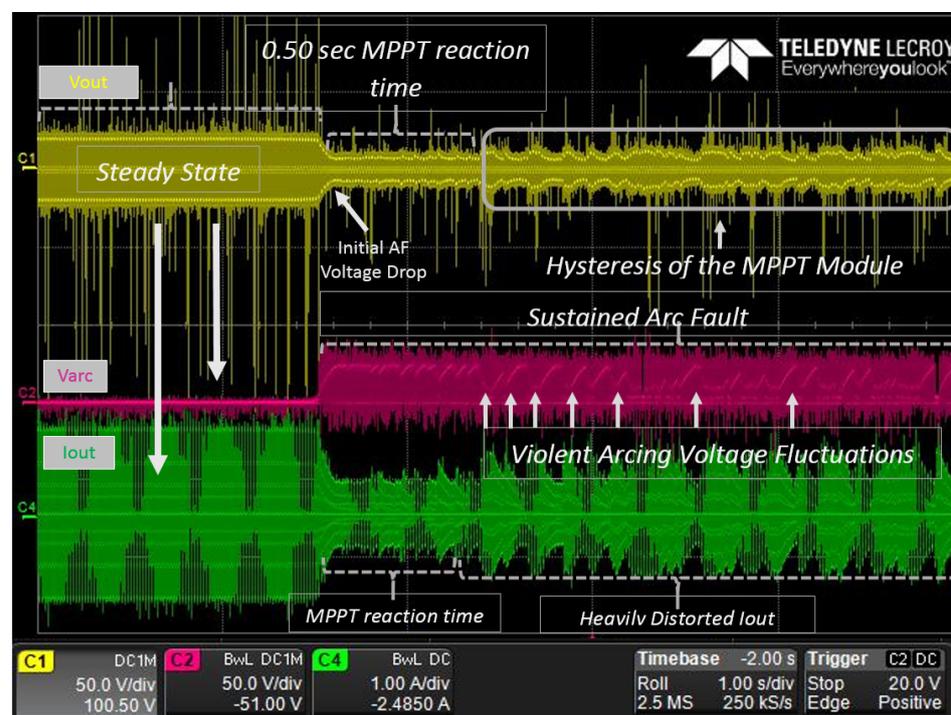


Figure 18. Experimental results of arcing before the MPPT module.

In this case, it is observed that the control algorithm assumes a more active voltage regulation behavior. Nevertheless, the control is still limited by the amount of current that can be delivered by the MPPT controller. Because of this limitation, after approximately 0.5 s of the initial voltage drop (that is, the average reaction time of the MPPT module), the MPPT detects this change, which is traduced in an increased current consumption of the system. To compensate the voltage drop detected, the MPPT module increases the

current, this starts a vicious counter reaction, because by increasing the delivered current, the AF proportionally increases its current consumption. It is mentioned above why the fluctuations in V_{arc} (C2) increase after the MPPT reaction time, which is shown in I_{out} (C4) of Figure 18. With both cases of MPPT facing an AF, we can conclude that this module is also strongly affected by the AF. The control loop malfunctioning causes fluctuations in V_{arc} (C2), thus affecting in an important manner V_{out} and I_{out} .

6. Conclusions and Future Works

This study contributes with a deep analysis of the converter internal signals when facing a series AF. Different configurations are presented, which is fundamental to the development of a more efficient and secure power inverter that can integrate the detection of AF's.

Thanks to the results obtained by using an innovative hybrid converter, it was possible to set a solid base for future developments. Given the various stages in the energy conversions tested (MPPT, DC/DC and DC/AC), the AF understanding is enlarged and important facts are summarized as presented below, which are all based on a real experimental test bench scenario.

- The various points of measurement in both DC/DC and DC/AC converters are affected by the appearance of an AF, which is studied and discussed in Section 3
- When studying the DC/DC converters, when facing an AF in an open-loop control, the variation caused by the AF will be followed by the DC/DC converter modifying the voltage and current output proportionally to the AF sustained values (and following the rapid variations).
- An additional contribution of this work is the experimental study of the arc-fault influence in the MPPT behavior when the fault is produced either before or after the MPPT converter. This experimental study allows us to confirm that the arc-fault location after the MPPT has a higher influence in regulation capability compared to the arc-fault location before the MPPT, as discussed in Section 4.
- DC/AC topologies are highly dependent on the supplied voltage to each cell (especially in cascade cells configuration); if the AF causes a perturbation in the prior DC/DC stage (hybrid converter), the multilevel signal will be affected. The implications of this under different experimental scenarios with different types of loads will be presented in detail in a future work.

The detection of AF in DC systems is a challenging topic, especially if the converter configuration, type of load, solar radiance variations and distance between AF electrodes, among other common factors present in PV installations, are considered. For this reason, a characterization of the basic blocks of conversion facing an AF was addressed. In a future work, a DC AF detection technique based on the results presented in this publication will be presented and detailed with both simulation and experimental results.

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