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Review

A Survey of Neural Front End Amplifiers and Their Requirements toward Practical Neural Interfaces

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Abstract: When designing an analog front-end for neural interfacing, it is hard to evaluate the interplay of priority features that one must upkeep. Given the competing nature of design requirements for such systems a good understanding of these trade-offs is necessary. Low power, chip size, noise control, gain, temporal resolution and safety are the salient ones. There is a need to expose theses critical features for high performance neural amplifiers as the density and performance needs of these systems increases. This review revisits the basic science behind the engineering problem of extracting neural signal from living tissue. A summary of architectures and topologies is then presented and illustrated through a rich set of examples based on the literature. A survey of existing systems is presented for comparison based on prevailing performance metrics.

Keywords: neural recording; analog front-end; neural amplifier; low-noise; review

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1. Introduction

Interfacing electronics with the brain is one of the greatest technical challenges of our era. During the past decade, specialized amplifier circuitry to retrieve weak neural bio-potentials from extracellular microelectrodes has improved dramatically [1]. Such progress enabled to significantly accelerate advances in the field of neural engineering in neural prosthesis, because neural amplifiers are key building blocks of active microelectronic interfaces. Neural interfaces are becoming increasingly important for enhancing our understanding of brain function, and for developing potentially therapeutic and prosthetic applications. Neural interfaces generally aim to utilize the largest number of channels for the study of neurons from specific brain microcircuits. The important design parameters, such as power consumption, noise performance, CMRR and size of neural amplifiers have all improved; and, despite the opposing design options and tradeoffs, many have successfully improved several of these parameters simultaneously. This is in part thanks to innovative design approaches and novel circuit topologies. The objective of this paper is to present a comprehensive review of current designs trends and strategies in neural front-end amplifier circuitry. In the end we glimpse into a comparison of multi-channel systems with a compilation of significant implementations to date.

2. Physiology and Action Potentials, a Brief Review

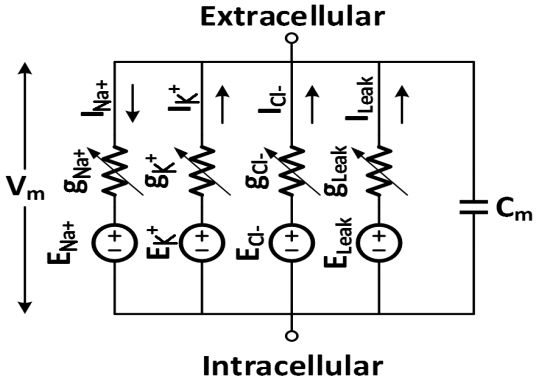
Action potentials are the basic signal waveform mediating information transfer in neural cells. These action potentials occur because the neural cell membrane reverts its polarization or depolarizes. The occurrence of this event can be understood by the movement of ions across the cell membrane. While at rest, several mechanisms, active and passive, promote the transport of potassium K^+ into the cell; while sodium Na^+ ions are transferred to the exterior. By active and passive, it is implied that they either consume or not the energy storage molecule ATP to mediate their action. Despite the fact that K^+ and Na^+ ions are positively charged; the inside of the cell is more negative than positive. The main cathions involved possess different leakage properties across the cell membrane and other elements, such as negatively charged proteins impose a negatively charged resting potential. Thus, the membrane potential is non-zero and in mammalian nervous systems, the outside of the cell is more positive than the interior, which at rests is approximately around −70 mV. When ionic channels become activated either electrically, biochemically or though other mechanisms, the depolarization that occurs is generally the result of voltage sensitive Na^+ sodium channels opening first. The passage of sodium causes an influx of positive charges into the cell and thus raising the potential there rapidly. The resting potential is restored only when, a few moments later the K^+ channels open up sending potassium ions across the cell membrane and into the external surrounding fluid to re-balance things out. This ionic transit occurs sequentially because the voltage dependent channels for potassium open more slowly than their sodium counterparts. This sequence of events transpires in a timeframe in the order of the millisecond. A bio-molecular structure, the Na^+/K^+ ATPase pump then restores the resting equilibrium; this molecular ion pump is powered by ATP, the main energy molecule in animal cells [2]. The ion transport model can be understood physically with the electrical circuit model displayed below in Figure 1. In this figure, ionic leakage and active transport can be seen as a set of battery cells in series with variable resistors. The membrane's lipid bilayer can be correctly predicted to act as a capacitor.

The resting potential that ensues is the result of ionic gradients across the cell membrane and can be computed by derivation from the Nernst equation. The famous result is known as the constant field equation first coined by Goldman in 1943. The take home message from an engineering perspective is that nerve signals mainly travel as binary electrical pulses of roughly 0.1 V in amplitude in the 1-ms range and signal amplitude is pulse code modulated. This last point means that intensity is translated as a proportional increase in firing frequency. The resting membrane potential in real cells is estimated as follow:

$$V_m = \frac{RT}{F} ln\left(\frac{p_K[K^+]_o + p_{Na}[Na^+]_o + p_{Cl}[Cl^-]_i}{p_K[K^+]_i + p_{Na}[Na^+]_i + p_{Cl}[Cl^-]_o}\right) \quad (1)$$

in which K^+, Na^+, and Cl^- are the major contributors to the membrane potential. Note that the unit of V_m is the Volt. However, for practical reasons the membrane potential is typically reported in millivolts (mV). If the channels for a given ion (Na^+, K^+, or Cl^-) are closed, then the corresponding relative permeability values can be set to zero. For example, if all Na^+ channels are closed, $p_{Na} = 0$. R is the universal gas constant (8.314 $J \cdot K^{-1} \cdot mol^{-1}$). T is the temperature in Kelvin (K = °C + 273.15). F is the Faraday's constant (96485 $C \cdot mol^{-1}$). p_K is the membrane permeability for K^+. Normally, permeability values are reported as relative permeabilities with p_K having the relative reference value of one (because in most cells at rest p_K is larger than p_{Na} and p_{Cl}). For a typical neuron at rest, $p_K:p_{Na}:p_{Cl} = 1:0.05:0.45$. Because permeability is reported in relative terms, permeability values are unitless. p_{Na} is the relative membrane permeability for Na^+. p_{Cl} is the relative membrane permeability for Cl^-. $[K^+]_o$, $[Na^+]_o$ and $[Cl^-]_o$ are the concentrations of K^+, Na^+ and Cl^- on the outside of the cell or extracellular fluid; while $[K^+]_i$, $[Na^+]_i$, $[Cl^+]_i$ are the same ionic concentrations but in the intracellular fluid. During depolarization permeabilities and concentrations are dynamically modulated resulting in the observed waveforms.

Figure 1. The electrical circuit model of the ion transport model.



3. Neural Amplifiers Specifications

To get a sneak peak at these action potentials, an amplifying mechanism is required. A neural amplifier must filter neural waveforms to remove DC offsets and augment the resulting signal's amplitude. To provide high signal quality this amplifier must generate sufficient gain, filter appropriate bandwidth, possess high signal-to-noise ratio (SNR) with excellent linearity, and have high common mode and power supply rejection ratios (CMRR and PSRR). The background noise present at the electrode tissue interface is usually in the range of about 10 μV_{rms} or less. This background noise sets the stage for

practical neural signal recording. The majority of neural amplifiers that successfully extract *in vivo* action potentials have an input referred noise value below 3–7 μV_{rms} [1,3,4]. Without this controlled noise level, the signal is drowned in a sea of noise. Locally, at the neural cell membrane level, the action potential is in the 100-mV range; but at a relatively short distance away from the cell surface, this potential falls away rapidly. This is why a gain in the 40-dB range is the least amount one can get away with [4]. Action potentials can be argued to have useful frequency content between 100 Hz to about 8 kHz and signal amplitude that can go into single digit microvolt range [1]. It is evident from stimulation studies that several factors are significant; signal characteristics owe some dependency on physiological factors but are also modulated by electrode geometry [5], target neural tissue composition [2] and electrode impedance [6–8]. The presence of external noise as well as internal noise sources, common mode and power supply noise must also be kept in check. Examples of external noise sources are as the electrical activity from muscle contractions, which mostly affects nerve signal recordings and intensified brain activity which can modulate low-frequency baseline potential levels; environmental noise from radio, cellular and electrical equipment in general can also affect performance. In standard MOSFETs, which are prevailing in modern microelectronics, internal noise sources are mainly thermal noise and flicker noise resulting from intrinsic semiconductor properties. Thermal noise can be controlled by modulating transconductance or the W/L ratio. Flicker noise on the other hand, can mainly be improved by increasing gate capacitance and the easiest way to do that is to increase the area of the input pair transistors. In so doing, however, one must use large input transistors. This yet again pushes the design into weak inversion regions [9]. Fortuitously, the weak inversion point is also the optimal current efficiency area of the device. Maintaining low power consumption and low noise thus dictates common design trends. Finally, it should be mentioned that for practical purposes, one must keep chip size within reasonable bounds. Achieving all those specifications simultaneously is a tall order and a challenge that was recognized early on by experimenters and engineers alike.

When it comes to competing engineering options, difficulty arises when trying to compare the performance of different amplifier topologies, architectures and design tradeoffs. One figure of merit that has endured the test of time is the Noise Efficiency Factor (NEF) [10], despite limitations of this comparison metric, and perhaps in lieu of a better alternative, it is still widely used today. It will be used for comparison in later sections.

$$NEF = V_{rms,in}\sqrt{\frac{2 \cdot I_{total}}{4\,\pi\, kT \cdot BW}} \tag{2}$$

4. System Level Specifications

The previous section sets the stage in terms of performance features for a neural amplifier. However, there is a design gap between the single neural amplifier and requirements for a practical system. Indeed additional design constraints are befitting; for starters, if one wishes to observe even a small parcel of living brain function, multi-electrode systems are essential. In multi-electrode systems, one amplifier is often needed for each channel. Four architectures are possible: either a fixed architecture in which one electrode is connected to one amplifier; a semi-static architecture where the number of electrodes is greater than the number of amplifiers; a third architecture where

electrode/amplifier assignment can be configured occasionally to account changes in performance; and finally, a real-time dynamic system in which assignment and topology may be reassigned in real-time.

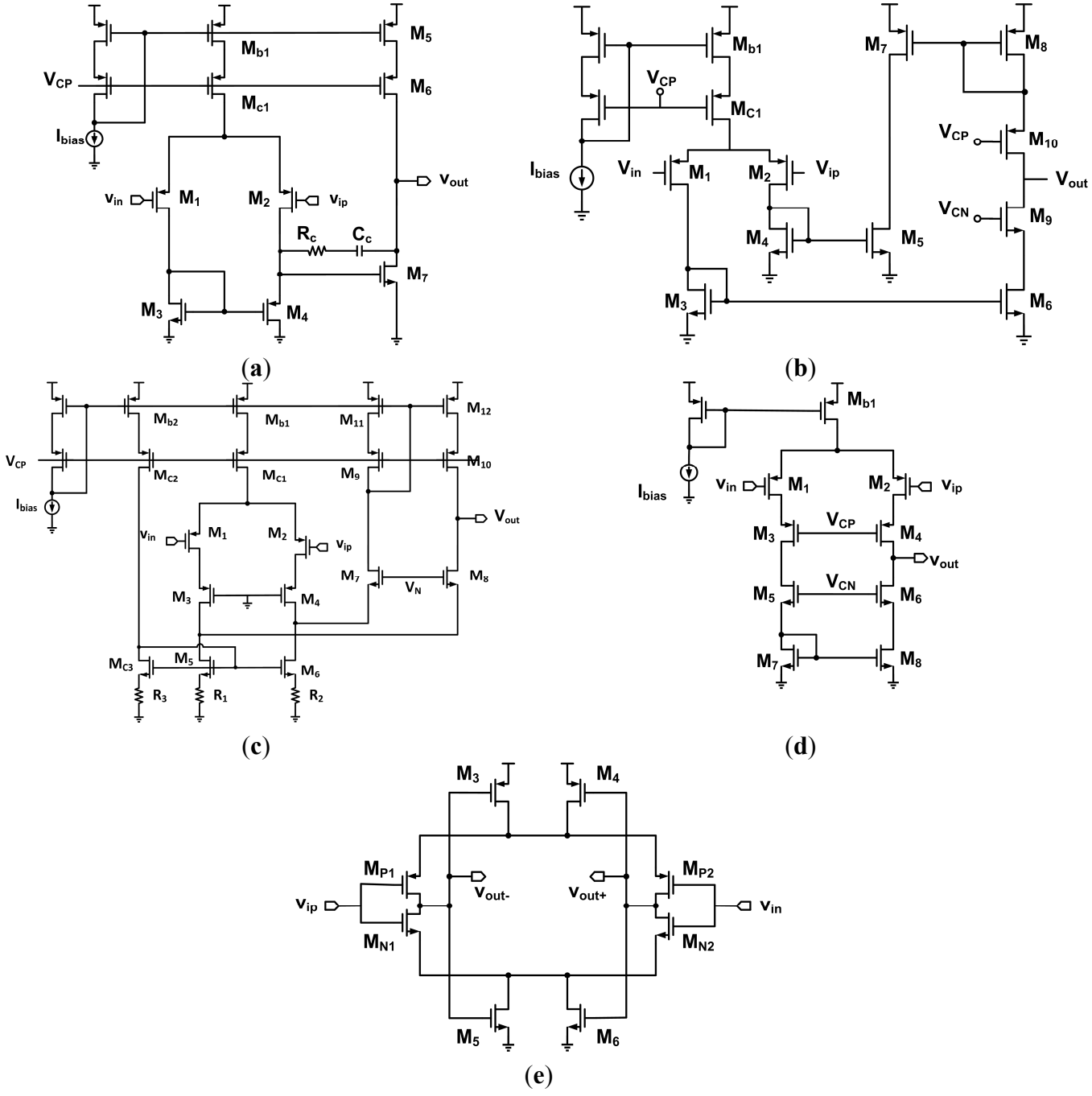
Regardless of architectural choice the requirement for multiple channel observation dictates low power operation, reduced size, and scalability for integration into implantable devices. Yet, the diminutive magnitude of *in vivo* signals requires amplifiers to have substantial gain at low noise and all this demands power. The power conundrum is aggravated by a third limitation; heat dissipation. It is widely accepted that the maximum practical power consumption for a neural implant is in great part set by the maximum heating of its components. Several groups have estimated this limit [11,12], and some normative texts even indirectly dictate it [13]. It has also been shown that a heat flux of 80 mW/cm^2 can be set as a safe limit to uphold [14], in that article, a 4–5 °C elevation was given as an empirical limit based on observed tissue response pathology. In the medical device industry; the acceptable temperature rise limit is usually regulated at ≤2 °C. That limit is typically the maximum tolerated for all commercial implants [13]. Others go even further setting the safety limit at 1 °C or lower [15]. The thermal ceiling imposes a threshold for power dissipation in small device enclosures. Wireless power transmission is also an issue because of inductive heating losses in circuit structures. Furthermore, with inductive charging, the practical charge rate is also limited for commercial medical devices. The reason for this is that electromagnetic field strength exposures are constrained for safety. Within a chip scale device, a practical estimate would typically result in a few mA of available current supply. For a 1.8 V supply for example, this so called limit can be estimated to be 3–5 mA/h or 9 mW/h [11,16]. For useful brain machine interfaces as envisioned by many; a very large number of electrodes will be required. It is expected that systems with thousands of electrodes will emerge within the next two decades [17,18]. Let's suppose as an example such an implantable device with 10 thousand electrodes powered from a state-of-the-art medical grade rechargeable battery with a current capacity of 200 mA/h at 3.7 V. Battery chemistries remain relatively stable and slow changing in medical devices as safety regulations are extremely stringent. If the battery needs to be fully recharged every three to four days; then this leaves us with a power budget about 9 mW, the previously demonstrated limit. With control circuitry, ADC, signal processing, telemetry and heat losses there may be at best half the available power left for neural sensing amplifiers. Theoretically, this would mean a maximum per channel of approximately 450 nW. This is quite a challenge even without considering integration obstacles. Although the 10 thousand electrode count may seem ambitious, similar large count electrode arrays have already been reported and interfaced [19] albeit at a lesser functionality and multiplexed channel conditioning circuitry. Unlike the critical parameters just illustrated for brain machines; this last example was devised for the purpose of cultivated cells in a controlled environment. Regardless of the technology; the goal of these systems is to develop efficient neural interfaces for peering into action potentials mediated brain activity.

5. Circuit Topologies

From the aforementioned specifications, designs can be implemented using various circuit architectures. The most common circuit topologies for implementing low-noise operational transconductance amplifiers (OTAs) are the two stage Op-Amp (Miller OTA, see Figure 2 below) and the current mirror OTA; also there is the folded cascode that allows larger swing margins or reduced supply margins. This last

architecture is becoming increasingly popular as the push for sub 1 V supplies becomes prevalent. Other notable architectures include the telescopic cascode amplifier as reported by [20–22]. Source degenerate active loads lead to significantly diminished currents in the folded branch compared to the differential pair [23]. Finally, one last structure that deserves mention is the differential self-biased OTA as reported by [24]. A full treatment comparing the noise performance of these architectures can be found in [25].

Figure 2. Low-noise OTA. (**a**) Miller OTA; (**b**) current mirror OTA; (**c**) folded cascade; (**d**) telescopic and (**e**) differential self-biased OTAs.



The previously mentioned topologies can be implemented in differential form. In [21], several differential architectures including closed-loop fully differential, telescopic-cascode amplifier;

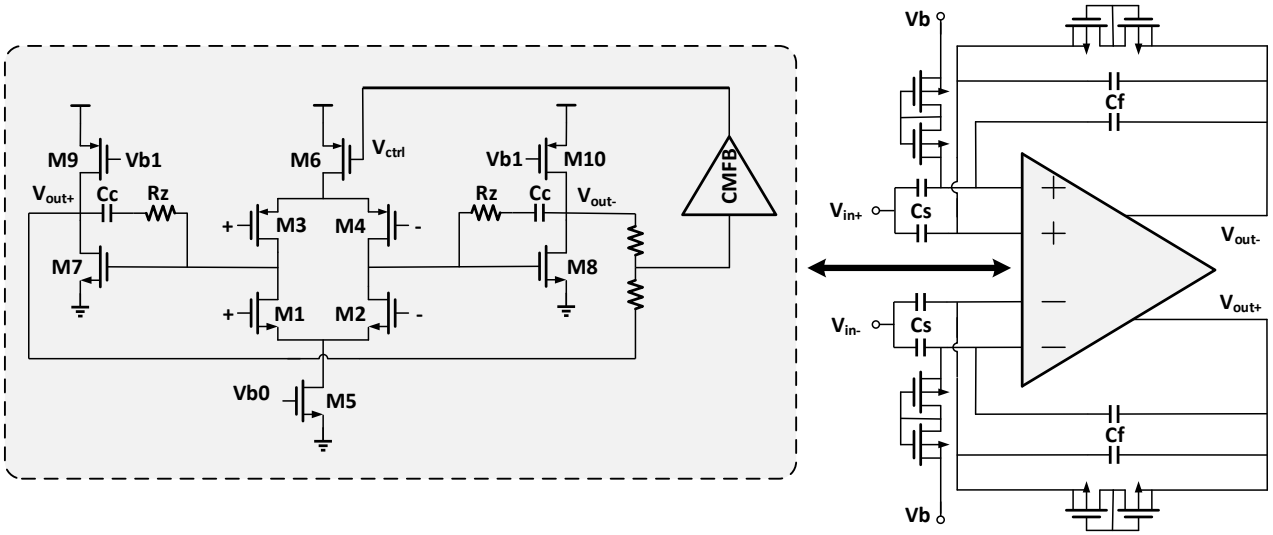
complementary-input open-loop amplifier and complementary-input closed-loop amplifier architectures are presented and tested. The last one was the most successful achieving a gain of 40.5 dB an NEF of 4.5 and a power consumption of 12.5 μW. The chip area was also impressive being below 0.05 mm^2. The table below summarizes the main characteristics achieved by theses comparative designs. One should note here that the second architecture had a debilitating PSRR. Figure 3 also shows the circuit of the most significant implementation.

Table 1. Comparison of the different structures reported in [21].

Architecture	NEF	Power consumption (μw)	Mid band gain (dB)	Area (mm^2)
Telescopic-cascode Closed-loop Amplifier	4.5	12.5	40.5	0.047
Complementary-input Open loop Amplifier	1.9	0.8	36	0.046
Complementary-input Closed-loop Amplifier	2.9	12.1	40	0.072

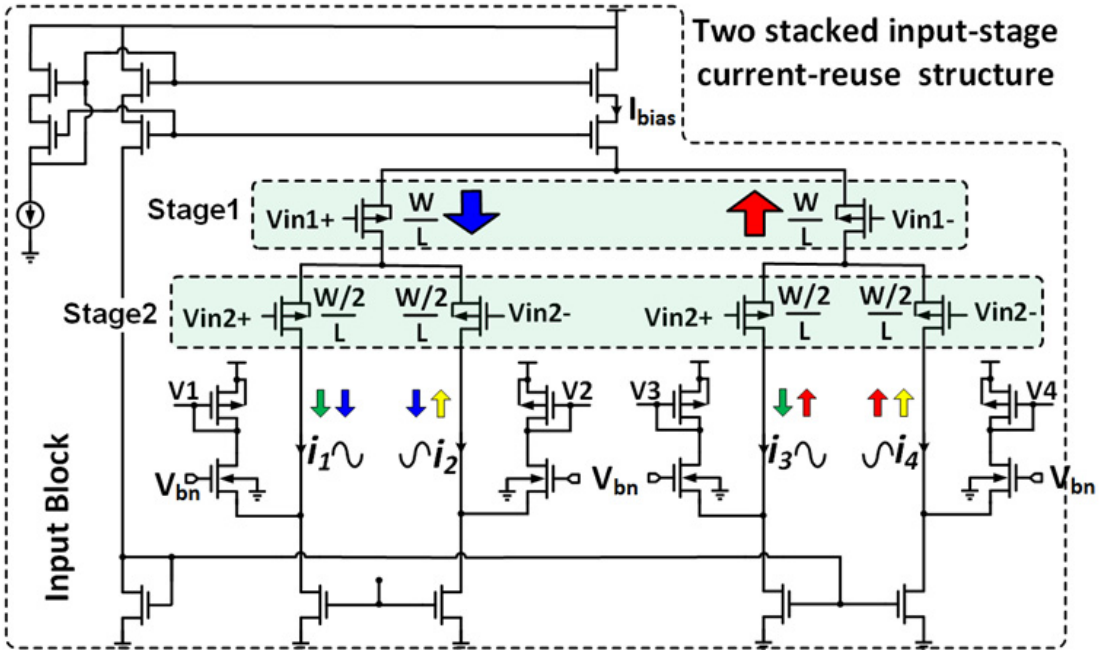
The current feedback instrumentation amplifier possesses key features, such as high impedance and CMRR [26]. However, common problems with this architecture include offset in the mV range. Chopping effectively modulates noise and offset to a pre-selected chopping frequency resulting in a white noise base band. The downside as in most switching architecture is a ripple at the output. Different topologies exist for canceling the ripple [27–32] but they require high chopping frequencies. [33] shows that this can be avoided by using a ripple reduction loop. This type of feedback loop reduces unwanted ripple in the low-frequency chopped output filter by effectively introducing a notch filter in the pass band. Although chopper stabilization results in lower noise; the design is ill suited for large scale integration where power consumption and circuit complexity push the design towards simpler architectures when optimization is key.

Figure 3. The efficient complementary input closed-loop fully differential design as reported by [21].



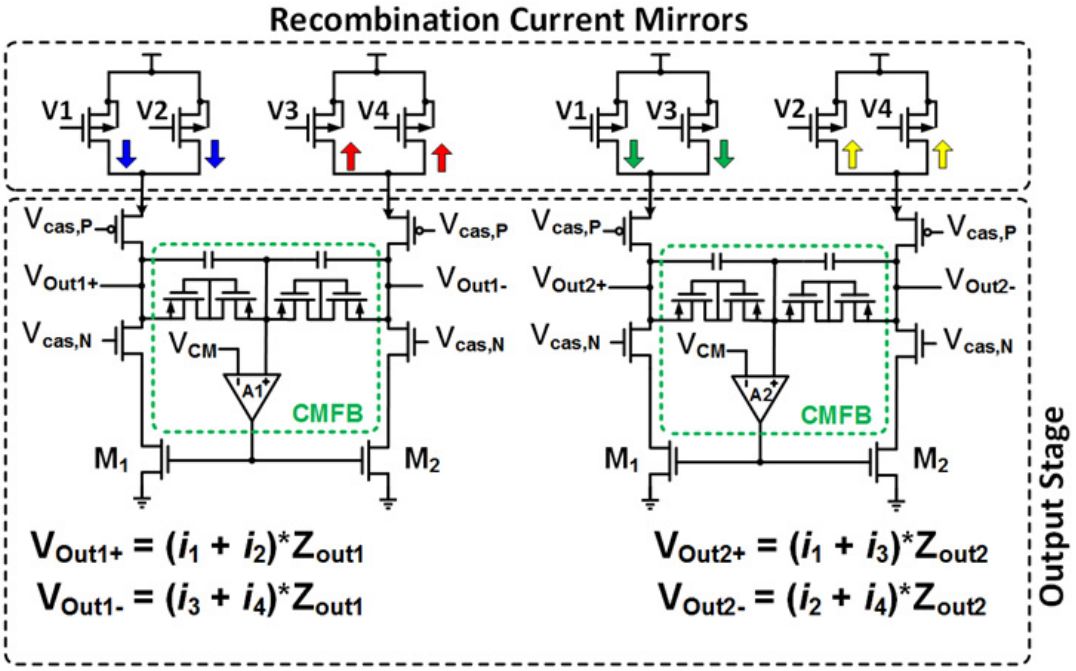
Recently, a NEF of 1.64 was achieved by using the technique of current reuse as described by [34] and [35] (see Figure 4). In this scheme, current is reused between parallel stages to save power consumption and silicon area. Such a scheme consists of multi-staked differential input pairs (Figure 6a) and a current recombination block (Figure 4b), which separates the output currents assigned to the input signals, and an output stage (Figure 4b), which uses recombined currents to generate an output voltage that corresponds to a given input signal. One current source is employed to bias each stack of several differential input stages, in which tail currents are coming from previous stage. The schematic of a two stacked input stage current reuse amplifier is presented in Figure 4a. The second stage (Stage 2 in Figure 4a) is divided into two differential pairs, the input transistors of which are half the size of the input transistors of the first stage. Both stacked input-stages (Stage 1 and Stage 2 in Figure 4) have same g_m. As the total current that flows in second stage is same as the current that flows in the first stage (I_{bias}), the overall g_m in the second stage is equal to the g_m in the first stage. Each output current (small signal currents i_1, i_2, i_3, i_4) is an independent and linear combination of several output currents derived from the corresponding input voltages. The input pairs in the second stacked stage are parallel because they have same inputs (V_{in2+}, V_{in2-}), but they are independent since their tail currents ($I_{bias}/2$) are independent. For example, to generate V_{Out1}, V_{Out1+} and V_{Out1}, the corresponding output currents are re-constructed by summing currents i_1, i_2 and currents i_3, i_4 respectively. V_{Out2} is generated by summing i_1, i_3 currents to construct V_{Out2+}, and currents i_2, i_4 to construct V_{Out2-} (See the schematic of the Output stage in Figure 6b). However, when employed in a multi-channel system, there is some concern that the resulting crosstalk would likely cause issue with increasing channel count. Current reuse as a noise and power reduction method was also discussed in [36].

Figure 4. Two-Stage orthogonal current reuse scheme by [35]. (**a**) The input block consists of two stacked input differential pairs; and (**b**) the output stage includes recombination current mirrors.



(**a**)

Figure 4. *Cont.*



(**b**)

6. System Architectures

6.1. Open-Loop Amplifiers

The above circuit topologies can be used to implement different neural front-end amplifier architectures. Taking a top down approach, a comparison of amplifier topologies is appropriate. The first is the open-loop topology; this structure offers high gains at lowered noise levels it is often implemented adopting some sort of instrumentation *type* layout. Generally open-loop circuits are used for either extremely low power or extremely low noise, but have rarely been reported to achieve both objectives simultaneously. Some good design examples can be found in [37–39] refer to Figure 5 below. It is interesting to note that manually tuned tube versions were used by early electro-physiologists. Open-loop amplifiers are nowadays seldom used in implantable devices. This can be explained by their inherent power and size disadvantages when designing for portable systems. They must often be tuned or screened for performance due to a lack of reproducibility between devices [21]. The problem is mainly due to the gain and CMRR variability that results from imperfect lithographic tolerance between circuit structures. For microelectronics, successful open-loop designs typically use mature, lower resolution, processes as the relative process tolerances are diminished. This approach yields better performance repeatability between channels and devices at the cost of size increase and higher power consumption. Without the lithographic considerations mentioned above, significant discrepancy are observed between simulated and fabricated devices especially for CMRR; the empirical difference in value reaching up to 40 dB from simulations. Modern microelectronic applications are mainly limited to cuff electrode recording where the mechanical layout and nerve implant site require particularly low input noise performance that can be achieved with this architecture. State-of-the-art for tripolar recording systems using this technology is reported in [40]. This amplifier consumes a relatively

elevated 310 μA at 3 V but exhibits a close to theoretical limit of 0.68 μV_{rms}. [41] also describes a micropower fully differential instrumentation amplifier capable of monitoring neurochemical modalities by its sensitivity also reaching a low input referred noise of 2 μV_{rms}. The dynamic range of this current mode amplifier spans an impressive six decades from picoamps to microamps and is thus well suited for scientific investigation as it is also wirelessly interfaced. [39] presented an open-loop sub-microwatt amplifier that made use of pseudo-resistors. Their design achieved 36 dB of gain with a bandwidth of 0.3 to 4.7 kHz and had a respectable input referred noise of 3.5 V_{rms} and NEF of 1.8.

Figure 5. Open-loop schematic reported in [38].

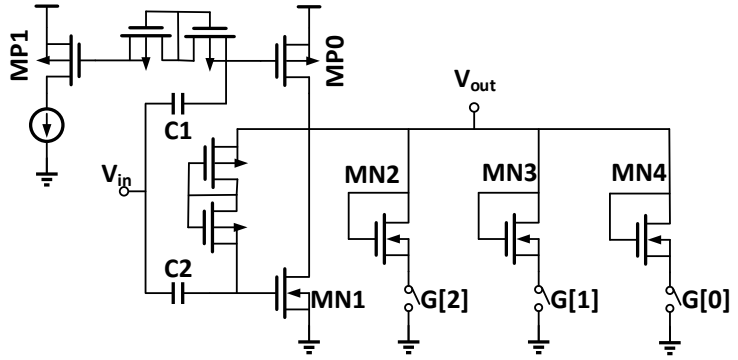
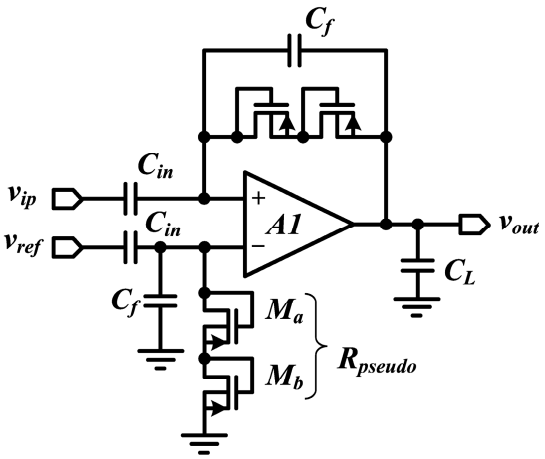


Figure 6. Classic neural amplifier topology with capacitive feedback.



6.2. Capacitive Feedback Topology

In the last decade, engineers have widely borrowed a model that early on, achieved many of the desirable features of neural amplifier. Thus know as capacitive feedback techniques has been the method of choice for many neural amplifier designs, as first reported by [12]. Figure 6 below show the basic topology. It is obvious to see that it is derived from the ubiquitous feedback topology, first introduced by H.S. Black in 1927. Here an impedance element constrains gain by a proportional bandwidth reduction. Increased power consumption is also the cost of "controlling" signal output via the feedback loop and providing a controllable linear response. Typically a small chip scale capacitor is use in conjunction with a very large MOSFET based resistor to create the required low pass response for neural amplifiers in scalable fashion.

The capacitive feedback topology has been optimized for very low-power operation through a dedicated circuit design methodology. The original design achieved a gain of 39.5 dB while posting a power consumption 80 μW and a respectable NEF of four. Modifications and extensive optimization for low-noise resulted through the use of source degenerate current mirrors and high current scaling ratios between input differential pair and folded branch transistors of a folded cascode design, as reported by [23]. The successful results were only possible due to the careful matching of the degenerate mirror. This resulted in a current consumption of 7.56 μW power consumption and an NEF of 2.67 at a gain over 40 dB.

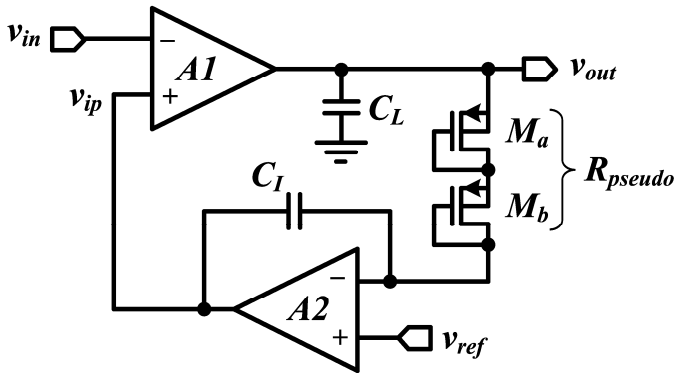
Others have optimized the capacitive feedback topology; [42] reports an ultra-low-power 77-nW bioamplifier, with an NEF of 1.32 and tunable bandwidth, however this circuit also has an input referred noise of 14.3 μV_{rms}. The circuit is a classic capacitive feedback single stage LNA. Similarly, [43] described a 220-nW neural amplifier, also with tunable bandwidth. However, Kim added a buffer, adopting a two-stage architecture with a similarly limiting input noise of 14.5 μV_{rms}. The high input noise and low reported gains (around 30 dB) severely limit the usefulness of these amplifiers. It is important to note here that NEF as a means for comparing amplifiers is practical; but the previous design illustrate its limitation. As seen, a very low NEF can result in bad performance if the input referred noise isn't constrained within the bounds of ambient noise.

More recently [3,11] reported a power consumption of 7.92 μW and an input referred noise of 3.5 μV_{rms}. Also described is an OTA sharing architecture that effectively reduces both chip area and NEF, which was reported to be 3.35. The sharing architecture, in essence, commonly replaces C_f, from Figure 6 above and the MOS pseudo-resistance composed of M_a and M_b in the reference branch input for all channels (see Figure 6) of a classic capacitive feedback design.

6.3. Active Feedback Topology

The third significant topology discussed is the active feedback topology. In this topology a segment of the signal spectrum is filtered and used as a feedback canceling element for suppressing that signal component. This is a very efficient way of extracting low-frequency components from the signal of interest and makes for very stable systems. This method is commonly used in other biomedical engineering applications such as EEG. Figure 7 displays the salient features of this topology. Another advantage of this architecture is the reduction in size that it allows by reducing the capacitor size compared to the capacitive feedback topology [44]. The slowly drifting DC offset is also eliminated in this way. Muller also followed suit on this design by modifying the active feedback with a digital to an analog converter achieving further reductions in size [45] however most of the improvement there shifts analog hardware to a digital platform. Wei's work [46] upholds the arguments of efficiency for this architecture by achieving a 6 μW, an NEF of 3.1, a bandwidth of 8.9 kHz and a mid-band gain of 46 dB occupying a mere 0.022 mm^2 [47] also showed an interesting and novel local feedback at the output technique for reducing DC output. Yet another approach is to design an amplifier in current mode active feedback as demonstrated by [48] and [49]. [48] Achieved a 13 μW power consumption with a 55 dB gain with a 10 kHz bandwidth and a final size of 0.76 mm^2. One interesting feature is that no large value resistor or capacitor needs to be used to achieve a high-frequency cutoff of 0.3 Hz.

Figure 7. Active feedback LNA topology.



A comparative study of a capacitive feedback, a Miller integrator feedback and a capacitive amplifier feedback networks showed that for a given input noise the capacitive feedback topology edged out other designs in terms of NEF, area and power [4]. In this work; area, NEF and power consumption were constrained and plotted against noise in an iterative process until they reached preset gain and frequency specifications. Although the study is interesting, this topic is likely to be mooted in future, as the study was theoretical and other critical design parameters like CMRR and DC rejection performance were not analyzed or observed. Furthermore, it was demonstrated above that NEF can be a pitfall, especially when used as a target specification due to existing power and noise antagonism.

6.4. Pseudo-Resistors

In many of the previous sections we briefly touched upon the use of pseudo-resistors. The large input impedances required for measuring biopotentials as well as the requirement to amplify signals in a range starting from the sub-Hz range requires large resistors. However such resistors are impractical because of the large size that would result. One clever solution to this problem is the use of pseudo-resistors. Such devices provide a means of generating large impedance using biased MOSFET channels. Pseudo-resistor design techniques are extensively discussed in [50] they make use of cross-coupled pseudo-resistors to tune band pass circuits and use fixed versions for the input block. Other design examples can also be found in [51–53]. Pseudo-resistors offer high impedance with limited space use, a desirable feature, additionally they offer tuning possibilities. [54] demonstrated full bandwidth adjustments using pseudo-resistors. Linearity of pseudo-resistors is also an issue. [51,55] addressed the linearity issue by using a cross-coupled circuit with a referenced bias and a sine wave that only turns on one of the pseudo-resistor MOSFETs at a time thereby eliminating voltage variations and the non-linear resistive effects that result from this.

6.5. Adaptive Topology

One emerging method for reduction power consumption in amplifier circuits is to have variable performance features or tunable devices. This allows the modulation overall power duty cycling depending on functional needs. This can take the shape of topology changes and broad range tuning [56,57] uses similar techniques to modulate slew rate and phase margin depending on circuit use. [28] reports an asynchronously adjustable data output rate. [58] describes duty cycling and time division techniques

for improving front-end overall power efficiency; using such techniques a LNA with power consumption of 2 μW was achieved for a 32 KHz bandwidth and an excellent NEF of 1.3. A sophisticated power scheduling scheme is often used in medical devices as exemplified in [59] were a duty cycling is applied to the higher power consumption circuits. In this example sensor conditioning amplifiers and data telemetry have a modulated power scheme. One caveat is that power cycling applied front end circuits require fast settling times such that the sensor signal can be sampled in the shortest time following a power on of the circuit. This reduced settling time requirement usually translates into higher current consumption. A fine balance must therefore be struck between the selected designs tradeoffs, as the combination of benefits does not follow a linear trend when it comes to power economy.

7. Integrated Systems Based on Neural Amplifiers

Merging subsets of the above techniques has resulted in an impressive collection of complete neural acquisition systems. Many such implementations have been reported over the years. In chronological order of reporting for high performance multi-channel systems a list of relevant papers is reported in Table 2 below. Such systems are not so easily compared as they have different aims and inherently different design optimization schemes. Selected systems had to have a bandwidth that permitted neural recording at least up to 4 KHz. For current relevance; our survey was limited to the previous seven years. The main architecture and topology details are listed for reference. Also listed are the NEF, the Gain, the supply voltage and current, the CMRR and the area. Some data were estimated from available information. At the time of writing, the highest numbers of amplifier channels are in the low hundreds as reported by [20] and [60].

8. Discussion

Better designs begin with a better understanding of the problem at hand. This is the reason why we started with an overview of physiological mechanisms involved in neural firing. Three main points are worth noting. At the cell surface nerve signals typically have an amplitude of about 100 mV, their period is of the order of the millisecond and signals are often pulse code modulated. It was then noted that a noise performance in the range of $\leq 5\ \mu V_{rms}$ was a key factor in achieving a quality neural signal. This last requirement comes with the caveat that despite the increased need for power, heat must be limited such that the devices maintains a ΔT within 2 °C. Adding these constraints, power and chip size are limited. For power, we argued that a 450 nW/ch is a singularity point after which practical large-scale systems would become possible.

From these specifications, classic circuit topologies were reviewed including the Miller OTA, the current mirror OTA, the folded cascode, telescopic and self-biased as well as their derivatives. Finally we delved into current feedback, current reuse and chopping architecture as means for improved CMRR, power consumption and noise control.

In the following section our attention is focused on system level architectures, the principal ones described are: open-loop, capacitive feedback, active feedback and adaptive or variable circuits. Open-loop circuits provide the best noise performance but at the cost of higher power consumption and a lack of inter device repeatability. Capacitive feedback is the most popular topology at present because of the good compromises between competing design objectives. The main features for active feedback

are spectral separation and stability. Later, we report on the necessary trend of power scaling, and power management that results in optimized circuit topology.

Finally significant complete systems from the past seven years were listed in a comprehensive table (Table 2) lending to easy comparison of surveyed designs. It can be remarked that increased channel count devices typically are still an order of magnitude too high in power consumption when compared with the requirements we aimed for initially (450 nW) see [20,60–62]. In state-of-the-art devices, the channel count is also an order or two of magnitude below what we would needed for complex neural circuit observation. Typically, noise and gain are marginally within the aforementioned requirements of 40 dB and about 5 μV_{rms} noise; but it's a fine balance between the two [62]. Diminishing size is the metric that has scaled the best in the past years starting with great leaps in 2009 by [60] and [63,64].

With the coming bounty of channels and signals, comes the imperative of signal processing. In that line of thought, the aim is to decipher the underpinnings of neural circuitry and not observe the action potential in a traditional scientific approach. Rather, a pragmatic engineering perspective is to extract only the required firing information before transmission. In that effort, many have labored on the ever increasing need for such spike sorting circuitry. Some reference on the topic have included: [61,63–66].

Although great strides have been made in the past decade, a manufacturable, high-performance, low noise sub-microwatt neural amplifier building block remains an elusive quest. The competing demands for size, power, speed, noise control and integration illustrated still amount to a significant challenge even with today's tools.

9. Conclusions

Much of the past has focused on this microscopic aspect of nerve cells function resulting in a wealth of information regarding action potential mechanisms. We can now understand and accurately simulate cellular interaction quite well. Humans have also observed the macroscopic effect of neural circuitry through behavior analysis and brain physiology as far back as the earlier part of the last century. Current trends provide great optimism that solution for a practical neural front end is within grasp. When beginning the design of a front end amplifier one must ask: Is the design objective to observe details of the action potential waveform or detect the presence of this action potential? Answering this question has significant impacts on design decisions. The former approach has guided neuroscience of the past 70 years while the later seeks to exploit this new information. However to obtain the "in between" part, we need to focus on the significant portions of the signal processing chain and thus the required electronics. We presented not only specifications for achieving efficient neural amplifiers but also the intricate requirements to achieve practical brain interface systems. It would be impractical to design a multi-million transistor digital circuit by modeling every transistor simultaneously. Based on that premise, sensing all signal at high resolution simultaneously is not likely the correct approach to decipher the mechanisms of the brain.

Table 2. Comparison of previously reported multi-channel neural front-end amplifier and systems. Some of the acronyms and contractions used are defined as follows: N/A is used to indicate that information is not available, missing or cannot be computed from published values. CMRR is the "Common Mode Rejection Ratio"; HP stands for "high pass" in the filter sense; LNA stands for "Low Noise Amplifier"; NEF is the "Noise Efficiency Factor" as defined in [10]; OTA stands for "Operational Transconductance Amplifier"; BW stands for "Band Width".

Author	Year of publication	Circuit topology/Architecture	Number of channels	Gain (dB)	NEF	Frequency range (Hz)	Noise (μV_{rms})	Supply voltage (V)	Supply current (µA)	CMRR (dB)	Power consumption per Ch. (Front-end only) or * entire chip (µW)	Area per Ch./Entire chip (mm^2)
Harrison [67]	2007	Two-stage with added g_m-C HP filter/Capacitive feedback	100	60	10.47	300–5 k	5.1	N/A	12.8	N/A	13500 *	N/A/5.9 × 4.7
Chae [61]	2008	Two-stage/Capacitive feedback differential	128	40	8	0.1–20 k	4.9	1.65	40.0	90	6000*	N/A/8.8 × 7.2
Aziz [60]	2009	Two-stage/Capacitive feedback + transconductance LNA	256	48–68	4.6	0.01–5 k	7	3	5.0	N/A	15	0.04/3.5 × 4.5
Gosselin [68]	2009	Active feedback/Multiple stage	16	70	4.9	100–9.2 k	5.4	1.8	4.8	45	8.6	0.05/2.304
Mollezadeh [41]	2009	Two stage/Capacitive feedback	16	39.6	2.9*	0.2–8.2 k	1.94	3.3	8.0	70	26.4	0.107/N/A
Sodagar [64]	2009	Two stage/Capacitive feedback	64	59.5	21.3	24m–9.1 k	8	1.8	41.7	N/A	75	0.072/N/A
Liew [69]	2009	Two-stage/Capacitive feedback	16	45.7–60.5	2.16	0.23–7.8 k	4.43	1	3.8	58	3.77	N/A
Miranda [70]	2010	N/A	32	N/A	N/A	1–4.5 k	5	N/A	N/A	N/A	142000 *	N/A/24000
Perlin [71]	2010	Two-stage/Capacitive feedback	64	60	11.42	<10–9.1 k	4.8	1.5	33.3	N/A	50	0.098/N/A
Shahrokhi [20]	2010	Fully differential/Telescopic	128	33	5.55	10–5 k	6.08	3	2.8	N/A	8.4	0.02/N/A

Table 2. *Cont.*

Author	Year of publication	Circuit topology/Architecture	Number of channels	Gain (dB)	NEF	Frequency range (Hz)	Noise (μV_{rms})	Supply voltage (V)	Supply current (µA)	CMRR (dB)	Power consumption per Ch. (Front-end only) or * entire chip (µW)	Area per Ch./Entire chip (mm^2)
Greenwald [72]	2011	Two-stage with Common mode feedback/Differential	16	40	4.61	N/A–8.2 k	3	3.3	12.5	N/A	41.25	N/A/(3.4 × 2.5)
Aceros [73]	2011	Two stage/Capacitive feedback	32	45.6	115.66	0.1–7.8 k	8.5	3	14.5	N/A	43.8	N/A
Al-Ashmouny [17]	2011	Two stage/Capacitive feedback	16	52.4–79.8	2.9	0.1–17 k	6.76	0.9	3.7	60	3.3	0.07/N/A
Jo-Yu [74]	2011	Two stage/Capacitive feedback	4	51.9	2.79	2.38–12.9 k	4.7	–0.9/+0.9	2.9	N/A	5.22	N/A
Lopez [75]	2011	Folded Cascode OTA multiple stages/Capacitive Feedback	16	40–60	12.12	2.6–6.2 k	2.9	3.3	70.0	>63	231	N/A/25.2
Majidzadeh [11]	2011	Shared reference structure/Capacitive feedback	N/A	39.4	3.35	10–7.2 k	3.5	1.8	4.4	70.1	7.92	0.065/N/A
Rouse [76]	2011	N/A	96	variable	N/A	5 k	N/A	1.7–2.2	2.5	>80	4.25–5.5	N/A
Szuts [77]	2011	N/A	64	65	N/A	10–4.5 k	4	3	N/A	N/A	N/A	N/A
Wattanapanitch [78]	2011	Three-stage—Source degenerate active loads/Capacitive feedback	32	49–66	4.4–5.9	350–11.6 k	5.4–11.2	1.8	3–11.11	62	5.4–20	0.03/N/A
Lo [79]	2011	Two stage/Capacitive feedback	64	47–59	3	0.5–12 k	3.8	1.2	5.0	N/A	6	N/A/(3 × 4)

Table 2. *Cont.*

Author	Year of publication	Circuit topology/Architecture	Number of channels	Gain (dB)	NEF	Frequency range (Hz)	Noise (μV_{rms})	Supply voltage (V)	Supply current (µA)	CMRR (dB)	Power consumption per Ch. (Front-end only) or * entire chip (µW)	Area per Ch./Entire chip (mm^2)
Zoladz [80]	2011	Two stage—folded cascode/Capacitive feedback	64	60	21.28	0.1–12 k	3.7	1.65	15.2	48	25	N/A/(5 × 5)
Yin [81]	2012	Two-stage/Capacitive feedback	100	46	3.3	0.1–7.8 k	2.83	3	20	60	60	N/A/(5.2 × 4.9)
Gao [82]	2012	Fully differential/Capacitive feedback, with switch-cap filtering	96	40–56	6.62	1–10 k	2.2	1.2	56.7	N/A	68	0.26/(5 × 5)
Dong [83]	2013	Two-stage/Capacitive Feedback—fully differential	100	52	1.57	1–10 k	3.2	0.45	162.2	73	73	N/A/25
Johnson [34]	2013	Orthogonal Current-Reuse/ Capacitive feedback	4	40	1.64	19.9 k BW	3.7	1.5	2.6	78	3.9	0.125/N/A
Kmon [56]	2013	Two stage—folded cascode/Capacitive feedback	8	48/60	4.6	0.3–9 k	5	1.8	6.1	48	11	0.065/N/A
Zou [55]	2013	Low Noise OTA/Capacitive feedback multi-stage	100	–	1.9	0.001–5.1 k	4	1.8	6.4	60+	11.6	N/A/28.2
Yin, [84]	2013	Two-stage/Capacitive feedback	100	46	3.3	0.1–7.8 k	2.83	3	20	60	60	N/A/(5.2 × 4.9)
Lopez [62]	2014	Two-stage/Capacitive feedback	55/455	29.5/72	3.08	0.2–6 k	3.2	1.8	3.9	60	7.02	0.19/N/A
Sepehrian [35]	2014	Orthogonal Current-Reuse/ Capacitive feedback	4	45.2–59.7	4.37	10.02 k BW	3.28	1.8	2.27	76	4.1	0.035/N/A

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Author Contributions

In this work, Éric Bharucha conducted an in-depth survey of the literature, and he wrote the initial draft of the paper. He was responsible for comparing the presented circuit topologies and discussing their advantages and disadvantages, and for drawing figures. Hassan Sepehrian and Benoit Gosselin contributed to the writing of the paper, they drew figures and they proofread the paper.

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Jochum, T.; Denison, T.; Wolf, P. Integrated circuit amplifiers for multi-electrode intracortical recording. *J. Neural Eng.* **2009**, *6*, doi:10.1088/1741-2560/6/1/012001.
2. Shepherd, G.M. *Neurobiology*, 2nd ed.; Oxford University Press: New York, NY, USA, 1988.
3. Majidzadeh, V. A Micropower Neural Recording Amplifier with Improved Noise Efficiency Factor. In Proceedings of the European Conference on Circuit Theory and Design, Antalya, Turkey, 23–27 August 2009; pp. 319–322.
4. Ruiz-Amaya, J. A Review of Low-Noise Amplifiers for Neural Applications. In Proceedings of the 2nd Circuits and Systems for Medical and Environmental Applications Workshop (CASME'10), Merida, Mexico, 13–15 December 2010.
5. Krasteva, V.; Papazov, S. Estimation of current density distribution under electrodes for external defibrillation. *BioMed. Eng. OnLine* **2002**, *1*, doi:10.1186/1475-925X-1-7.
6. Ackermann, D.M.; Bhadra, N.; Foldes, E.L.; Wang, X.F.; Kilgore, K.L. Effect of nerve cuff electrode geometry on onset response firing in high-frequency nerve conduction Block. *IEEE Trans. Biomed. Circuits Syst.* **2010**, *18*, 658–665.
7. Ackermann, D.M.; Foldes, E.L.; Bhadra, N.; Kilgore, K.L. Electrode Design for High Frequency Block: Effect of Bipolar Separation on Block Thresholds and the Onset Response. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'09), Minneapolis, MN, USA, 3–6 September 2009; pp. 654–657.
8. Agnew, W.F.; McCreery, D.B. *Neural Prostheses: Fundamental Studies*; Prentice Hall: Englewood Cliffs, NJ, USA, 1990.
9. Baker, R.J. *CMOS: Circuit Design, Layout, and Simulation*; Wiley: Hoboken, NJ, USA, 2011.
10. Steyaert, M.S.J.; Sansen, W.M.C. A micropower low-noise monolithic instrumentation amplifier for medical purposes. *IEEE J. Solid State Circuits* **1987**, *22*, 1163–1168.
11. Majidzadeh, V.; Schmid, A.; Leblebici, Y. Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor. *IEEE Trans. Biomed. Circuits Syst.* **2011**, *5*, 262–271.

12. Harrison, R.R.; Charles, C. A low-power low-noise CMOS amplifier for neural recording applications. *IEEE J. Solid Stare Circuits* **2003**, *38*, 958–965.
13. British Standards Institution. *Active Implantable Medical Devices. General Requirements For Safety, Marking and Information to Be Provided by the Manufacturer*; British Adopted European Standard, B. EN45502–1:1998; BSI: London, UK, 1998.
14. Seese, T.M.; Harasaki, H.; Saidel, G.M.; Davies, C.R. Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue to chronic heating. *Lab. Investig.* **1998**, *78*, 1553.
15. IEEE. *IEEE Standard for Safety Levels With Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3 kHz to 300 GHz*; IEEE Std C95.1–2005 (Revision of IEEE Std C95.1–1991); IEEE: Piscataway, NJ, USA, 2006; pp. 1–238.
16. Silay, K.M.; Dehollain, C.; Declercq, M. Numerical Analysis of Temperature Elevation in the Head Due to Power Dissipation in a Cortical Implant. In Proceedings of the 30th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'08), Vancouver, BC, USA, 20–25 August 2008; pp. 951–956.
17. Al-Ashmouny, K.; Sun-Il, C.; Euisik, Y. A 4 mW/Ch Analog Front-End Module with Moderate Inversion and Power-Scalable Sampling Operation for 3-D Neural Microsystems. In Proceedings of the IEEE Biomedical Circuits and Systems Conference (BioCAS'11), San Diego, CA, USA, 10–12 November 2011; pp. 1–4.
18. Olsson, R.H.; Wise, K.D. A three-dimensional neural recording microsystem with implantable data compression circuitry. *IEEE J. Solid State Circuits* **2005**, *40*, 2796–2804.
19. Urs, F. An 11k-Electrode 126-Channel High-Density Microelectrode Electrode to Interact with Electrogenic Cells. In Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'07), San Francisco, CA, USA, 11–15 February 2007; pp. 158–593.
20. Shahrokhi, F.; Abdelhalim, K.; Serletis, D.; Carlen, P.L.; Genov, R. The 128-channel fully differential digital integrated neural recording and stimulation interface. *IEEE Trans. Biomed. Circuits Syst.* **2010**, *4*, 149–161.
21. Zhang, F.; Holleman, J.; Otis, B.P. Design of ultra-low power biopotential amplifiers for biosignal acquisition applications. *IEEE Trans. Biomed. Circuits Syst.* **2012**, *6*, 344–355.
22. Saberhosseini, S.S.; Zabihian, A.; Sodagar, A.M. Low-Noise OTA for Neural Amplifying Applications. In Proceedings of the 8th International Caribbean Conference on Devices, Circuits and Systems (ICCDCS'12), Playa del Carmen, Mexico, 14–17 March 2012; pp. 1–4.
23. Wattanapanitch, W.; Fee, M.; Sarpeshkar, R. An energy-efficient micropower neural recording amplifier. *IEEE Trans. Biomed. Circuits Syst.* **2007**, *1*, 136–147.
24. Chae, M.; Kim, J.; Liu, W. Fully-differential self-biased bio-potential amplifier. *Electron. Lett.* **2008**, *44*, 1390–1391.
25. Gosselin, B. Recent advances in neural recording microsystems. *Sensors* **2011**, *11*, 4572.
26. Qinwen, F.; Huijsing, J.H.; Makinwa, K.A. A 21 nV/ $Hz^{-1/2}$ Chopper-Stabilized Multipath Current-Feedback Instrumentation Amplifier with 2 mV Offset. In Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'10), San Francisco, CA, USA, 7–11 February 2010; pp. 80–81.

27. Wu, R.; Makinwa, K.A.A.; Huijsing, J.H. A chopper current-feedback instrumentation amplifier with a 1 mHz 1/f noise corner and an AC-coupled ripple reduction loop. *IEEE J. Solid State Circuits* **2009**, *44*, 3232–3243.
28. Wei, T.; Chenxi, H.; Dongsoo, K.; Martini, B.; Culurciello, E. 4-Channel Asynchronous Bio-Potential Recording System. In Proceedings of the 2010 IEEE International Symposium on Circuits and Systems (ISCAS), Paris, France, 30 May–2 June 2010; pp. 953–956.
29. Wu, R.; Huijsing, J.H.; Makinwa, K.A.A. A current-feedback instrumentation amplifier with a gain error reduction loop and 0.06% untrimmed gain error. *IEEE J. Solid State Circuits* **2011**, *46*, 2794–2806.
30. Belloni, M.; Bonizzoni, E.; Fornasari, A.; Maloberti, F. A Micropower chopper-CDS operational amplifier. *IEEE J. Solid Stare Circuits* **2010**, *45*, 2521–2529.
31. Kusuda, Y. A 5.9 nV/Hz$^{-1/2}$ Chopper Operational Amplifier with 0.78 mV Maximum Offset and 28.3 nV/°C Offset Drift. In Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'11), San Francisco, CA, USA, 20–24 February 2011; pp. 242–244.
32. Burt, R.; Zhang, J. A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path. *IEEE J. Solid Stare Circuits* **2006**, *41*, 2729–2736.
33. Qinwen, F.; Huijsing, J.; Makinwa, K. A Capacitively Coupled Chopper Instrumentation Amplifier with a +/−30 V Common-Mode Range, 160 dB CMRR and 5 mV Offset. In Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'12), San Francisco, CA, USA, 19–23 February 2012; pp. 374–376.
34. Johnson, B.; Molnar, A. An orthogonal current-reuse amplifier for multi-channel sensing. *IEEE J. Solid Stare Circuits* **2013**, *48*, 1487–1496.
35. Sepehrian, H.; Mirbozorgi, A.; Gosselin, B. A Low-Power Current-Reuse Analog Front-End for Multi-Channel Neural Signal Recording. In Proceedings of the 12th IEEE International NEWCAS conference (NEWCAS'14), Trois-Rivieres, Quebec, Canada, 22–25 June 2014.
36. Liu, L.; Zou, X.; Goh, W.L.; Je, M. Comparative Study and Analysis of Noise Reduction Techniques for Front-End Amplifiers. In Proceedings of the 13th International Symposium on Integrated Circuits (ISIC'11), Singapore, Singapore, 12–14 December 2011; pp. 555–558.
37. Baru Fassio, M.D. Implantable Signal Amplifying Circuit for Electroneurographic Recording. U.S. Patent 6996435, 2006.
38. Rieger, R.; Schuettler, M.; Pal, D.; Clarke, C.; Langlois, P.; Taylor, J.; Donaldson, N. Very low-noise ENG amplifier system using CMOS technology. *IEEE Trans. Neural Syst. Rehabil. Eng.* **2006**, *14*, 427–437.
39. Holleman, J.; Otis, B. A Sub-Microwatt Low-Noise Amplifier for Neural Recording. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'07), Lyon, France, 22–26 August 2007; p. 3930.
40. Demosthenous, A.; Pachnis, I.; Jiang, D.; Donaldson, N. An integrated amplifier with passive neutralization of myoelectric interference from neural recording tripoles. *IEEE Sens. J.* **2013**, *13*, 3236–3248.

41. Mollazadeh, M.; Murari, K.; Cauwenberghs, G.; Thakor, N.V. Wireless micropower instrumentation for multimodal acquisition of electrical and chemical neural activity. *IEEE Trans. Biomed. Circuits Syst.* **2009**, *3*, 388–397.
42. Kazerouni, I.A.; Dehrizi, H.G.; Isfahani, S.M.M.; Zhuo, Z.; Baghaei-Nejad, M.; Li-Rong, Z. A 77 nW Bioamplifier with a Tunable Bandwidth for Neural Recording Systems. In Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS'10), Kuala Lumpur, Malaysia, 6–9 December 2010; pp. 36–39.
43. Kim, J.; Chae, M.S.; Liu, W. A 220 nW Neural Amplifier for Multi-Channel Neural Recording Systems. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'09), Taipei, Taiwan, 24–27 May 2009; pp. 1257–1260.
44. Gosselin, B.; Sawan, M.; Chapman, C.A. A low-power integrated bioamplifier with active low-frequency suppression. *IEEE Trans. Biomed. Circuits Syst.* **2007**, *1*, 184–192.
45. Muller, R.; Gambini, S.; Rabaey, J.M. A 0.013 mm(2), 5 mu W, DC-coupled neural signal acquisition IC with 0.5 v supply. *IEEE J. Solid Stare Circuits* **2012**, *47*, 232–243.
46. Wei, Z.; Li, H.; Youguang, Z. A Low-Noise Integrated Bioamplifier with Active DC Offset Suppression. In Proceedings of the IEEE Biomedical Circuits and Systems Conference (BioCAS'09), Beijing, China, 26–28 November 2009; pp. 5–8.
47. Castro, P.; Silveira, F. High CMRR Power Efficient Neural Recording Amplifier Architecture. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'11), Rio de Janeiro, Brazil, 15–18 May 2011; pp. 1700–1703.
48. Chung-Yu, W.; Wei-Ming, C.; Liang-Ting, K. A CMOS power-efficient low-noise current-mode front-end amplifier for neural signal recording. *IEEE Trans. Biomed. Circuits Syst.* **2013**, *7*, 107–114.
49. Ferrari, G.; Gozzini, F.; Molari, A.; Sampietro, M. Transimpedance amplifier for high sensitivity current measurements on nanodevices. *IEEE J. Solid State Circuits* **2009**, *44*, 1609–1616.
50. Rezaee-Dehsorkh, H.; Ravanshad, N.; Lotfi, R.; Mafinezhad, K. A Linear Tunable Amplifier for Implantable Neural Recording Applications. In Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS'11), Seoul, South Korea, 7–10 August 2011; pp. 1–4.
51. Zou, X.D.; Xu, X.Y.; Yao, L.B.; Lian, Y. A 1-V 450-nW fully integrated programmable biomedical sensor interface chip. *IEEE J. Solid Stare Circuits* **2009**, *44*, 1067–1077.
52. Chaturvedi, V.; Amrutur, B. A Low-Noise Low-Power Noise-Adaptive Neural Amplifier in 0.13 um CMOS Technology. In Proceedings of the 24th International Conference on VLSI Design (VLSI Design'11), Chennai, India, 2–7 January 2011; pp. 328–333.
53. Yao, K.-W. Design of A Neural Recording Amplifier with Tunable Pseudo Resistors. In Proceedings of the IEEE International SOC Conference, Taipei, Taiwan, 26–28 September 2011; pp. 376–379.
54. Yin, M.; Ghovanloo, M. A Low-Noise Preamplifier with Adjustable Gain and Bandwidth for Biopotential Recording Applications. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'07), New Orleans, LA, USA, 27–30 May 2007; pp. 321–324.
55. Zou, X.; Liu, L.; Cheong, J.H.; Yao, L.; Li, P.; Cheng, M.-Y.; Goh, W.L.; Rajkumar, R.; Dawe, G.S.; Cheng, K.-W.; *et al*. A 100-channel 1-mW implantable neural recording IC. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2013**, *60*, 2584–2596.

56. Kmon, P.; Grybos, P. Energy efficient low-noise multichannel neural amplifier in submicron CMOS process. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2013**, *60*, 1764–1775.
57. Al-Ashmouny, K.; Sun-Il, C.; Euisik, Y. A 8.6 mW 3-bit Programmable Gain Amplifier for Multiplexed-Input Neural Recording Systems. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'11), Boston, MA, USA, 30 August–3 September 2011; pp. 2945–2948.
58. Gosselin, B. Approaches for the Efficient Extraction and Processing of Neural Signals in Implantable Neural Interfacing Microsystems. In Proceedings of the 33th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'11), Boston, MA, USA, 30 August–3 September 2011; pp. 5855–5859.
59. Park, H.; Kiani, M.; Hyung-Min, L.; Jeonghee, K.; Block, J.; Gosselin, B.; Ghovanloo, M. A wireless magnetoresistive sensing system for an intraoral tongue-computer interface. *IEEE Trans. Biomed. Circuits Syst.* **2012**, *6*, 571–585.
60. Aziz, J.N.Y.; Abdelhalim, K.; Shulyzki, R.; Genov, R.; Bardakjian, B.L.; Derchansky, M.; Serletis, D.; Carlen, P.L. 256-channel neural recording and delta compression microsystem with 3D electrodes. *IEEE J. Solid Stare Circuits* **2009**, *44*, 995–1005.
61. Chae, M.; Liu, W.; Zhi, Y.; Chen, T.; Kim, J.; Sivaprakasam, M.; Yuce, M. A 128-Channel 6 mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Tansmitter. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC'08), San Francisco, CA, USA, 3–7 February 2008; pp. 146–603.
62. Lopez, C.M.; Andrei, A.; Mitra, S.; Welkenhuysen, M.; Eberle, W.; Bartic, C.; Puers, R.; Yazicioglu, R.F.; Gielen, G. An Implantable 455-Active-Electrode 52-Channel CMOS Neural Probe. In Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'13), San Francisco, CA, USA, 17–21 February 2013; pp. 288–289.
63. Gosselin, B.; Sawan, M. A low-power integrated neural interface with digital spike detection and extraction. *Analog Integr. Circuits Signal Process.* **2009**, *64*, 3–11.
64. Sodagar, A.M.; Perlin, G.E.; Ying, Y.; Najafi, K.; Wise, K.D. An implantable 64-channel wireless microsystem for single-unit neural recording. *IEEE J. Solid State Circuits* **2009**, *44*, 2591–2604.
65. Gosselin, B.; Sawan, M. Adaptive Detection of Action Potentials Using Ultra Low-Power CMOS Circuits. In Proceedings of the IEEE Biomedical Circuits and Systems Conference (BioCAS'08), Baltimore, MD, USA, 20–22 November 2008; pp. 209–212.
66. Gosselin, B.; Sawan, M.; Kerherve, E. Linear-phase delay filters for ultra-low-power signal processing in neural recording implants. *IEEE Trans. Biomed. Circuits Syst.* **2010**, *4*, 171–180.
67. Harrison, R.R.; Watkins, P.T.; Kier, R.J.; Lovejoy, R.O.; Black, D.J.; Greger, B.; Solzbacher, F. A low-power integrated circuit for a wireless 100-electrode neural recording system. *IEEE J. Solid State Circuits* **2007**, *42*, 123–133.
68. Gosselin, B.; Ayoub, A.E.; Roy, J.F.; Sawan, M.; Lepore, F.; Chaudhuri, A.; Guitton, D. A mixed-signal multichip neural recording interface with bandwidth reduction. *IEEE Trans. Biomed. Circuits Syst.* **2009**, *3*, 129–141.
69. Liew, W.-S.; Zou, X.; Yao, L.; Lian, Y. A 1-V 60 mW 16-Channel Interface Chip for Implantable Neural Recording. In Proceedings of the IEEE Custom Integrated Circuits Conference (CICC'09), San Jose, CA, USA, 13–16 September 2009; pp. 507–510.

70. Miranda, H.; Gilja, V.; Chestek, C.A.; Shenoy, K.V.; Meng, T.H. HermesD: A high-rate long-range wireless transmission system for simultaneous multichannel neural recording applications. *IEEE Trans. Biomed. Circuits Syst.* **2010**, *4*, 181–191.
71. Perlin, G.E.; Wise, K.D. An ultra compact integrated front end for wireless neural recording microsystems. *J. Microelectromechanical Syst.* **2010**, *19*, 1409–1421.
72. Greenwald, E.; Mollazadeh, M.; Hu, C.; Tang, W.; Culurciello, E.; Thakor, N. A VLSI neural monitoring system with ultra-wideband telemetry for awake behaving subjects. *IEEE Trans. Biomed. Circuits Syst.* **2011**, *5*, 112–119.
73. Aceros, J.; Ming, Y.; Borton, D.A.; Patterson, W.R.; Nurmikko, A.V. A 32-Channel Fully Implantable Wireless Neurosensor for Simultaneous Recording from Two Cortical Regions. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'11), Boston, MA, USA, 30 August–3 September 2011; pp. 2300–2306.
74. Jo-Yu, W.; Kea-Tiong, T. A Band-Tunable, Multichannel Amplifier for Neural Recording with AP/LFP Separation and Dual-Threshold Adaptive AP Detector. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'11), Boston, MA, USA, 30 August–3 September 2011; pp. 1847–1850.
75. Lopez, C.M.; Braeken, D.; Bartic, C.; Puers, R.; Gielen, G.; Eberle, W. A 16-Channel Low-Noise Programmable System for the Recording of Neural Signals. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'11), Rio de Janeiro, Brazil, 15–18 May 2011; pp. 1451–1454.
76. Rouse, A.G.; Stanslaski, S.R.; Cong, P.; Jensen, R.M.; Afshar, P.; Ullestad, D.; Gupta, R.; Molnar, G.F.; Moran, D.W.; Denison, T.J. A chronic generalized bi-directional brain-machine interface. *J. Neural Eng.* **2011**, *8*, 036018.
77. Szuts, T.A.; Fadeyev, V.; Kachiguine, S.; Sher, A.; Grivich, M.V.; Agrochao, M.; Hottowy, P.; Dabrowski, W.; Lubenov, E.V.; Siapas, A.G.; *et al*. A wireless multi-channel neural amplifier for freely moving animals. *Nat. Neurosci.* **2011**, *14*, 263–269.
78. Wattanapanitch, W.; Sarpeshkar, R. A low-power 32-channel digitally programmable neural recording integrated circuit. *IEEE Trans. Biomed. Circuits Syst.* **2011**, *5*, 592–602.
79. Lo, Y.-K.; Liu, W.; Chen, K.; Tsai, M.-H.; Hsueh, F.-L. A 64-Channel Neuron Recording System. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'11), Boston, MA, USA, 30 August–3 September 2011; pp. 2862–2865.
80. Zoladz, M.; Kmon, P.; Grybos, P.; Szczygiel, R.; Kleczek, R.; Otfinowski, P.; Rauza, J. Design and Measurements of Low Power Multichannel Chip for Recording and Stimulation of Neural Activity. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'12), San Diego, CA, USA, 28 August–1 September 2012; pp. 4470–4474.
81. Ming, Y.; Borton, D.A.; Aceros, J.; Patterson, W.R.; Nurmikko, A.V. A 100-Channel Hermetically Sealed Implantable Device for Wireless Neurosensing Applications. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'12), Seoul, Korea, 20–23 May 2012; pp. 2629–2632.

82. Gao, H.; Walker, R.M.; Nuyujukian, P.; Makinwa, K.A.A.; Shenoy, K.V.; Murmann, B.; Meng, T.H. HermesE: A 96-channel full data rate direct neural interface in 0.13 μm CMOS. *IEEE J. Solid Stare Circuits* **2012**, *47*, 1043–1055.
83. Dong, H.; Yuanjin, Z.; Rajkumar, R.; Dawe, G.; Minkyu, J. A 0.45 V 100-Channel Neural-Recording IC with Sub-mW/Channel Consumption in 0.18 mm CMOS. In Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'13), San Francisco, CA, USA, 17–21 February 2013; pp. 290–291.
84. Yin, M.; Borton, D.A.; Aceros, J.; Patterson, W.R.; Nurmikko, A.V. A 100-channel hermetically sealed implantable device for chronic wireless neurosensing applications. *IEEE Trans. Biomed. Circuits Syst.* **2013**, *7*, 115–128.