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Article

Extensionless UTBB FDSOI Devices in Enhanced Dynamic Threshold Mode under Low Power Point of View †

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Abstract: This work presents an analysis about the influence of the gate and source/drain underlap length (L_{UL}) on UTBB FDSOI (UltraThin-Body-and-Buried-oxide Fully-Depleted-Silicon-On-Insulator) devices operating in conventional (V_B = 0 V), dynamic threshold (DT, $V_B = V_G$), and the enhanced DT (eDT, $V_B = kV_G$) configurations, focusing on low power applications. It is shown that the underlap devices present a lower off-state current (I_{OFF} at V_G = 0 V), lower subthreshold swing (S), lower gate-induced drain leakage (GIDL), higher transconductance over drain current (gm/I_D) ratio and higher intrinsic voltage gain ($|A_V|$) due to their longer effective channel length in weak inversion and lower lateral electric field, while the eDT mode presents higher on-state current (I_{ON}) with the same I_{OFF}, lower S, higher maximum transconductance (gm_{max}), lower threshold

voltage (V_T), higher gm/I_D ratio and higher |A_V| due to the dynamically reduced threshold voltage and stronger transversal electric field.

Keywords: dynamic threshold; UTBB; underlap; low power applications

1. Introduction

Thanks mainly to its better back gate coupling, ultrathin-body-and-buried-oxide fully-depleted-silicon-on-insulator (UTBB FDSOI) devices present better performance for sub 28 nm technology nodes such as lower short channel effects (SCE) and better threshold voltage control, while keeping the planar structure [1–5]. Also, they can be used at high frequencies with a lower back gate leakage, lower voltage operation and better power efficiency [4,6]. Moreover, by using a Ground Plane (GP) implantation, the threshold voltage can be adjusted without increasing the channel doping, which avoids mobility degradation and random-dopant fluctuations [7]. This region diminishes the depletion thickness underneath the buried oxide layer, reducing the source and drain electric field that reaches the channel through the buried oxide [7–9].

In circuits, a reduced minimum energy consumption has been demonstrated, which occurs at a lower supply voltage [6], when compared to bulk CMOS devices. This minimum energy consumption is a tradeoff between the leakage and the active current, as indicated in Equation (1) and Figure 1 [10].

$$P = \overbrace{C{V_{DD}}^2 f}^{Active} + \overbrace{I_{leak} V_{DD}}^{Leakage} \tag{1}$$

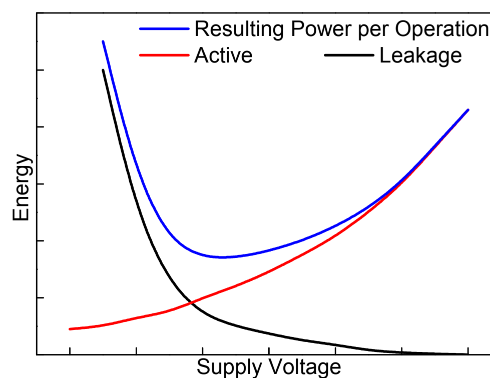

Figure 1. Energy consumption as a function of the supply voltage [10].

With its lower lateral electric field and longer effective channel length, extensionless devices, also known as underlap devices, have demonstrated a better SCE, providing a more scalable structure, better analog performance, and advantages in memory applications [11–15]. Moreover, they have shown a better subthreshold behavior, which in the weak inversion regime is favorable for low power low voltage applications [16].

Originally, the dynamic threshold (DT) concept was explored in partially depleted SOI (PDSOI) devices as a way to avoid the floating body problems. The gate and the body are short-circuited; consequently, the body is never floating [17]. However, the bulk-drain junction can be forward biased

if the gate voltage is higher than 0.7 V, which is a disadvantage for these devices. Recently, with the advent of UTBB devices, a new generation of dynamic threshold voltage configuration (DT2) has been studied [3,18]. In this case, the front gate is connected to the back-gate and the same concept is achieved: during the V_G sweep, the threshold voltage (V_T) is dynamically reduced, as it is a function of the V_{Body} (in PDSOI) or V_B (in UTBB), which is equal to V_G, improving the device performance [17].

Some optimizations have been reported about this approach, regarding the ground plane and the channel length influence in these operation modes [19] or the impact of the silicon film thickness [20]. The effect of the buried oxide thickness on the analog figures of merits has been studied [20–23], as well as the circuit for generating the back gate of the eDT mode for a sleep transistor, taking into account the back gate capacitance influence on the circuit performance. Finally, the application of the dynamic threshold technique in UTBB devices as a power switch has also been discussed [24].

Therefore, the goal of this work is to compare the impact of the underlap length (L_{UL}), including the self-aligned devices (L_{UL} = 0 nm), on UTBB SOI MOSFETs when submitted to a conventional and a dynamic threshold voltage (DT2) configuration, focusing on low power low voltage applications. In order to enhance the back gate influence on V_T, a back gate bias with a multiple value of the front gate voltage ($V_B = k \times V_G$) is also used [3,18], with $k > 1$, which is called the eDT mode in this paper.

2. Device Description

Figure 2 shows the structure of an extensionless UTBB FDSOI device. The devices were built on 300 mm diameter SOI wafers with a 20 nm silicon film (t_{Si}) and 10 nm buried oxide (t_{BOX}). A B-implantation was performed for GP doping. The gate stack is composed by 5 nm SiO_2 and a 5 nm plasma enhanced atomic layer deposition (PEALD) TiN layer capped with 100 nm a-Si. A low energy As-implantation was performed on the standard nMOSFETs (self-aligned with lightly-doped drain—LDD) for the extensions while extensions were left free for the extensionless ones. This was followed by a formation of a first nitride spacer of 15 nm or 20 nm width and of the implanted Si-epitaxial raised Source-Drain (SEG) As-HDD (highly-doped drain) [25]. After the HDD a second nitride spacer is formed followed by silicidation and a standard back-end of line process. The effective channel length (L_{eff}) and width (W) were fixed to 70 nm and 920 nm, respectively. The underlap lengths (L_{UL}) are 0 nm (for the self-aligned devices with LDD), or the first spacer width (15 nm or 20 nm).

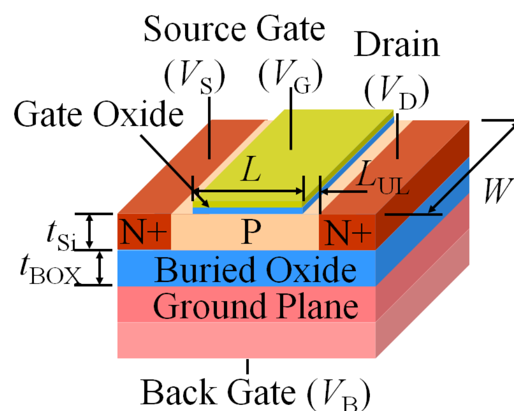

Figure 2. Extensionless UTBB FDSOI (ultrathin-body-and-buried-oxide fully-depleted-silicon-on-insulator) structure considered in this work.

It is important to mention that devices with an underlap of 10 nm have been analyzed in [26]. They presented a worse behavior than the self-aligned devices, due to the shorter effective channel length. These devices have a larger difference between the doping concentration of the channel and the source and drain regions, which increase the lateral diffusion [26]. Therefore, this case will not further be discussed here.

3. Results and Discussion

The I_D-V_G (drain current as a function of front gate voltage) characteristics are presented in Figure 3 for the self-aligned case and for an underlap of 20 nm in the conventional and the eDT (k = 3) modes.

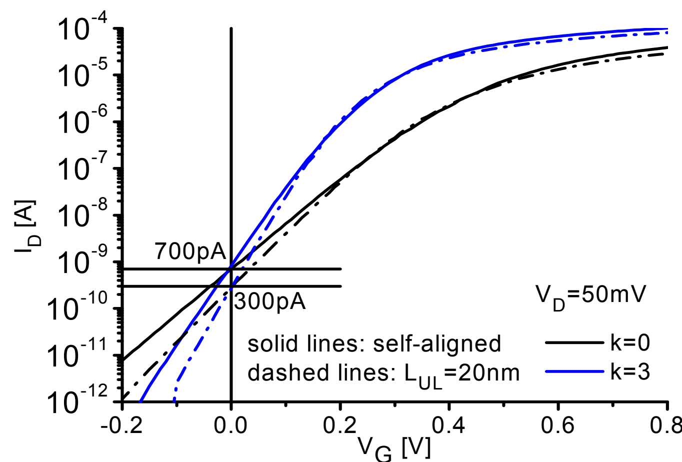

Figure 3. Drain current *versus* front gate voltage for self-aligned and an underlap length of 20nm in conventional and eDT (k = 3) operation. L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

Table 1. I_{ON}/I_{OFF} ratio for self-aligned and an underlap length of 20 nm and for conventional and eDT (k = 3) configurations. I_{OFF} @ V_G = 0V and I_{ON} @ V_{GT} = 200 mV. L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

Self-Aligned, k = 0	Self-Aligned, k = 3	L_{UL} = 20 nm, k = 0	L_{UL} = 20 nm, k = 3
3.08×10^4	6.54×10^4	6.48×10^4	10.52×10^4

One can observe in Figure 3 a lower I_{OFF} (at V_G = 0V), *i.e.*, a lower off-state current, for underlap devices in the conventional mode. A lower off-current is aimed in order to reduce the power dissipation during off-state. This behavior can be due to the longer L_{eff}, and better SCE. This remains in the eDT mode, since the back gate bias applied in both cases is the same. As the devices reach weak inversion, the L_{eff} approaches L_G and the I_D of the underlap device becomes closer to the self-aligned counterpart [15]. In strong inversion, the I_D decreases around 10% due to the higher total resistance of the underlap devices, but I_{OFF} reduces around 57% [14]. Also, when the back gate bias is increased (in DT and eDT conditions) the threshold voltage reduces dynamically and a higher I_{ON} can be achieved. This results in a higher I_{ON}/I_{OFF} ratio for underlap devices in eDT mode (Table 1).

The subthreshold swing (S) and the maximum transconductance were extracted and are presented as a function of the k-values for three underlap lengths in Figures 4 and 5.

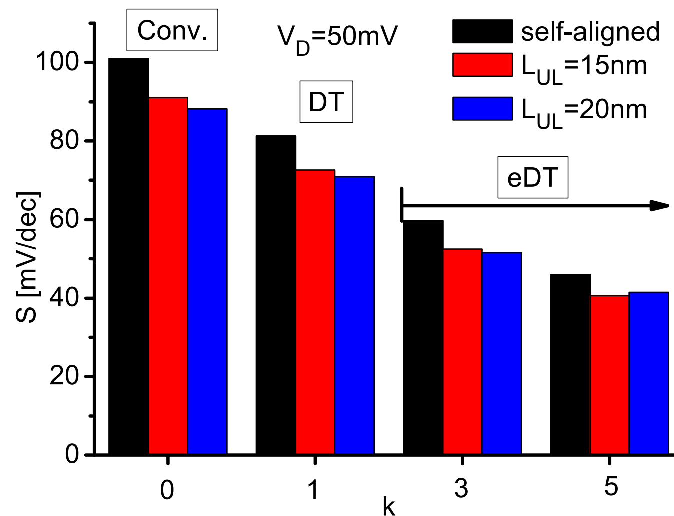

Figure 4. Subthreshold swing for various *k*-values and underlap lengths (based on reference [27]). L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

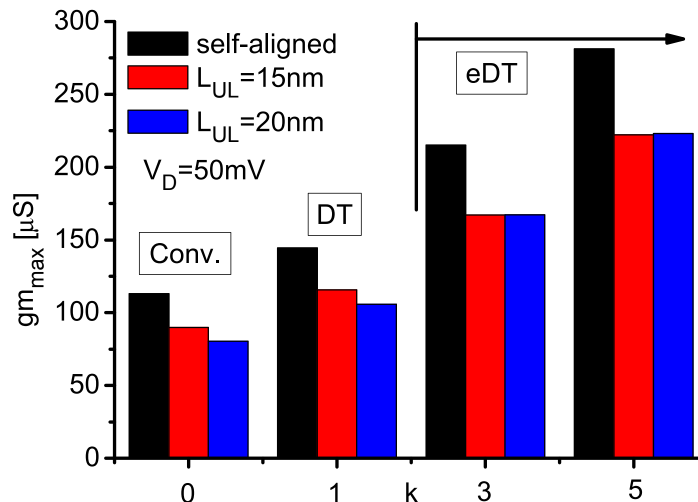

Figure 5. Maximum transconductance for various *k*-values and underlap lengths (based on reference [27]). L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

The higher I_D variation with V_G shown in Figure 1 for underlap devices, and now also with V_B for higher *k* values, leads to a lower subthreshold swing, which is important for low power devices by enabling reduced supply voltages [28]. Moreover, although the underlap devices present a lower maximum transconductance due to the higher total resistance, the eDT mode can overcome this drawback.

Another important aim for low power applications is the reduction of the threshold voltage without raising the off-current, since it means a lower supply voltage added to a constant, or lower, leakage current Equation (1) [10]. Table 2 and Figure 6 show, respectively, the absolute and normalized threshold voltage for the three devices studied and for various *k*-values.

As expected, the threshold voltage decreases for higher *k* values due to the stronger DT effect (Table 2). This effect can also be strengthened by the lower lateral electric field for a higher underlap, which is seen by a lower normalized threshold voltage for DT and eDT in Figure 6.

Table 2. Threshold voltage for various k-values and underlap lengths (based on reference [27]). L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

k	Threshold Voltage [V]		
	Self-Aligned	L_{UL} = 15 nm	L_{UL} = 20 nm
0	0.45	0.48	0.48
1	0.40	0.40	0.37
3	0.29	0.30	0.25
5	0.22	0.24	0.20

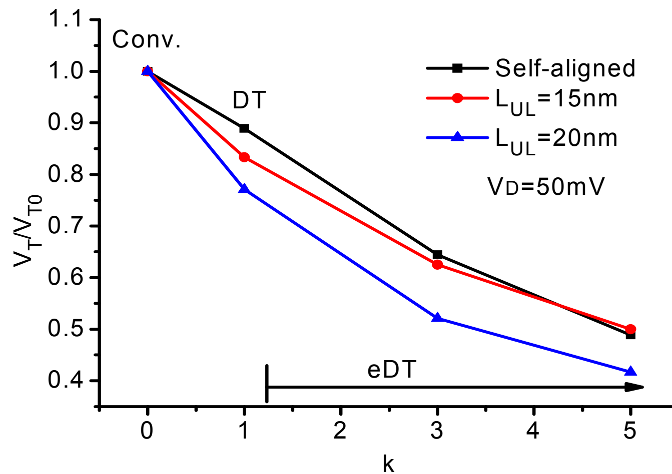

Figure 6. Normalized threshold voltage for various k-values and underlap lengths (based on reference [27]). L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

Concerning the leakage current, there is also the gate-induced-drain-leakage (GIDL), which can be seen in Figure 7 for various k values as a I_D-V_{GT} (drain current *versus* gate overdrive, where $V_{GT} = V_G–V_T$) characteristics (left) and for the three devices studied (right).

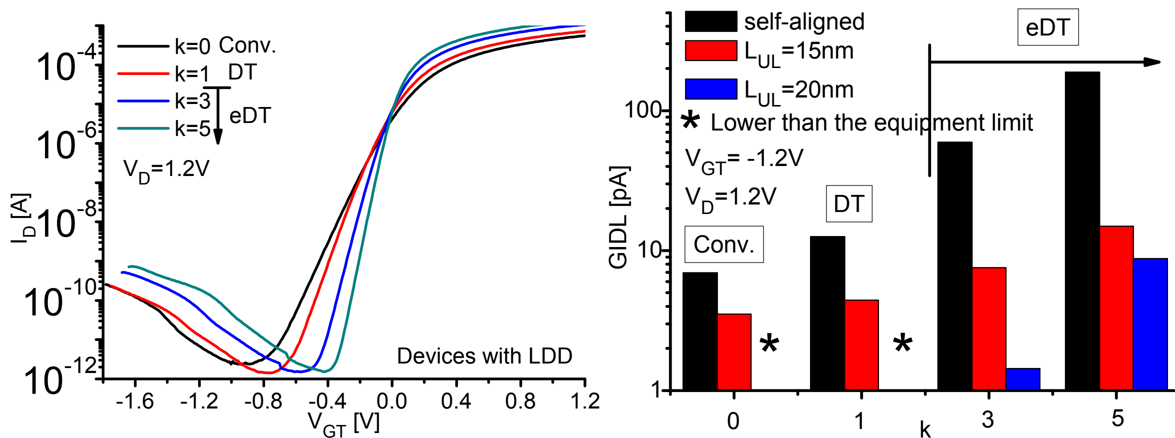

Figure 7. Drain current *versus* overdrive voltage for V_D = 1.2 V for various k-values (**left**) and gate-induced-drain-leakage for different k-factors and underlap lengths (**right**) (based on reference [27]). L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

Concerning the leakage current, as it has already been shown before, I_{OFF} (at V_G = 0V) is lower in underlap devices and is the same in DT and eDT modes. Besides, it is possible to see, in Figure 7,

a higher GIDL in DT and eDT modes, most probably due to a lower potential induced by the lower V_B. For higher *k*-values, the difference between the front and back gate potential increases, enhancing the transversal electric field. This can generate more tunneling charges near the drain, worsening this leakage. However, underlap devices reduce drastically this leakage by a lower lateral electric field [29]. One can notice from the right side of Figure 7, for example, that the 20 nm-underlap for $k = 5$ presents almost the same value than the self-aligned counterpart in the conventional mode.

Figure 8 shows the transistor efficiency, *i.e.*, the transconductance over drain current ratio (gm/I_D) for various k values and for the three underlap lengths in weak inversion, at a normalized $I_D/(W/L)$ of 1 nA.

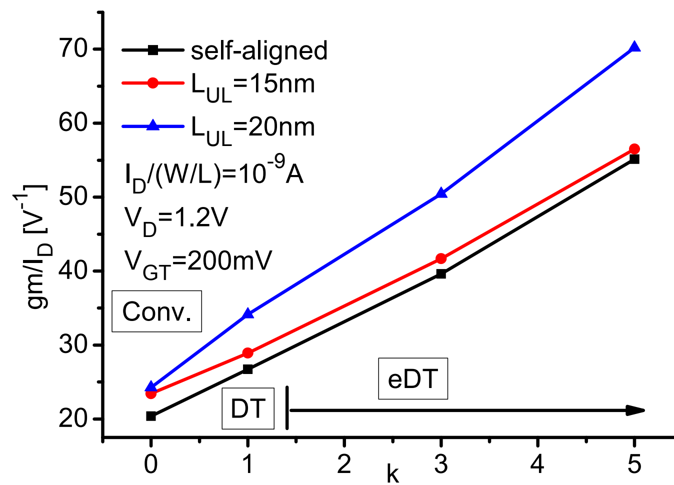

Figure 8. Transconductance over drain current ratio in weak inversion for various *k*-values and underlap lengths at a normalized drain current of 1nA (based on reference [27]). $L_{eff} = 70$ nm, $W_{eff} = 920$ nm, $t_{Si} = 14$ nm, $t_{BOX} = 18$ nm.

A higher efficiency is observed for longer underlap and higher k values, due to the lower subthreshold swing (Figure 4). In other words, one can achieve a higher amplification with the same supply energy in underlap devices in DT and eDT modes.

The intrinsic voltage gain of the studied devices is given for various k values in Figure 9.

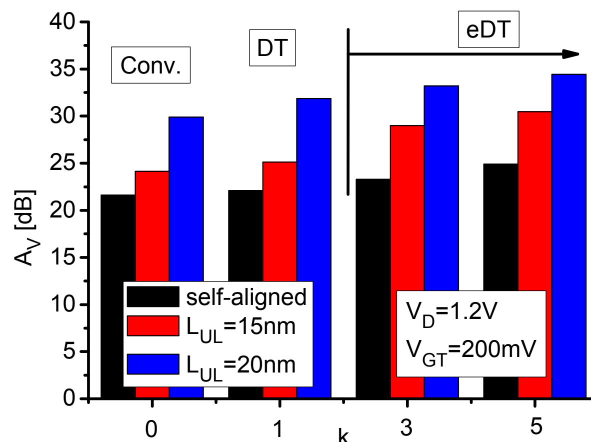

Figure 9. Intrinsic voltage gain for various *k*-values and underlap lengths (based on reference [27]). $L_{eff} = 70$ nm, $W_{eff} = 920$ nm, $t_{Si} = 14$ nm, $t_{BOX} = 18$ nm.

One observes an increased intrinsic voltage gain ($|A_V|$) for longer underlap and higher *k*-values. Since $|A_V| = V_{EA} \times gm/I_D$, Figure 10 shows the Early voltage (V_{EA}) and the gm/I_D in strong inversion for various *k* values and underlap lengths.

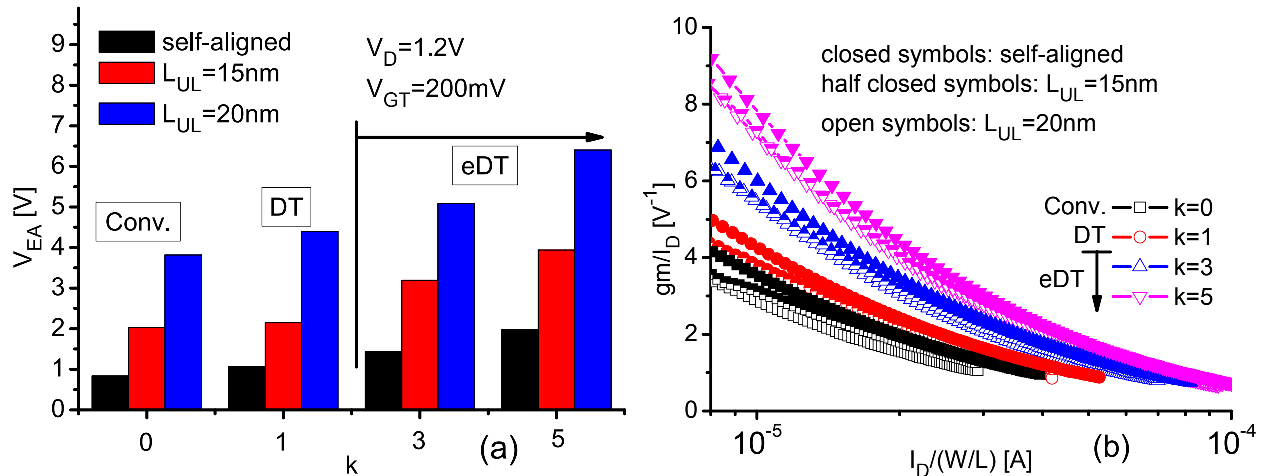

Figure 10. Early voltage (**a**) and transconductance over drain current ratio in strong inversion (**b**) for various k-values and underlap lengths (based on reference [27]). $L_{eff} = 70$ nm, $W_{eff} = 920$ nm, $t_{Si} = 14$ nm, $t_{BOX} = 18$ nm.

Although there is a slight reduction of the gm/I_D in strong inversion for longer underlap (Figure 10b) due to the higher total resistance [12,27], it is negligible when compared to the improvement of V_{EA} (Figure 10a), thanks to the lower lateral electric field [12,29]. Therefore, the main reason for the $|A_V|$ tendency is the substantial reduction of the lateral electric field and, consequently, a higher Early voltage (Figure 10a). Also, a higher influence of the transversal electric field can improve this parameter in DT and eDT operations.

Regarding the *k* values, both, the gm/I_D and V_{EA}, increase for higher k values in strong inversion (Figure 10a,b).

About the gm/I_D in strong inversion, as it is a drawback for longer underlap, one can observe that, for example, the self-aligned transistor in the conventional mode presents almost the same value than the 20 nm-underlap device for $k = 1$. This means that the eDT mode is overcoming the undesired trend.

In order to better evaluate the correlation between the lateral and the transversal electric field, Figure 11 shows the DIBL (Drain Induced Barrier Lowering) for devices with 20 nm and 15 nm underlap in the 3 operation modes considered.

In this figure, the DIBL can represent an estimation of the drain electric field existing in the channel. On the other hand, the *k*-values can be seen as operating on the transversal electric field, since a higher k-value leads to a higher difference between the front and the back interface potential.

One can observe a higher variation for the 20 nm-underlap case than for 15 nm when a higher *k* value is applied. It means that the longer underlap, which corresponds with a lower lateral electric field, is more susceptible to the dynamic threshold effect. In other words, the higher transversal electric field, resulting from a higher k-factor, strongly acts when the lateral electric field is lower.

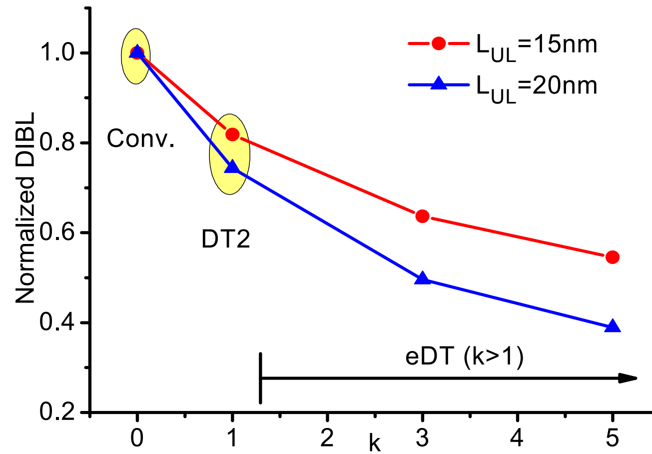

Figure 11. Normalized DIBL as a function of k-value for an underlap of 15 nm and 20 nm (based on reference [27]). L_{eff} = 70 nm, W_{eff} = 920 nm, t_{Si} = 14 nm, t_{BOX} = 18 nm.

4. Conclusions

The impact of the underlap length, including the self-aligned LDD device, on the main parameters was analyzed for three operation conditions: the conventional (V_B = 0 V), the standard dynamic threshold (DT, $V_B = V_G$) and the enhanced DT (eDT, $V_B = kV_G$), focusing on low power applications.

For low power low voltage applications, the best results were $S \cong 41$ mV/dec, V_T = 0.2 V, $gm/I_D \approx 70$ V^{-1} (in weak inversion) and $|A_V| \approx 34$ dB for the 20 nm-underlap device, a channel length of 70 nm and in eDT mode.

Although the longer underlap presented a lower ON-current and transconductance due to the higher total resistance, the dynamic threshold reduction compensates these drawbacks. On the other hand, a longer underlap substantially diminishes the GIDL current, which is a negative point of the dynamic threshold and enhanced modes, since it also means a more negative back gate bias. Looking at the OFF-current, the I_{ON}/I_{OFF} ratio, the subthreshold swing, the threshold voltage, the gm/I_D ratio and the intrinsic voltage gain, both features, longer underlap and eDT, mode improve these parameters.

Moreover, longer underlap devices are more susceptible with the increase of the *k*-factor, leading to a further performance improvement. This can be explained by the lower lateral electric field and higher influence of the transversal one, which strengthen the dynamic threshold effect.

Thus, the eDT mode or underlap devices alone present important shortcomings for low power low voltage applications, such as higher GIDL for eDT mode and lower I_{ON} and gm/I_D ratio for underlap devices. However, combined, they compensate the drawback of the other feature. The 20 nm-underlap device in eDT mode with $k = 5$ presented about the same GIDL current than the self-aligned transistor in the conventional mode. And even for $k = 3$, the eDT mode improves the lower I_{ON} and gm/I_D ratio shown by the longer underlap.

Therefore, the 20 nm-underlap device in eDT mode with $k = 5$ presented the best performance for low power low voltage applications, by enabling a low supply voltage together with a low leakage current.

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Author Contributions

Katia Sasaki measured and discussed the results. Marc Aoulaiche, Eddy Simoen and Cor Claeys fabricated the devices. Joao Martino discussed and coordinated the overall research.

Conflicts of Interest

The authors declare no conflict of interest.

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