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Editorial

A Summary of the Special Issue "Emerging Network-on-Chip Architectures for Low Power Embedded Systems"

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The International Technology Roadmap for Semiconductors [1] foresees that the number of processing elements that will be integrated into a system-on-chip will be on the order of thousands by 2020. The network-on-chip (NoC) paradigm—based on a modular packet-switched mechanism—emerged in the last years as the viable solution to address many of the on-chip communication issues, such as power and performance limitations of long interconnects, and integration of a large number of computing/storage cores on a single chip. However, the design of NoC systems involves several challenges, placed at different levels of abstraction, ranging from the optimization of low-level hardware resources (e.g., buffers, antennas, signals, and clock gating) to higher-level issues such as application tasks mapping, packet routing, and simulation tools.

The aim of this Special Issue is to collect some state-of-the-art contributions which reflect the heterogeneity of the expertise involved in the growing field of NoC design and simulation. An architectural-level perspective is given by the survey work [2], which summarizes recent power-saving techniques for efficient NoC designs, with a focus on the memory subsystem and the interconnection components. In particular, this includes techniques for optimizing both dynamic and leakage power consumption of the caches, along with approaches for designing low-power routers by tackling the problem at the buffer and crossbar level.

A different, high-level perspective on performance/power optimization is the one presented in [3], in which the authors address the problem of inefficient usage of resources due to the unpredictable system behavior at runtime. What they propose is a very promising proof of concept of an interactive consistency protocol in order to establish a global state within an NoC, thus allowing a non-local coordination among the different nodes of the network. The authors also show different possible concrete implementations, together with a resume of respective advantages and disadvantages.

The author of [4] focuses on a very specific and low-level aspect of the communication infrastructure of the next generation NoCs; that is, the usage of a wireless medium to enable fast communication (at several Gb/s) of data among processing and storage elements. The concept of wireless network-on-chip (WiNoC) has gained increasing interest in the last years as a solution to the scalability issues of traditional NoC by enabling single-hop communications between distant nodes. The paper proposes a bow-tie antenna which operates at mm-waves and can be implemented on-chip using the top metal layer of a conventional silicon CMOS. The antenna is compared to the state-of-the-art, including the zig-zag antenna topology that is typically used in literature as a reference for WiNoC, showing a potential good trade-off among bandwidth, gain, size, and beamwidth.

The effects on performance and energy from a data reuse methodology combined with parallelization and vectorization in multi- and many-core processors are investigated in [5], where authors also analyze the effects of parallelism at different granularities by combining vectorization with multithreading. Such topics, while not initially originated from the NoC field, have become more relevant in the recent years, since the traditional programming models are becoming inadequate to exploit the massive parallelism offered by the network-on-chip paradigm.

Finally, the utilization of innovative topologies that go beyond the classic 2D mesh is presented in [6]. Alternative interconnect fabrics such as non-homogeneous three-dimensional integrated network-on-chip (3D NoC), together with the already cited hybrid wired-wireless network-on-chip (WiNoC), have recently been proposed as a cost-effective solution for emerging system-on-chip design. Authors, in particular, propose a low-latency adaptive router with a low-complexity single-cycle bypassing mechanism to alleviate the performance degradation due to the slow 2D routers in such hybrid NoCs.

Conflicts of Interest: The author declares no conflict of interest.

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