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A Cyclic Vernier Two-Step TDC for High Input Range Time-of-Flight Sensor Using Startup Time Correction Technique

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Abstract: Herein, we present a low-power cyclic Vernier two-step time-to-digital converter (TDC) that achieves a wide input range with good linearity. Since traditional approaches require a large area or high power to achieve an input range >300 ns, we solve this problem by proposing a simple yet efficient TDC suitable for time-of-flight (TOF) sensors. In previous studies using the cyclic structure, the effect of startup time on the linearity of the TDC is not described. Thus, the achievable linearity has been limited when the TDC is used for applications requiring a high input range. We solve this problem by using a simple yet effective technique to compensate. The proposed technique is realized using (1) digitally-controlled oscillators (DCOs) that have dual frequency control and matched startup time; (2) an alignment detector that performs startup time correction by proper timing control; and (3) a fully symmetric arbiter that precisely detects the instant of edge alignment. To achieve a fine resolution for the cyclic Vernier TDC, we design two closely-matched DCOs with dual frequency control. The alignment detector performs the critical task of cancelling startup time via timing control. The detector is delay-compensated by using a dummy to provide matched loading for the two DCOs. To enhance the detection speed under low power, a current-reuse approach is employed for the arbiter. The TDC is fabricated using a $0.18\ \mu\text{m}$ complementary metal–oxide–semiconductor (CMOS) process in a compact chip area of $0.028\ \text{mm}^2$. Measured results show a dynamic range of 355 ns and a resolution of 377 ps. When the result is applied for TOF sensing, it corresponds to a distance range of 53.2 m and a resolution of 5.65 cm. Over a relatively large input range, good linearity is achieved, which is indicated by a DNL of $0.28\ \text{LSB}_{\text{rms}}$ and an INL of $0.96\ \text{LSB}_{\text{rms}}$. The result corresponds to root mean square (RMS) error distance of 5.42 cm. The result is achieved by consuming a relatively low power of 0.65 mW.

Keywords: time-to-digital converter; time-of-flight; input range; startup time; cyclic; Vernier; digitally controlled oscillator

1. Introduction

A time-to-digital converter (TDC) is widely used to quantize and digitize time interval information and regarded as one of the most important time sensor [1]. The time interval between pulse signals is used for various sensing applications, for example, altitude sensing [2], depth sensing [3], respiration rate sensing [4], biomedical image sensing [5,6], and distance sensing for navigation [7].

In reference [2], a TDC is integrated with the single-photon avalanche diodes (SPAD) to form the pixel of the sensor, which is used for the image sensor in short-range and for altimeters in the long-range applications. For image sensing applications, time-of-flight (TOF) measurements estimate

the shape of an object by measuring the distance between the sensor pixels and the target object [3]. For biomedical sensing applications, the fluorescence lifetime image (FLIM) sensor uses TDCs to extract important information for identifying cell microstructure [5], which is not usually available from intensity image sensing. TDCs also have great utility in positron emission tomography (PET) image sensing [6]. In reference [7], a TDC is integrated into a distance sensing system for providing range information.

Recently, challenging direct time-of-light (dTOF) applications have been reported using the SPAD equipped with high-performance TDCs. In reference [8], a technique to detect objects hidden from view and track them in real time is presented with a TDC having a 45.5 ps temporal resolution. In reference [9], a massively parallel FLIM microscope for live-cell FRET (Förster resonance energy transfer) imaging is presented with 52.5 +/− 0.7 ps resolution. In reference [10], a confocal non-line-of-sight (NLOS) imaging technique is presented to address the challenge of reconstructing the shape of hidden objects from extremely weak and multiply scattered light. Using a TDC having 4 ps resolution, this work achieves a precision up to 15.1 mm in 0.64 m distance. In reference [11], a depth and reflectivity imaging system with a 390 ps resolution single-photon camera is presented, which achieves high photon efficiency by exploiting both the transverse smoothness and longitudinal sparsity of natural scenes. Although these imaging system using dTOF are widely rely on TDCs, the depth imaging can also be realized using a time-gated image sensor, which achieves a relatively high fill-factor of 61% [12]. Imaging hidden objects are crucial in a diverse area of applications such as robot vision, medical diagnostics, remote sensing, and autonomous vehicles.

Thanks to the advantage of high speed and massive integration available with CMOS scaling, a modern sensor with monolithic integrated TDC has become a preferred approach [13,14]. Fast digital switching capability allows extracting fine time resolution and TDCs are realized using deep-submicron CMOS [15,16]. Because the operation of SPAD requires a high voltage, however, the imaging system is not usually realized in deep-submicron standard CMOS process. Another issue for integrated CMOS imaging system is that the SPAD pixel arrays usually suffer from a low fill-factor, which is attributed to the large area engaged with timing electronics. To overcome the drawback, techniques to integrate diffractive microlens arrays are presented for the SPAD fabricated using 0.35 μm high-voltage (HV) CMOS process [17,18]. In reference [19], the SPAD are realized in ultrathin-body silicon-on-insulator (SOI) process, which allows both frontside-illumination (FSI) backside-illumination (BSI) modes. The BSI mode allows imaging with a wide carrier region which is not blocked by metallization, achieving a virtually perfect fill factor.

For those sensing devices using the TDC, the operating principle is based on the TOF technique. Figure 1 shows the basic operation of a TOF sensing device. The sensor emits a signal with a known time reference and measures the reflected signal from an object. When the time difference T_{input} between signal emission (START) and detection (STOP) is measured, the distance d between the device and object is estimated using

$$d = \frac{c \times T_{\text{input}}}{2} \cos(\theta) \quad (1)$$

where c is the speed of the light and θ is the angle between the device and the object. If d is very large compared to the size of the device, θ is almost zero, leading to $d = c \times T_{\text{input}}/2$.

Figure 1. Operation of a time-of-flight (TOF) sensor. TDC: time-to-digital converter; STARTS: signal emission; STOP: detection.

When a TOF sensor or a 3D camera is used to measure the distance or object's surface depth, its range is directly related to the input range of the TDC [7]. Therefore, a high input range is desirable for many such sensing applications. For example, a high input range with fine resolution allows a camera to sense realistic shapes and surface textures of objects. Because long-time measurements are adversely affected by accumulated jitter and mismatch-related nonlinearity, realizing a sensor achieving a large input range is challenging [15]. Various strategies are reported to increase input range while achieving fine resolution, including two-dimensional (2-D) and three-dimensional (3-D) Vernier structure [16,20], cyclic Vernier [21], gated-Vernier oscillator [22], and a time-to-voltage converter (TVC) [23].

The Vernier TDC uses two delay lines to measure sub-gate delay or time delay smaller than the delay allowed by the process technology. Although this approach has the advantage of a simple implementation, the mismatch between the delay elements limits the achievable resolution. An improved approach involves replacing one of the delay lines with a delay latch chain [24]. This approach saves power and area in addition to reducing the mismatch of the conventional structure. However, the Vernier structure has an intrinsic limit for the achievable input range. This is because the range can only be extended by increasing the number of delay elements. To solve this problem, an interpolation technique is proposed [25], which is based on the Nutt method [26]. Another approach to reducing the length of the delay line involves extending the conversion dimension [16,20]. The 3D approach uses a delay line for the coarse step and a 2D Vernier plane for the fine step [20]. This approach achieves a moderate input range of 14 ns by using a relatively large area of 0.21 mm².

Another approach used to extend the performance of the TDC is using a time-to-voltage converter (TVC) followed by a successive approximation register (SAR) analog-to-digital converter (ADC) [23]. This approach converts the time interval into a voltage, and then quantizes the voltage by the ADC. In this approach, the design of a TVC with a high gain (for a full input range of the ADC) and linearity is challenging. Another drawback to this approach is the large area needed for the on-chip capacitors of the SAR ADC.

The limit of the Vernier delay line for high input range can be solved by using a ring structure for time quantization. In this cyclic Vernier architecture, the two delay lines are replaced with two oscillators which have slightly different frequencies [21,22]. The work in [21] synthesizes a cyclic TDC using the standard cell library and achieves 5.5 ps resolution. The systemic mismatch of the oscillator delay, which is generated by automatic place-and-route, is handled by measuring and calibrating the buffer delay. The ring oscillator is, however, rather sensitive to the process-voltage-temperature (PVT) variation. To handle PVT variation, a gated-Vernier oscillator is proposed [22]. By the first-order noise shaping, the effect of PVT variation and layout mismatch in the oscillator is reduced; the achieved input range of 20 ns is not suitable for TOF applications that demand a large input range.

To achieve a large input range, one can simply try to increase the number of bits of the counter. When the number of bits is increased, however, clock cycles integrate more jitter, which compromises

linearity. As such, this approach is suboptimal as it suffers from degraded linearity and requires increased power. Another important design consideration for cyclic TDCs is the startup time, T_{startup} , of an oscillator. The approach using the STOP signal to directly control the counter, which measures the number of oscillation cycles, cannot compensate for the delay caused by T_{startup} , resulting in counting errors. For applications demanding a large input range, the error caused by T_{startup} has a significant impact on linearity [27].

Since traditional approaches [16,20,25], require a large area or high power to achieve a large input range, we solve this problem by using a simple yet efficient TDC suitable for TOF applications. In the previous studies using cyclic structure [21,25,28], the effect of T_{startup} on the linearity of the TDC is not investigated. Thus, the achievable linearity has been limited when the TDC is used for applications requiring an input range >300 ns. We solve this problem by using a technique to remove the T_{startup} error.

To meet the demands of TOF applications which require the input range from sub-nanoseconds to hundreds of nanoseconds [7], herein, we present a low-power cyclic Vernier two-step TDC achieving good linearity over a wide input range. The TDC is realized using (1) digitally-controlled oscillators (DCOs) with dual frequency control and matched T_{startup} ; (2) a new alignment detector performing T_{startup} correction via proper timing control; and (3) a fully symmetric arbiter performing precise detection of the instant of edge alignment. To compensate for the delay caused by T_{startup} , the alignment detector controls the counters with proper timing instead of using the STOP signal. By the proposed technique, the error caused by T_{startup} is effectively removed by measuring T_{input} from the time difference between two closely-matched DCOs. The experimental results show that the proposed T_{startup} correction achieves a good linearity over a relatively wide input range of 355 ns. When the result is applied to TOF range sensor, it corresponds to a detection range of 53.2 m and a resolution of 5.65 cm. Over the input range, good linearity is indicated by a differential nonlinearity (DNL) of 0.28 LSB_{rms} (root mean square of the least significant bit) and an integral nonlinearity (INL) of 0.96 LSB_{rms} . When the INL is used to indicate the discrepancy between the measured and real distance [20], the corresponding error distance is about 5.42 cm.

2. Design

Figure 2 shows a block diagram of the proposed TDC. It consists of two DCOs, a digital controller, a coarse and a fine counter, and an output latch. The fast and slow DCOs generate outputs OSC_S and OSC_F , respectively. The DCOs use dual control for fine frequency tuning, which is achieved by using digital control word $\text{CTL}<3:0>$ and tuning voltage, V_{tune} . The coarse and fine counter clock signals, CN_C and CN_F , increment the count value during coarse and fine steps, respectively. An RSTD signal is used to reset the DCOs while the two counters are reset by the RSTC signal. In the cyclic Vernier structure, the fast DCO catches up with the slow DCO, resulting in edge alignment. The EDGE signal is used to distinguish two kinds (rising/rising and rising/falling) of the edge alignment. Using a 1-bit EDGE signal, 4-bit coarse counters and 8-bit fine counters, the TDC generates a 13-bit output.

Figure 2. Block diagram of the proposed TDC. CN_C and CN_F : coarse and fine counter clock signals; DCOs: digitally-controlled oscillators.

A Startup Time Cancellation

Consider a ring oscillator having an odd number of inverter stages, N_{stg} , as shown in Figure 5a. Ideally, when an enable signal EN is asserted, the oscillator would immediately generate the output CLK_OUT. In practice, each stage of the oscillator must accumulate some delay before producing an output. The propagation delay leads to startup time T_{startup} . Assuming equal charging and discharging currents as shown in Figure 5b, the rise and fall times are approximately equal to T_D as $t_{\text{rise}} = t_{\text{fall}} \cong T_D$, where T_D is the average propagation delay of the inverter.

Assuming that each of the stages has the same characteristics, the cycle time (or period, T_{cycle}) of the oscillator, which is the time it takes for the output to repeat its phase, can be expressed [29] as

$$T_{\text{cycle}} \cong 2N_{\text{stg}}T_D \quad (3)$$

In the ring oscillator, T_{startup} is the signal propagation time after the EN signal is enabled. Neglecting delay in the logic gate, it can be expressed as the sum of delays as

$$T_{\text{startup}} \cong N_{\text{stg}}T_D = T_{\text{cycle}}/2 \quad (4)$$

T_{startup} is affected by various factors such as clock jitter, supply noise, and PVT variation. Nevertheless, Equation (4) shows that T_{startup} is relatively large, on the order of T_{cycle} . For example, the slow DCO in this study runs at 43.1 MHz with $T_S = 23.2$ ns. In this case, $T_{\text{startup}} \cong T_{\text{cycle}}/2$ is 11.6 ns.

Figure 5. (a) Timing waveform of a ring oscillator. (b) Charging and discharging currents in an inverter.

To investigate the effect of T_{startup} on the linearity of the TDC, we consider the waveform as shown in Figure 6. It shows two cases for a relatively large $T_{\text{startup}} T_{\text{cycle}}/2$. Here, we consider the period of coarse step with $T_{\text{cycle}} = T_S$. Figure 6a shows the case when T_{input} is in the range of $k \times T_S < T_{\text{input}} < k \times T_S + T_{\text{startup}}$ ($k = 2$ in this case). When the START signal initializes the counter, the cycle of the OSC_S is counted until the STOP signal disables the counter. In the case shown in Figure 6a, the counter generates an incorrect output of $(k - 1)$ while the correct value is k . This error occurs because T_1 (between the rising edge of STOP and the 3rd cycle of OSC_S) is less than T_{startup} . This error can be explained more generally as follows: after the START signal, the counter *has to wait* an amount of T_{startup} to measure an oscillation cycle. However, when the STOP is activated, the counting is immediately disabled. This error cannot be simply corrected by adding one to the coarse value because there is another case. Figure 6b shows the case of $j \times T_S + T_{\text{startup}} < T_{\text{input}} < (j + 1) \times T_S$ ($j = 1$ in this case). When the oscillation cycle is counted between the START and STOP signals, it generates the correct value of j . This case of correct counting occurs as long as T_{startup} is less than T_1 .

Figure 6. Waveform of two cases of the input time for a large $T_{startup}$. (a) Incorrect counting by the startup time. (b) Correct counting.

Figure 7 shows the effect of $T_{startup}$ on the transfer characteristic of the TDC. The error occurs in the region corresponding to the case of Figure 6a. The result shows that the output is periodically disturbed by the error. In the case when the STOP signal is used directly to stop OSC_F, we note that the TDC does not generate the output when $T_{input} < T_{startup}$. This is because OSC_S is not yet started and the STOP signal has already arrived. Therefore, there are none of any oscillations initiated in the two DCOs. The $T_{startup}$ affects only the coarse step and generates the coarse counting error. Therefore, the influence of $T_{startup}$ can be ignored when T_{input} is small, for example, the error does not occur for the case of $T_{startup} < T_{input} < T_S$ as shown in Figure 7. When T_{input} is small, the TDC skips the coarse step and operates only in the fine step. Although OSC_F is delayed by $T_{startup}$, we note that a similar delay occurs in the OSC_S. In this work, we extract T_{input} from the first incoming edges between OSC_S and OSC_F. Therefore, $T_{startup}$ does not generate an error in the fine step. In the case when T_{input} is in a small range, for example, $2T_S < T_{input} < 2T_S + T_{startup}$ as shown in Figure 6a, the coarse error can be considered as an offset which can be removed by post-processing. When T_{input} is large, however, the error cannot be considered as an offset. Because the range of the T_{input} is unknown prior to the measurement, calibration of this nonlinearity is rather complicated.

Figure 7. Input and output characteristics of the TDC for a large $T_{startup}$.

The above result indicates that the effect of T_{startup} on the TDC's linearity may be mitigated by reducing T_{startup} . By modifying the logic gate where the EN signal is applied, we can indeed reduce T_{startup} ; when the logic gate for the EN signal in Figure 5a is moved to the last stage of the oscillator, it can be shown that T_{startup} is inversely proportional to N_{stg} as $T_{\text{startup}} \cong T_{\text{cycle}}/(2N_{\text{stg}})$ [29]. By increasing N_{stg} , T_{startup} can be reduced; this is achieved with increased power, accumulated jitter, and low speed ($T_{\text{cycle}} \cong 2N_{\text{stg}}T_D$).

Figure 8 shows two cases of waveforms for a relatively small T_{startup} . The result is shown for $T_{\text{startup}} \cong T_S/(2N_{\text{stg}})$ with $N_{\text{stg}} = 5$. Figure 8a shows the case of $k \times T_S < T_{\text{input}} < k \times T_S + T_{\text{startup}}$ ($k = 2$ in this case). Here, the STOP signal is activated before the 2nd cycle of OSC_S is finished and the counted value is $(k - 1)$, which is incorrect. The error is generated because T_2 (the time between STOP and the rising edge of 3rd OSC_S) is smaller than T_{startup} , and OSC_S is delayed by T_{startup} . Figure 8b shows a case in which the STOP signal is activated before the 2nd cycle of OSC_S is finished, which counts the correct value. In this case, T_2 is larger than T_{startup} , and the small T_{startup} time does not affect the counting result. These results are similar to those shown in Figure 7, except for the reduced width of the error region, showing that even when T_{startup} is reduced, incorrect counting still occurs in some cases. Therefore, the output is necessarily disturbed by a constant offset in the transfer characteristic.

Figure 8. Waveform of two cases of the input time for a relatively small T_{startup} . (a) Incorrect counting by the startup time. (b) Correct counting.

The counting error caused by T_{startup} is related to the method used to detect the moment when the coarse step ends. In the actual TDC, the START signal for the coarse step is delayed by an amount of T_{startup} . In the case when the STOP signal is used to disable the coarse step, there is no compensation for the delay caused by T_{startup} . Therefore, the conventional approach of using the STOP signal to end the coarse step can generate the counting error. In summary, this method generates an error because OSC_S is used to *directly* clock the counter.

To achieve good linearity over a wide input range, we propose a startup time correction technique. The proposed technique is based on the idea of using two DCOs with matched T_{startup} . In this system,

T_{input} is equal to the time difference between OSC_S and OSC_F instead of between the START and STOP signals. In more specifically, CN_C is generated from OSC_S . Before OSC_F is activated in the coarse step, the number of OSC_S cycles is counted to generate N_C . When OSC_F is activated in the fine step, it controls the latch to stop generating N_C . In this way, N_C is generated *indirectly* from OSC_S , not from the delayed rising edge of OSC_S . The proposed solution is implemented using the alignment detector as explained in the next section.

B. Alignment Detector and Arbiter

Figure 9a shows the schematic of the alignment detector. It performs two critical tasks: (1) detecting the edge alignment of two DCOs and (2) controlling the counter timing for startup time correction (explained above). When the conversion is started, an active-low reset signal RST changes the charging node 'C' to high and enables the logic gate that follows. In the coarse step, OSC_S is enabled. The arbiter receives the OSC_S signal and its output A_S goes through another inverter to generate CN_C . The CN_C signal is a delayed and gated version of OSC_S , which is used to increment the coarse counter. It is generated through the arbiter to immediately stop the counting when the edge alignment occurs. During the coarse step, OSC_F is inactive and the latch control signal LAT is low at this time. Thanks to the cross-coupled inverters used for the latch, the node 'C' is kept at a high level during the coarse step. The reason why we use the latch is to make sure that the NAND logic used for gating the CN_C is enabled even node 'C' is being discharged by leakage current.

The coarse step is finished when OSC_F is activated. It generates a short pulse for the LAT signal, which pulls down the node 'C' and disables the logic gate for CN_C . And the TDC enters the fine step. In the fine step, OSC_F catches OSC_S after some number of cycles. The alignment moment is detected by an arbiter followed by a D flip-flop (D-F/F), which generates the DETECT signal. The latch is added because the output of the arbiter is level sensitive.

Figure 9. (a) Schematic of the proposed alignment detector, (b) alternative approach to generate CN_C .

We note that the activation and de-activation of CN_C are performed by the two DCOs having closely matched $T_{startup}$; the time between START and OSC_S is closely matched to the one between STOP and OSC_F . By using OSC_F to control CN_C , the delay of $T_{startup}$ does not cause an error in the coarse counter. In comparison, the conventional approach using the STOP signal for counter control does not consider $T_{startup}$ and can result in incorrect counting as shown in Figure 7.

We may consider using OSC_S as the coarse counting clock and utilizing the first rising edge of OSC_F to directly stop the coarse counting. This approach looks intuitive, however, it can create unbalanced load in the OSC_S and OSC_F paths. In addition, the implementation of the counter control signal for CN_C requires a *pause* function instead of a simple reset. When OSC_F arrives, it should stop the coarse counter to end the coarse step. At this time, we note that its counted value should be preserved for TDC's output. This is because OSC_S still operates during the fine step until coincidence with OSC_F is detected. One example circuit realizing the pause function is shown in Figure 9b. This approach has the advantage of simple logic and generates a small delay in stopping the CN_C signal. Because of the setup time of the D-F/E, however, this approach may generate an unexpected counting error. This is in particular problematic when T_{input} is close to an integer multiple of OSC_S period. Another issue of using the simple logic is that the information available from the output A_S of the arbiter is wasted; it can be used to stop the coarse counting without causing additional loading to the DCOs.

To achieve the proposed startup time correction, a good balance between the two outputs of the DCO is necessary. The arbiter itself has an inherently symmetric structure (see Figure 10). Therefore, we consider balanced loading at the two inputs of the arbiter. If the loading at the two ports is different, there can be a mismatch in the transient time of the two DCOs, which increases the probability of incorrectly detecting alignment. To achieve balanced loading, we insert a dummy at the output of OSC_S . The size of the dummy is determined by performing extensive Monte-Carlo simulations that consider both local and global process variation. In this way, we are able to mitigate the load mismatch at the two outputs of OSC_S and OSC_F . The upper limit to the estimated value of $T_{startup}$ is $T_{cycle}/2$ as indicated by Equation (4). In the case when the startup times of OSC_S , ($T_{startup,S}$) and OSC_F ($T_{startup,F}$) are not equal, the difference can be approximated to half the resolution τ as

$$T_{startup,S} - T_{startup,F} \cong (T_S - T_F)/2 = \tau/2 \quad (5)$$

Fortunately, the difference is an offset error with a mean value of $\tau/2$, which can be easily removed by post-processing. We consider this post-processing because there can exist the mismatch caused by environmental noise and random jitter even when $T_{startup}$ has been matched well in the simulated conditions.

Figure 10. Schematic of the arbiter.

Figure 10 shows the schematic of the arbiter. The arbiter is adapted from the previous work [6], and modified to reuse current for increasing the transconductance and speed. Similar to the arbiter [6], which keeps the output in good balance during the reset phase, the output of the proposed arbiter is also reset when both inputs are high. Circuit simulations show that the average current of the proposed arbiter is 16 μA at a supply voltage $V_{DD} = 1.8$ V. In comparison, the current is 53 μA for the

arbitrator [6], in which the high current is attributed to leakage current occurring when the two inputs are high and the outputs are in the middle. The proposed arbitrator achieves a delay time from input to output of about 100 ps which is two times smaller than that of the previous work [6]. Compared with the conventional D-F/F and dynamic (true single-phase clocking-based) D-F/F, the proposed arbitrator achieves better load balance. This is because the arbitrator maintains a symmetric current steering path between two inputs while the D-F/F has different loads for the clock and data paths.

Although the arbitrator has a symmetric structure, an offset time, t_{offset} , occurs due to the mismatch of device parameters, routing parasitics, and unbalanced loading. When the alignment of two DCOs occurs, the edge of OSC_F leads/lags that of OSC_S by the time difference δ . In the case of $\delta > t_{\text{offset}}$, the difference between the input and the estimated value is $\tau - \delta$ which is smaller than the resolution τ of the TDC. In the case of $\delta < t_{\text{offset}}$, the fine step counts one more cycle and the error increases to $2\tau - \delta$. By careful symmetric layout, we reduce $t_{\text{offset}} < 2$ ps, which is quite small when compared to the range of the TDC.

C. Digitally Controlled Oscillator

Because the resolution of the cyclic Vernier TDC is determined by the frequency difference between the two DCOs, fine frequency control is necessary. In the previous study [6], there is no frequency tuning mechanism except the gating function. Our previous work included a DCO with a single control for frequency tuning [27]. In this work, we propose a DCO with dual frequency control. Figure 11 shows the schematic of the DCO. The oscillation is enabled by START and STOP signals for the slow and fast DCOs, respectively. The layout of this system is carefully designed to enhance matching between the two DCOs; the inverter stages of two DCOs are placed in an interdigitated manner and the binary-weighted current mirrors are designed using the common-centroid layout with a dummy. The dual-frequency control is implemented using four-bit control word $\text{CTL}\langle 3:0 \rangle$ and a tuning voltage V_{tune} applied to the current mirrors globally controls the amount of the current to the DCO. The $\text{CTL}\langle 3:0 \rangle$ adjusts the fine current via the digital-to-analog converter that acts as the discrete frequency controller for the DCO. The frequency f_{DCO} of the DCO can be expressed as

$$f_{\text{DCO}} = \frac{1}{2 \times [T_{\text{D,NAND}} + (N_{\text{stg}} - 1)T_{\text{D,INV}}]} \quad (6)$$

where $T_{\text{D,NAND}}$ and $T_{\text{D,INV}}$ is the delay of the NAND gate and the inverter, respectively. When V_{tune} and $\text{CTL}\langle 3:0 \rangle$ are applied, only $T_{\text{D,INV}}$ is varied while $T_{\text{D,NAND}}$ is kept constant. Even though $T_{\text{D,NAND}}$ is not controlled, it does not have much impact on the precise quantization of f_{DCO} . This is because we are able to achieve fine-tuning of f_{DCO} using V_{tune} . By varying $T_{\text{D,INV}}$, the proposed dual frequency control method achieves frequency tuning in 20 kHz steps over a 4.8 MHz range.

Figure 11. Schematic of the DCO.

The RSTD is a reset signal for the DCO. When the conversion is finished, it stops the DCO to reduce power consumption. After the conversion, the counter is reset as is the accumulated jitter. This observation suggests that the error can be reduced by increasing the operating frequency of the DCO. However, the high operating frequency is accompanied by increased jitter. With this tradeoff and power consumption in mind, we choose the frequency of two DCOs to be 43.1 and 43.8 MHz. This corresponds to the resolution $\tau = 371$ ps.

D. Edge-Type Detector

Figure 12 shows the schematic of the edge-type detector. The detector receives inputs DETECT and ENB and generates the EDGE and RSTD signals. The detector includes a D-F/F and a latch. The EDGE is generated through the D-F/F. The RSTD signal is generated through the latch which is controlled by the DETECT signal. This approach is used to ensure proper detection of edge alignment of the two DCOs. There are two transitions of DETECT signal (see Figure 4). The first transition occurs when OSC_F is starting and sets the DETECT signal to high. DETECT then transitions to low when alignment occurs. To prevent detecting a false alignment, the ENB signal is used to discard the first transition of the DETECT signal.

Figure 12. Schematic of the edge-type detector.

The ENB signal is generated by the D-F/F in the digital controller (see Figure 3). Before the START signal, the low level of ENB keeps the RSTD at a high level. After the START signal, ENB is kept high. By the second transition of the DETECT signal, which indicates the end of conversion, the active-low RSTD signal is generated. This keeps the starting node of DCO high, thus freezing the oscillation, and it reduces power consumption by stopping the DCO.

The EDGE signal indicates the type of edge alignment. In the case when both OSC_S and OSC_F are rising at the moment of alignment, as shown in Figure 13a, the DETECT signal goes from high to low generating $EDGE = 0$. This case corresponds to $T_{fine} < T_S/2$. In the case of a rising/falling alignment, as shown in Figure 13b, the DETECT signal goes from low to high generating $EDGE = 1$. In this case, the duration of the fine step can be greater than half of a period. To handle this issue, we add $T_S/2$ when $EDGE = 1$ so that the fine counter can measure a duration smaller than $T_S/2$. In this way, the size of the fine counter is reduced by detecting both alignments. In addition, this strategy reduces power and increases conversion speed. Because of the operating sequence of the alignment detector in which OCS_F stops the CN_C signal (see Figure 9), CN_C is activated one more time. Since this occurs in every conversion, it can be considered as an offset to N_C . Accounting for the offset and the status of the EDGE signal, the estimated time input T_{input}^* is obtained using

$$T_{input}^* = (N_C - 1) \cdot T_S + EDGE \cdot (T_S/2) + N_F \cdot (T_S - T_F). \quad (7)$$

Figure 13. Waveform for two cases of EDGE bit. (a) Rising/rising alignment, (b) rising/falling alignment.

3. Measured Results

Figure 14 shows the chip microphotograph of the fabricated TDC with core layout. The size of the core is 0.028 mm². Figure 15a shows the measurement setup for the TDC. Before characterizing the TDC, the DCOs are operated in a free-running mode to determine and calibrate the oscillation frequencies. Two function generators (Agilent 33220A) are used to create input signals (START and STOP). To reduce the number of I/O pads, a parallel to serial converter is included in the chip. An field-programmable gate array (FPGA) board is used to collect and convert the serial output to 13-bit data. Two level shifters are used to interface between the FPGA and the TDC. Finally, the data is transferred to a computer for further processing.

Figure 14. Chip microphotograph of the TDC.

Characterizing the TDC is challenging, especially under the time sweep condition, because it requires precise control of time differences over a relatively long period. In this work, we use function generators to provide the START and STOP signals with slightly different frequencies. When the two signals are synchronized with a 1 Hz frequency difference, this method allows for increasing T_{input} in steps of 25 ps, as shown in Figure 15b. Thanks to the synchronization feature of the instrument, we precisely configure the time difference between two signals with a standard deviation of about 200 ps. Because the jitter from the equipment does not allow ideal time step, it does affect the test results. To handle this issue, we perform a number of measurements and take the average. In this way, the error caused by the jitter from the equipment can be averaged out. When combined with nonlinearity caused by mismatch, the linearity is further affected because more variation is added. Even with this nonlinearity, our measured result shows that the TDC achieves a relatively good linearity using the proposed approach (see Table 1).

Figure 15. (a) Measurement setup, (b) time sweep method.

Figure 16 shows the measured transfer characteristic of the TDC obtained by taking an average of eight measurements. Each measurement includes 14,400 steps with 25 ps increment. The result shows a relatively large input range of 355 ns. The maximum coarse and fine times of the proposed TDC are $(2^{N_c} - 1 + 0.5) \times T_S$ and $T_S/2$, respectively. The ‘−1’ term is used to correct the offset in the coarse clock; CN_C is activated one more time before OSC_F stops CN_C signal. The ‘+0.5’ term is added in consideration of the EDGE bit. The calculated result obtained using this expression is 371 ns which agree with the measured range. The inset of Figure 16 shows a magnified view of a portion of the curve. The resolution of a TDC is defined as the minimum time interval that a TDC can resolve [30], and it can be estimated as the reciprocal of the slope [6]. From the linear fitting curve of the data in Figure 16, we obtain a resolution of 377 ps, which agrees with the calculated resolution of 371 ps. The relatively low resolution is limited by the frequency difference of the two DCOs, which operate at a low speed for small power consumption; the result is still suitable for a long-range TOF application. When the result is used for range sensing, it corresponds to a detection range of 53.2 m and a resolution of 5.65 cm.

System level simulations of the TDC show that the power consumption depends on T_{input} ; a longer fine step requires extended DCO oscillation time before the alignment event occurs, thus, consuming more power. When we take an average value for the maximum $T_{\text{input}} = 355 \text{ ns}$, the TDC consumes 0.65 mW which is a total power (active and standby power). The latency also depends on the T_{input} ; it increases with each extended coarse cycle of T_{input} . When the maximum range is covered, it requires the longest conversion time and in this case, the conversion rate is 0.67 MS/s.

Figure 16. Measured transfer characteristic of the TDC.

We obtain DNL and INL using code density method [6]. The size of the bin is 15 and the maximum code is 941 LSB. Figure 17 shows the result before and after calibration. The calibration is required because the static test is swept over a relatively long T_{input} and the input signals can be corrupted by the jitter from the equipment. To deal with this issue, we perform calibration by removing incorrect codes by checking consistency with the previous and subsequent codes. Using this method, we calibrate out 349 codes (2.4%) which are out of range (3-sigma) among the 14,400 codes. We note that this calibration is not needed for single-shot measurement. After calibration, the TDC achieves a DNL of 1.41 LSB (maximum) and 0.28 LSB_{rms}. The INL performance is 2.31 LSB (maximum) and 0.96 LSB_{rms}. Before calibration, we obtain a DNL of 0.31 LSB_{rms} and an INL of 1.41 LSB_{rms}. When the INL is used to estimate the discrepancy between the estimated and real distance, the result corresponds to an error of 5.42 cm.

In cyclic TDCs based on an oscillator, nonlinearity occurs due to layout mismatch, supply noise, signal cross-talk, and PVT variation. Compared to other studies (see Table 1), the proposed TDC achieves good linearity. We note that the shape of INL is changed periodically. This is attributed to the accumulated nonlinearity in the coarse step. Using the measured data, we obtain the number of bits $N_{\text{Bit}} = \log_2(\text{maximum input range/resolution})$ to be 9.88 bits. Taking nonlinearity into consideration, we obtain the equivalent number of linear bits $N_{\text{linear}} = N_{\text{Bit}} - \log_2(\text{INL} + 1)$ to be 8.15 bits [23].

Figure 17. Measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the TDC.

The precision of the TDC is evaluated using the single-shot measurement. Figure 18 shows the result for three cases of T_{input} . In each measurement, we keep the same T_{input} and repeat the conversion up to 260,000 times, which is large enough to observe the precision of the TDC. The result shows a standard deviation, std_{TDC} , of 0.5, 0.8, and 0.7 LSB for $T_{\text{input}} = 41.2$, 148.3, and 217.7 ns, respectively. The results agree with our expectation that std_{TDC} increases with T_{input} due to accumulated jitter.

Figure 18. Single-shot measurement. (a) $T_{\text{input}} = 41.2$ ns, (b) 148.3 ns, (c) 217.7 ns.

Table 1 shows the performance comparison with other studies. The work in [5] integrates TDCs for single-photon avalanche diode array to perform time-correlated single-photon counting. By using an external delay-locked loop (DLL), this work reduces the circuit complexity; the drawback is relatively poor linearity. The work in [6] presents a gated-Vernier oscillator that achieves a resolution of 7.3 ps with a relatively small input range of 9 ns. Using a look-up table for correcting the INL error, this work achieves a DNL of 0.8 LSB_{rms} and an INL of 1.2 LSB_{rms}. The work in [13] presents a detailed analysis of compensating PVT variations for the TDCs. By using a global compensation loop based on a phase-locked loop (PLL), the TDC in this work achieves an input range of 716 ns with a resolution of 357 ps. The work in [21] realizes a cyclic TDC using a hardware description language (HDL) which allows chip synthesis with automatic place-and-route tools. The work in [23] presents a two-step TDC based on a pseudo-differential TVC and a 6-bit SAR ADC. This work achieves a high conversion rate of 120 MS/s with a power of 3.73 mW. These works achieve a high resolution of 5.5 ps [21] and 0.63 ps [23]. However, the input range is 4.5 ns and 0.3 ns, which is not sufficient for TOF applications that demand wide ranges. Another work in [31] presents per-pixel TDC for PET imaging. The result achieves a resolution of 64.5 ps with an input range of 50 ns, however, its relatively poor linearity (max INL = 3.9 LSB) needs further correction. Thus, this work can suffer from a large error when applied to a TOF range sensor. The work in [32] presents detailed circuit techniques for all digital TDC to achieve a high resolution of 10 ps, however, only a limited amount of measured data is available. Two works developed for TOF imager, which realizes the TDC using a ring oscillator and a ripple counter, present TDCs achieving a high input range [13,33]. By locking phase and frequency among the ring oscillators, the TDC in [33] achieves an input range of 2 μ s with a resolution of 125 ps. With a simple structure, it is suitable for realizing in-pixel TDCs for dTOF image sensors; compared to our work, the linearity performance (max INL = LSB) needs further improvement.

Table 1. Performance summary and comparison.

	[5]	[6]	[13]	[21]	[23]	[31]	[33]	This Work
Tech. (nm)	130	130	180	65	65	130	65	180
Area (mm ²)	-	0.03	<0.002	0.006	0.064	-	<0.001	0.028
Type	DLL based	Gated Vernier	Ring oscillator	Cyclic Vernier	TVC, SAR	Ring oscillator	Ring oscillator	Cyclic Vernier
Input range (ns)	64	9	716	4.5	0.3	50 *	2000	355
Resolution (ps)	62.5	7.3	357	5.5	0.63	64.5	125	377
Precision (LSB)	-	2.35	-	0.78	1.12	-	-	0.8
DNL (LSB _{rms})	<4	0.8	0.35	-	-	0.28	<2	0.28
INL (LSB _{rms})	<8	1.2	1.5	-	-	-	-	0.96
Max. INL (LSB)	8	2.6	-	1	3.0	3.9	3	2.3
Conv. Rate (MS/s)	0.4	1	0.5	10	120	-	-	0.67
Power (mW)	-	1.2	<0.01	2.0 [†]	3.73	1.19	0.5	0.65
N_{linear} ** (bit)	-	8.42	-	8.68	6.89	7.31	-	8.15
FOM ***	-	3.5	-	0.49	0.26	-	-	3.4

* An input range up to 261 ns was reported, but linearity was up to 50 ns. ** Equivalent number of linear bits $N_{\text{linear}} = N_{\text{Bit}} - \log_2(\text{INL} + 1)$. *** FOM = Power/(2 ^{N_{linear}} × Conv. rate) [pJ/conv.-step]. [†] This is the maximum power reported in the paper. TVC: time-to-voltage converter; SAR: successive approximation register; DNL: differential nonlinearity; FOM: figure of merit.

The results in Table 1 show that it is challenging to achieve both high dynamic range and high resolution with a good linearity. Those TDCs that target PLL applications achieve a high resolution with a good figure-of-merit (FOM), however, provide only a limited input range [21,23]. The systems developed for TOF applications provide an increased input range [5,32], but show relatively poor

linearity. References [21,23] achieve better FOM than ours, but these works are realized using the 65 nm process for a small input range of 4.5 and 0.3 ns, respectively. Obviously, the range is not suitable for TOF applications requiring a high input range. Except for [13,33], which are realized using a simple ring oscillator and a ripple counter, our work achieves the lowest power consumption. In the cyclic TDC, a large part of power is consumed by DCOs. Therefore, we carefully design the DCOs for low power: (1) we use the RSTD signal to stop the DCO when the conversion is done; (2) we use a small number of five ring stages; (3) we operate the DCOs in low speed although this approach trades the resolution for power. Overall, our TDC in this work achieves a relatively high input range of 355 ns with a good linearity and a low power.

The number of bits N_{Bit} can be used to quantify the dynamic range by considering input range and the resolution. A better metric is N_{linear} which takes the linearity performance into account. Compared to other work [23,31], our work achieves an N_{linear} of 8.15 which indicates good linearity. Increasing performance by 1-bit in an ADC with more than 12-bit resolution is challenging when both area and linearity is constrained. Even though the TDC in this study doesn't use a capacitor as do SAR ADC, the area and circuit complexity increase in a similar manner. Therefore, a TDC achieving both high dynamic range and resolution tends to be costly and power-hungry, which will be challenging to realize in portable applications. The proposed TDC is suitable for low-power TOF sensor applications demanding both a high input range and a good linearity.

4. Conclusions

In this paper, a low-power cyclic Vernier two-step TDC having a high input range has been designed, fabricated, and successfully characterized. The high input range is achieved by addressing the nonlinearity caused by the startup time in the conventional cyclic TDC. We solve this problem successfully by using DCOs with matched startup times and a high-precision alignment detector. The alignment detector performs precise detection of edge alignment of the two DCOs and controls the counters with proper timing to compensate for the delay caused by the startup time. The proposed TDC achieves a high input range up to 355 ns and a resolution of 377 ps while consuming an average power of 0.65 mW. The proposed TDC can find a useful application in various TOF applications such as TOF ranging and biomedical imaging.

Author Contributions: V.N.N. designed the TDC, performed the experimental work, and wrote the manuscript. D.N.D. performed circuit simulations and edited the manuscript. Y.C. gave comment to the paper and revised the manuscript. J.-W.L. conceived the project, organized the paper content, and edited the manuscript.

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