sensors

MDPI

Article

Time-Interleaved SAR ADC with Background Timing-Skew Calibration for UWB Wireless Communication in IoT Systems

Kiho Seong [1], Dong-Kyu Jung [1], Dong-Hyun Yoon [1], Jae-Soub Han [1], Ju-Eon Kim [2], Tony Tae-Hyoung Kim [2], Woojoo Lee [1] and Kwang-Hyun Baek [1,*]

1 School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, Korea; tjdrlgh@cau.ac.kr (K.S.); jdgring@cau.ac.kr (D.-K.J.); kindyoon@cau.ac.kr (D.-H.Y.); lynn2776@cau.ac.kr (J.-S.H.); space@cau.ac.kr (W.L.)

2 School of Electrical and Electronics Engineering, Nanyang Technology University, Singapore 639798, Singapore; jueon.kim@ntu.edu.sg (J.-E.K.); THKIM@ntu.edu.sg (T.T.-H.K.)

* Correspondence: kbaek@cau.ac.kr; Tel.: +82-2-820-5765

Received: 11 March 2020; Accepted: 21 April 2020; Published: 24 April 2020

Abstract: Ultra-wideband (UWB) wireless communication is prospering as a powerful partner of the Internet-of-things (IoT). Due to the ongoing development of UWB wireless communications, the demand for high-speed and medium resolution analog-to-digital converters (ADCs) continues to grow. The successive approximation register (SAR) ADCs are the most powerful candidate to meet these demands, attracting both industries and academia. In particular, recent time-interleaved SAR ADCs show that multi-giga sample per second (GS/s) can be achieved by overcoming the challenges of high-speed implementation of existing SAR ADCs. However, there are still critical issues that need to be addressed before the time-interleaved SAR ADCs can be applied in real commercial applications. The most well-known problem is that the time-interleaved SAR ADC architecture requires multiple sub-ADCs, and the mismatches between these sub-ADCs can significantly degrade overall ADC performance. And one of the most difficult mismatches to solve is the sampling timing skew. Recently, research to solve this timing-skew problem has been intensively studied. In this paper, we focus on the cutting-edge timing-skew calibration technique using a window detector. Based on the pros and cons analysis of the existing techniques, we come up with an idea that increases the benefits of the window detector-based timing-skew calibration techniques and minimizes the power and area overheads. Finally, through the continuous development of this idea, we propose a timing-skew calibration technique using a comparator offset-based window detector. To demonstrate the effectiveness of the proposed technique, intensive works were performed, including the design of a 7-bit, 2.5 GS/s 5-channel time-interleaved SAR ADC and various simulations, and the results prove excellent efficacy of signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of 40.79 dB and 48.97 dB at Nyquist frequency, respectively, while the proposed window detector occupies only 6.5% of the total active area, and consumes 11% of the total power.

Keywords: analog-to-digital converter (ADC); successive approximation register (SAR) ADC; time-interleaved SAR ADC; timing-skew calibration; comparator offset; ultra-wideband (UWB) wireless communication

1. Introduction

The fourth industrial revolution is upon us. Internet-of-things (IoT), big data analytics, and artificial intelligence (AI) are the representative leading-edge technologies that serve as enablers and facilitators of this revolution. In particular, the explosive growth of data produced via IoT has been

playing a pivotal role in building big data and creating AI learning data. The proliferation of the IoT is, in turn, attributable to tremendous researches and engineering efforts to develop new methodologies and techniques for low-power designs and wireless communication systems [1–4].

Ultra-wideband (UWB) wireless communication is one of the contributors to the prosperity of the IoT and is also one of the representative beneficiaries that is continuing to evolve with the IoT. With the continued development of UWB wireless communications, the demand for multi-GS/s (giga sample per second) high-speed and medium-resolution analog-to-digital converters (ADCs) have been ever-increasing [5–10]. To meet the high-speed requirements, flash ADCs have been the most widely used in UWB applications. However, these ADCs have decisive limitations in terms of power consumption and area as ADC resolution increases. Because of the limitations, most flash ADCs have been designed with less than 6-bit resolution [11–14], which makes it difficult to meet today's medium-resolution requirements.

The successive approximation register (SAR) ADCs are well-known power and area-efficient ADCs. In addition, the digital affinity of SAR ADCs enables scalability to various semiconductor technologies, thereby accelerating versatility. However, the SAR ADCs are not as fast as the flash ADCs because of their unique operating characteristic. Even if the SAR ADCs are designed to be relatively high speed, the power efficiency tends to be faded because power-hungry comparators and fast capacitive-digital-to-analog converter (CDAC) settling time are required.

To enable high-speed ADC designs while maintaining the power-efficient advantage, researches to apply the time-interleaved architecture to the SAR ADC have been intensively studied [5,15–23]. Parallel operations of several slow-running sub-ADCs provide the same parallelization effect as a single fast ADC, enabling the low-power and high-speed ADCs. Unfortunately, these time-interleaved SAR ADCs still have a critical drawback; mismatches between the sub-ADCs can significantly degrade overall ADC performance. More specifically, the time-interleaved ADCs suffer from offset mismatch, gain mismatch, and sampling timing skew between channels. Fortunately, the offset and gain mismatches cause constant errors regardless of the input frequency, so they can be easily corrected in the digital domain. However, calibrating the sampling timing skew is very challenging, because the errors strongly depend on the input frequencies [24].

The sampling error induced by the (sampling) timing skew can be analyzed in Figure 1. Figure 1a shows the basic structure of a time-interleaved SAR ADC that consists of N sub-ADCs. Given that the input $V_{in}(t)$ is applied to the sub-ADCs, as seen in Figure 1b, the timing skew (ΔT) gives rise to the voltage error (ΔV). The precise relationship between ΔT and ΔV is as follows:

$$\Delta V \approx \frac{\partial Vin(t)}{\partial t} \cdot \Delta T \tag{1}$$

Meanwhile, for a sinusoidal input, the signal-to-noise ratio (SNR) of the time-interleaved ADC, which includes the quantization noise and the timing-skew error, can be expressed as:

$$SNR = \frac{1}{\frac{1}{6}\left(\frac{2}{2^M}\right)^2 + \pi^2 \Delta T^2 {f_{in}}^2} \tag{2}$$

where M and f_{in} represent the ADC resolution and the input frequency, respectively. From the above equations, it can be seen that the timing skew (ΔT) degrades the SNR significantly as f_{in} increases.

The MATLAB simulation results of the 7-bit time-interleaved ADC reported in Figure 2 show a more intuitive relationship between the timing skew and the SNR degradation. As seen in the figure, faster f_{in} causes greater SNR degradation. To achieve the SNR above 40 dB, for example, the timing-skew error must be lower than 2.5 ps and 1.2 ps in case f_{in} = 1 GHz and f_{in} = 2 GHz, respectively.

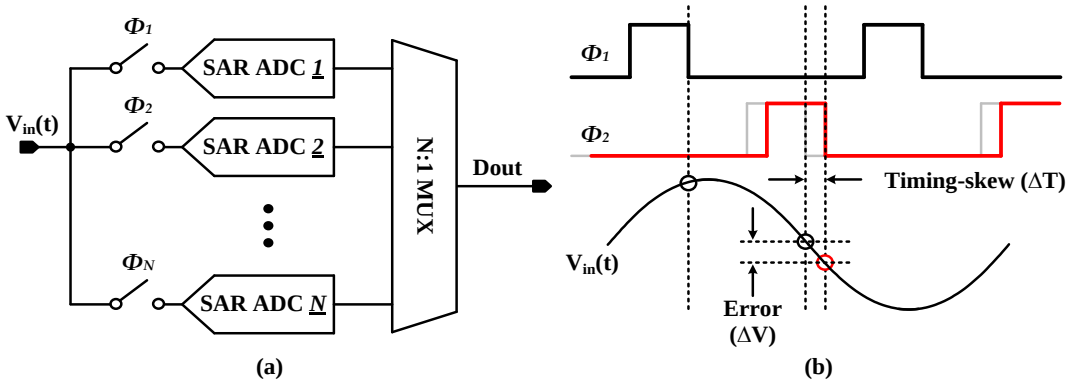

Figure 1. (**a**) Basic structure of a time-interleaved successive approximation register analog-to-digital converters (SAR ADC) and (**b**) timing-skew error in a time-interleaved SAR ADC.

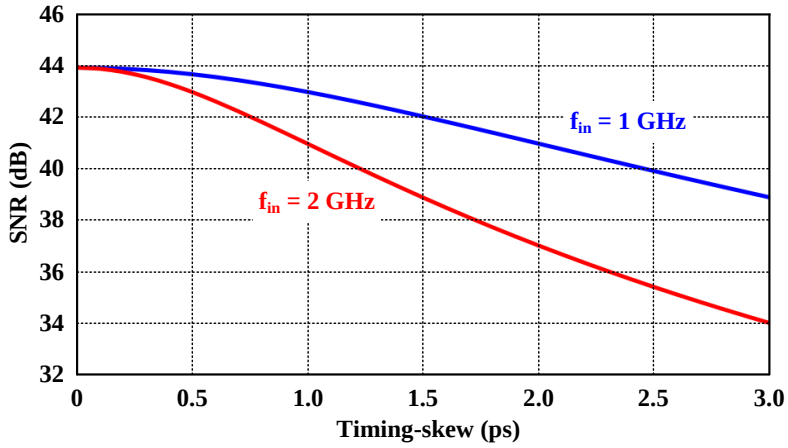

Figure 2. Signal-to-noise ratio (SNR) degradation of the 7-bit time-interleaved ADC due to the timing skews.

There have been extensive studies to overcome the timing-skew error problem of the time-interleaved ADCs, and the various timing-skew calibration techniques have been proposed [14–16,18–23,25–30]. In Section 2, the previous timing-skew calibration techniques will be reviewed in detail. Then, Section 3 introduces the proposed timing-skew calibration technique using a comparator offset-based window detector. The proposed technique includes a calibration algorithm that comes with a window detector design that is area efficient and robust to process–voltage–temperature (PVT) variations. More precisely, the detailed design and operating principle of the proposed window detector are presented in Section 3.1, while the proposed timing-skew calibration algorithm is elucidated in Section 3.2. Section 4 is dedicated to presenting detailed information about the simulation results, and Section 5 concludes the paper.

2. Timing-Skew Calibration Techniques: A Review

One of the best-known timing-skew calibration techniques is the statistic-based scheme proposed in several previous literatures [14,18,25,27,29]. This scheme tries to resolve the timing-skew error by maximizing the correlation between sub-ADCs or between sub-ADC and reference ADC. Due to the assumption that the input statistics are wide-sense-stationary (WSS), the statistic-based scheme has serious constraints on the input. In other words, if the input characteristics, such as frequency and statistics, change frequently, the WSS will be invalid and will limit the calibration, significantly reducing calibration accuracy.

Meanwhile, the derivative-based timing-skew calibration scheme was proposed in [21,26]. This scheme exploits an auxiliary ADC to get the input derivative and then calibrates for it by

extracting the direction and magnitude of the timing skew. Although this scheme effectively reduces timing-skew errors, it has a disadvantage of very high design complexity. Furthermore, this scheme is vulnerable to the PVT variations because it delays the input in the analog domain.

In addition, the flash-assisted timing-skew calibration scheme was introduced in [16,28]. This scheme adopts a flash-ADC as a timing-skew estimator and achieves considerable error mitigation. However, the power-consuming flash ADC results in power-efficiency degradation. Moreover, as the sampling speed increases, the power consumption may grow exponentially.

More recently, a timing-skew calibration scheme using a window detector was proposed [20,22,23]. The basic motivation for this scheme is that the timing-skew information can be obtained by detecting whether ΔV is within a specified window region or not. For example, when the window detector determines that the input is within the window, one of the sub-ADCs samples the input inside the window if there is no timing skew. This case is described in Figure 3a; the sub-ADC_n samples the input within the window. On the other hand, if the timing-skew exists, the corresponding sub-ADC_n will sample the input outside the window, which is illustrated in Figure 3b. Eventually, the timing skew can be calibrated by adjusting the sampling clock, thus allowing ΔV to enter the window region.

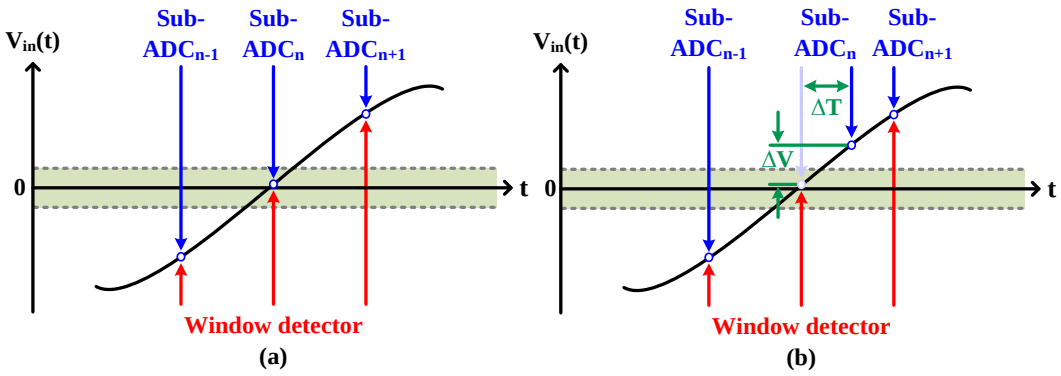

Figure 3. Concept of the window detector-based timing-skew calibration (**a**) without timing skew (**b**) with timing skew.

Then, detecting whether the input is in the specific window region or not is critical in this scheme. To this end, a detection technique using a comparator and its comparison time was presented in [20,23]. As shown in Figure 4, if the input voltage falls into the window region, the comparison time becomes longer than a certain time. Based on this relationship, a specific delay can be set and used to determine whether the input is in the window or not. Despite the successful detectability of this technique, additional calibration logics are required because the delay cell and comparison time are vulnerable to the PVT variations. And, unfortunately, the additional logics inevitably increase design complexity and power consumption.

To offload the additional calibration logics, a SAR-based window detector has recently been proposed [22]. Figure 5a shows the basic structure of the SAR-based window detector, and Figure 5b and c show the concept of its operating principle which consists of two steps: The first step is to determine whether the input voltage is greater or less than zero (which is the most significant bit (MSB) of the SAR conversion), and the second step is to switch the CDAC and then determine whether it is greater than zero again. If the input voltage is out of the window region, the comparator outputs of the first and second steps should be the same (Figure 5b). Otherwise, the two outputs should be different from each other (Figure 5c). Note that because the SAR-based window detector requires at least two comparison cycles (Φ_{comp}), the clock cycle following the sampling clock (Φ_{sample}) is used for comparison rather than sampling, as shown in Figure 5d. Therefore, the input impedance varies, and eventually, it causes the bandwidth mismatch. To solve this bandwidth mismatch problem, an extra dummy-SAR ADC is included in [22] to sample the input alternately with Φ_{sample} (Φ_{dummy}). However,

because of the extra dummy-SAR ADC, which occupies a large area, the presented technique still has critical limitations.

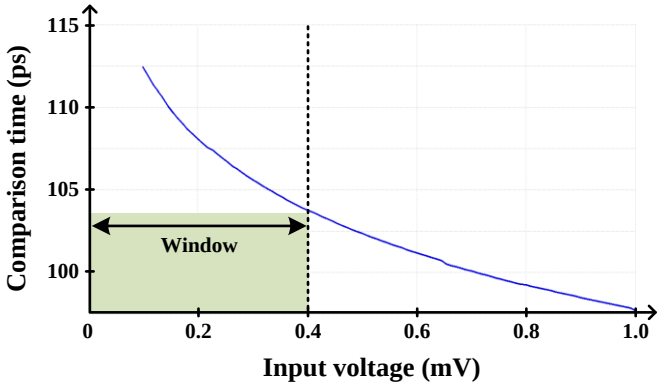

Figure 4. Relationship between the comparison time and input voltage.

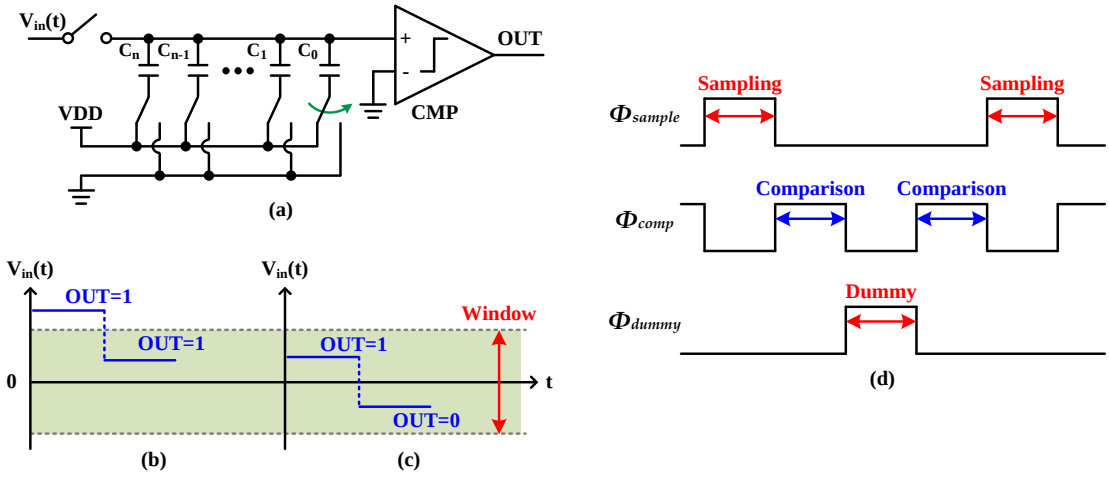

Figure 5. (**a**) Basic structure of the SAR-based window detector and its operating principle when (**b**) outside the window and (**c**) inside the window. The timing diagram is shown in (**d**).

This paper presents a new window detection scheme and the timing-skew calibration algorithm for the high-speed time-interleaved SAR ADCs. The proposed window detector is more resistant to PVT variations, and it has lower digital complexity than previous works [20,23]. In addition, it has a higher area efficiency than [22].

3. Proposed Timing-Skew Calibration Scheme

The block diagram of the proposed time-interleaved SAR ADC is described in Figure 6. The tsub-channel SAR ADC and window detector SAR ADC are illustrated in Figure 7a and b, respectively.

The sub-ADCs basically utilized the 2b/cycle architecture presented in [31–33], whereby conversion speed can be significantly enhanced. As seen in Figure 7a, the three differential-difference comparators (DDCs) [34] compare the sampled input differential voltage with three reference voltages, which are generated by reference CDACs. And they resolve 2-bit in each decision cycle. The nonbinary decision scheme is adopted to compensate for CDAC settling error and kickback noise [31,35]. Eventually, ADC resolves 8-bit, including 1-bit redundancy, and then the nonbinary-to-binary decoder convert it to 7-bit binary codes.

The window detector SAR ADC has a similar structure to sub-ADCs, except for the input cross-coupled comparators, which are used for window detection. The detailed explanations are mentioned in the following subsections.

The phase generator generates sampling clock phases of the sub-ADCs ($\Phi_{1\text{-}5}$) and that of the window detector SAR ADC (Φ_{WD}). Then the timing-skew calibration logics control the VDLs to align $\Phi_{1\text{-}5}$ with Φ_{WD}.

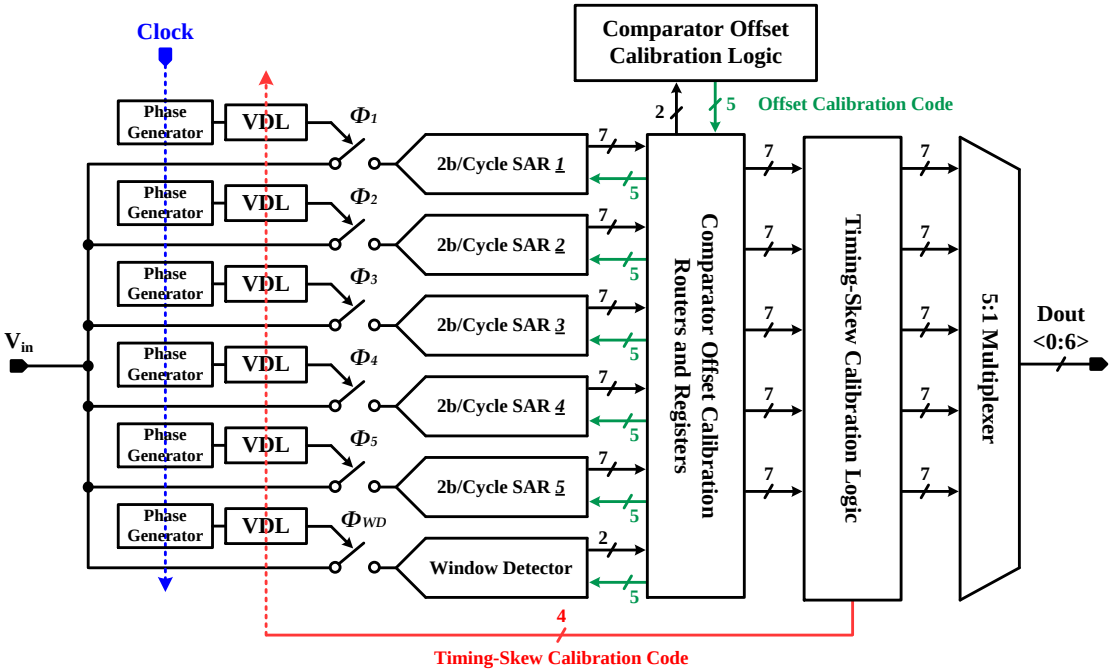

Figure 6. Block diagram of the proposed time-interleaved SAR ADC.

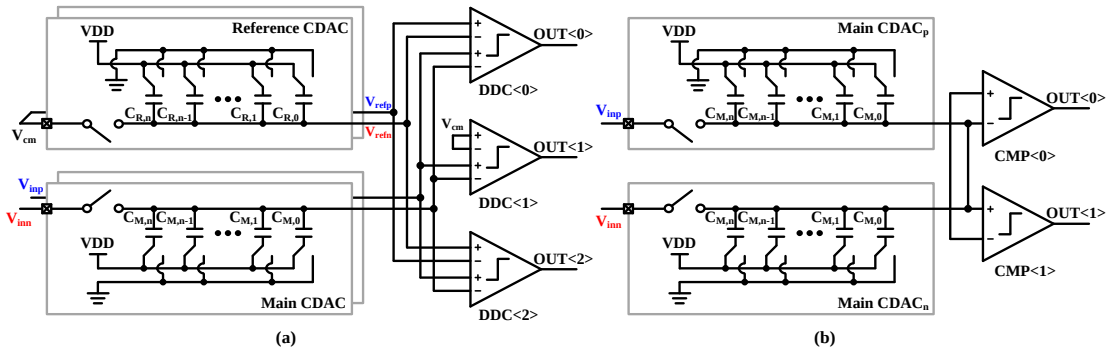

Figure 7. Block diagram of (**a**) the sub-channel 2b/cycle SAR ADC and (**b**) window detector SAR ADC.

The single offset calibration logic not only compensates the sub-ADC's offset but also makes the input cross-coupled comparators act as window detector. The total 17 comparators are used in the proposed architecture: 15 DDCs are used in the sub-ADCs, and the other two comparators (i.e., these are the differential comparators) are used in the window detector ADC. All these comparators are sequentially calibrated by single calibration logic and the calibration data are stored in the register in each ADC.

3.1. Comparator Offset-based Window Detector

The proposed window-detector SAR ADC has two differential comparators implemented in the Strong-ARM latch-based dynamic comparators [36], so as to operate at high speed while maintaining

high power efficiency. Figure 8 shows the detailed schematic of this differential comparator which consists of pre-amp ($M_{1,2,11}$), latch ($M_{3\text{-}6}$), reset switches ($M_{7\text{-}10}$), dummy input transistors (M_{Dum}) for kick-back noise reduction, and offset calibration transistors ($M_{F,C}$).

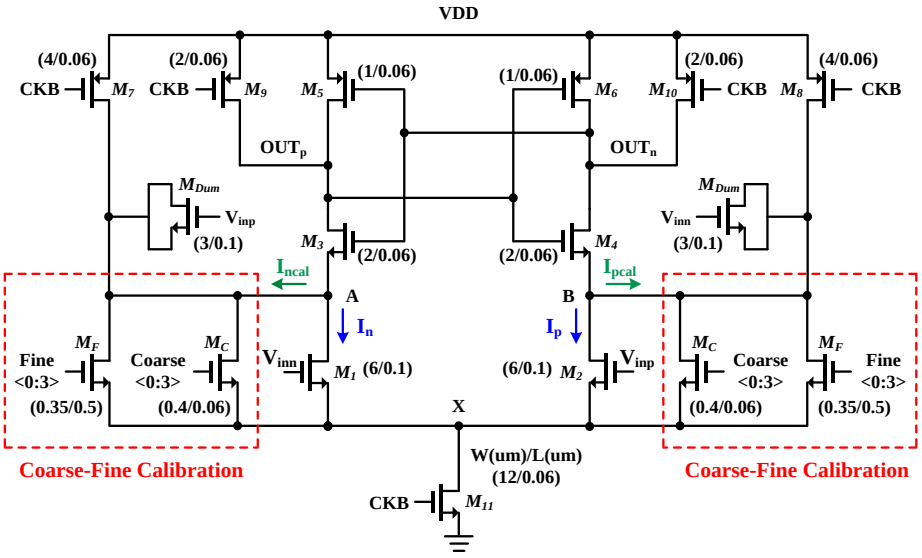

Figure 8. Schematic of the differential comparator with offset calibration transistors.

Because the input difference of comparator makes different currents, if $V_{inp} > V_{inn}$, then $I_p > I_n$, it leads to OUT_p and OUT_n to be VDD ("1") and GND ("0"), respectively, due to the regeneration of the latch. (i.e., we define that the comparator output is "1" when OUT_p is VDD). However, if there is an offset, despite $V_{inp} > V_{inn}$, it makes $I_n > I_p$. In this case, the comparison error can be corrected by calibration current (I_{pcal}) by turning on $M_{F,C}$ connected in parallel with input transistor M_2.

If there is no offset, and the input difference is zero, the comparator outputs will be randomly distributed to "1" or "0". However, if there is an offset, the outputs will remain "1" or "0", even though the input difference is zero. Therefore, by applying the input difference to zero and monitoring the comparator outputs, it is always possible to see if there is an offset. And, from this confirmation, the offset calibration can be conducted.

Figure 9 presents the block diagram of the offset calibration logic. After shorting the inputs to the common-mode voltage (V_{cm}), the comparator outputs control the up–down counter. If the comparator keeps outputs either "1" or "0", the up–down counter will reach the specific code (OS+ or OS-), and then it turns on or off the calibration transistors ($M_{F,C}$).

If a small offset remains after a series of the offset corrections, the comparator output may appear slightly alternating between "1" and "0", it can be detected by majority voting scheme [37]. That is, the up–down counts compete and then, one of them reaches the specific code first, the calibration is performed.

As aforementioned, we propose to use the comparators which have inevitable offset as the window detector. Figure 10a and b show the input cross-coupled comparators without and with offset (OS_{WD}), respectively. As seen in Figure 10c and d, if there is no offset, the comparator outputs are must always be opposite, regardless of the input voltage. However, if there is an offset, the comparator outputs are the same when the input voltage falls into the window region. Whereas, if the input voltage is out of the window region, the comparator outputs are opposite again. Therefore, the input cross-coupled comparators with inevitable offset can be used as the window detector.

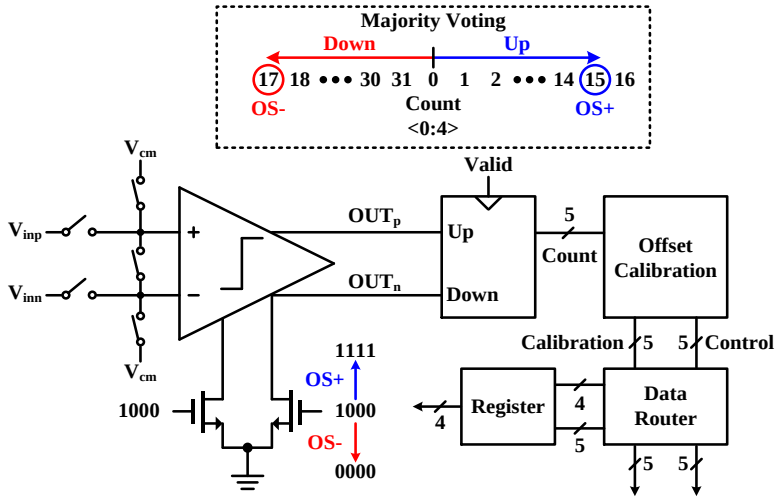

Figure 9. Block diagram of the offset calibration logic with the majority voting scheme.

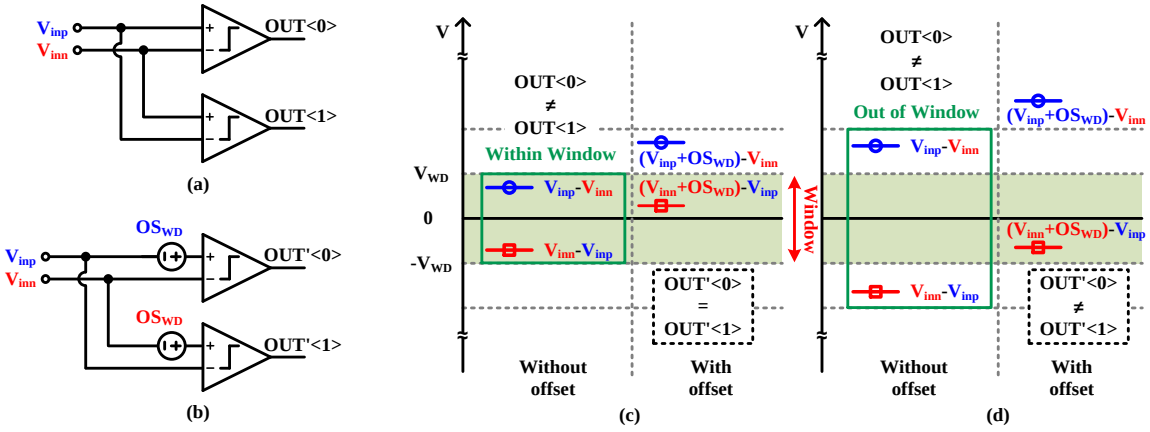

Figure 10. The input cross-coupled comparators (**a**) without and (**b**) with offset, and the comparator outputs equality (**c**) inside, and (**d**) outside window.

In this scheme, the smaller window width, the longer calibration convergence time, so it may not be able to keep up with temperature and voltage variations that have a significant effect on timing skew. On the other hand, the larger window width, the lower calibration accuracy.

Figure 11 shows the relationship between window width, calibration accuracy, and convergence time. If W = 1 least significant bit (LSB), it needs more than 130 k samples to converge within ±1 ps skew. Whereas, if W = 2 LSB, it needs 70 k samples to converge within ±1 ps skew. Its convergence time is half of W = 1 LSB while maintaining ±1 ps accuracy. On the other hand, if W = 10 LSB, although it needs only 40 k samples to converge, its accuracy is very poor which is ~6 ps. Therefore, taking this trade-off between convergence time and accuracy into consideration, we determine to set the window width to 2 LSB (±1LSB, ±15 mV).

Since the window width of the proposed offset-based window detector is determined by offset, it is necessary to control the offset to set the window width. To force the desired offset, the unwanted offset induced from the process random mismatch must be first compensated.

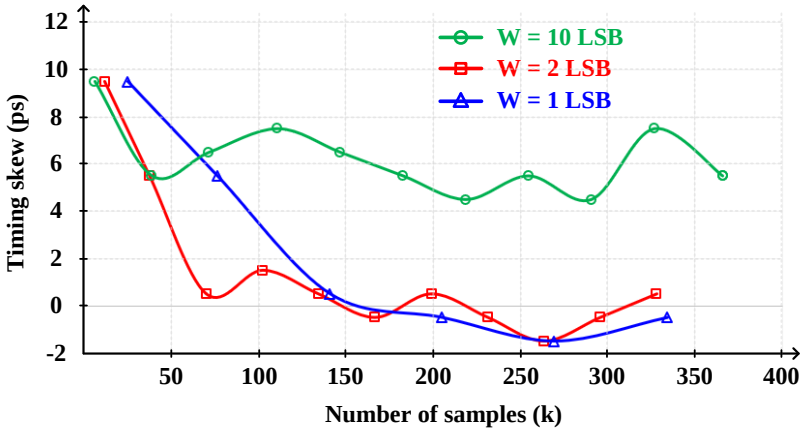

Figure 11. Relationship between window width, calibration accuracy and convergence time.

To this end, it is important to know how much offset could be caused by process mismatch. From the Monte-Carlo simulation and post-layout parasitic extraction, the offset is estimated to be ±48 mV. The additional calibration transistors are connected in parallel with the input transistors to compensate the offset. To control the offset 1.5 mV accuracy, the compensation current (I_{pcal} and I_{ncal} in Figure 8) must be much smaller than the main current (I_p and I_n in Figure 8). To this end, long-channel transistors are used for calibration. Furthermore, to calibrate such ±48 mV offset, it is necessary that more than 6-bit extra transistors are needed. It results in large parasitic capacitance and limits the speed of the comparator. To tackle this issue, we adopt the coarse-fine calibration; that is, first the short-channel transistors cover ±48 mV range with 8.5 mV accuracy, then the long-channel transistors control the offset with 1.5 mV accuracy. Therefore, only 4-bit long-channel transistors are required, allowing accurate calibration while maintaining the comparator speed.

In practically, because the comparator has a random offset which is unwanted offset (OS), it is necessary to force only the desired offset (OS_{WD}) corresponding to the window width. For this, the differential CDACs sample the common-mode voltage (V_{cm}) and the C_{WD} on the positive input side is switched from VDD to GND which shifts the sampled input difference to "-OS + (-OS_{WD})". It is described in Figure 12a,b. This is equivalent to having offset of "-OS + (-OS_{WD})", so if the offset calibration logic compensates it, the input difference will change to zero again. After storing the calibrated offset in the comparator, sampling the V_{cm} again, if the C_{WD} is not switched, the offset of OS_{WD} is forced as described in Figure 12b. It is because the offset calibration compensates the unwanted offset "-OS" as well as "-OS_{WD}" made by C_{WD} switching. Therefore, the only desired offset (OS_{WD}) value remains.

Note that because the window width of the proposed window detector is determined by the switched capacitor (C_{WD}) ratio and it has a similar structure to sub-ADCs, it is thus advantageous to resist the PVT variations than comparison time-based window detector [20, 23]. If the offset is forced on both comparators, the comparators can be used as window detector with only one conversion cycle.

Finally, compared with previous works [20,22,23], the proposed circuit does not require the additional calibration to adjust the window width, thanks to its resistance to PVT variations. Furthermore, because it requires only one comparison cycle, eliminating the need for the extra dummy-SAR ADC to compensate for input impedance variations.

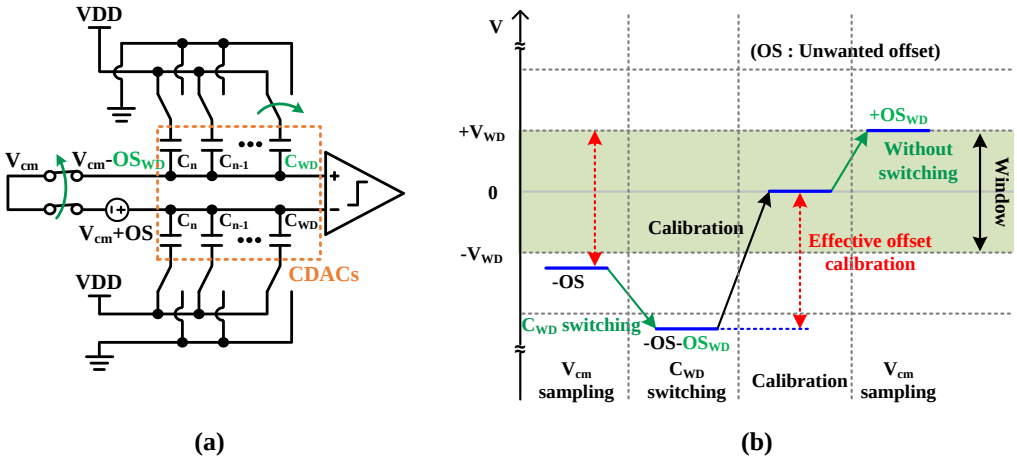

Figure 12. The offset calibration after C_{WD} switching to force desired offset.

3.2. Timing-Skew Calibration Algorithm

The mean absolute deviation-based (MAD) timing-skew calibration [23] is adopted to reduce digital complexity and power consumption. Because MAD does not need multiplier, unlike variance-based calibration. The detail of MAD timing-skew calibration is as follows.

If there is no timing-skew, the digital outputs of each sub-ADC, D_{out}'s, should be gathered near the zero because the window is set near the zero-crossing as seen in Figure 13. Therefore, the mean absolute values of D_{out}'s, $E(|D_{out}|)$, tends to be very small [23]. However, if there is timing skew, $E(|D_{out}|)$ may become very large, because D_{out}'s are distributed far from the zero. Therefore, the timing skew can be minimized by adjusting the sampling clock in a direction that can minimize $E(|D_{out}|)$.

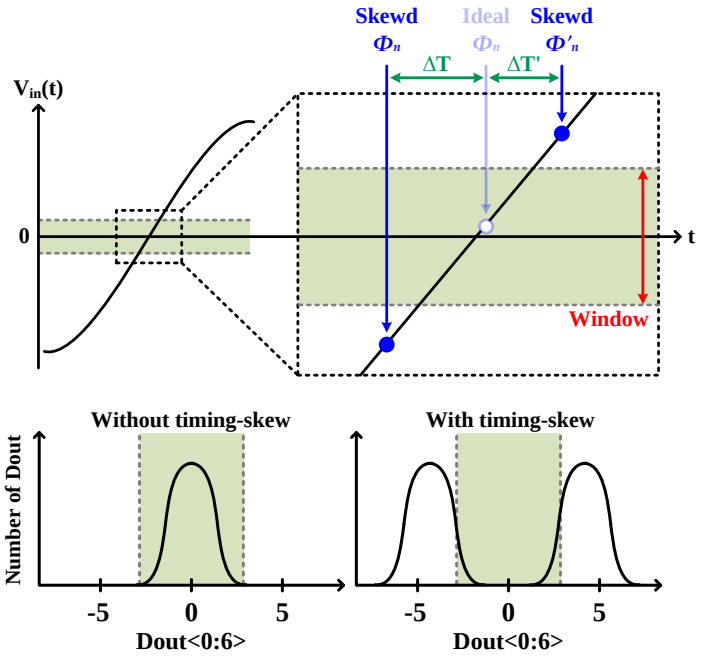

Figure 13. Histograms of D_{out} without and with timing skew.

Figure 14 shows the block diagram of the proposed timing-skew calibration. The calibrator initially controls the VDL to lead or lag the sampling clock in an arbitrary direction. And then, the digital integrator takes absolute values of D_{out}'s and integrates them for each cycle. After the integration, the timing-skew arbiter compares $E(|D_{out}|)$ with the previous one and investigates whether the timing

skew is reduced or increased compared to the previous cycle. Then, if the timing skew is reduced, the arbiter commands the calibrator to keep the adjustment direction of VDL the same as before (keeping the sampling clock lead or lag as it did in the previous cycle). Other if the timing skew increases, the arbiter instructs the calibrator to invert the adjustment direction of VDL in the previous cycle.

To help readers better understand the above procedure, let us look at an example of the operation of each block in the n^{th} cycle. After all, the D_{out}'s at n^{th} cycle are integrated by the digital integrator, n^{th} mean value of $|D_{out}|$'s, $E_n(|D_{out}|)$ is compared with the previous $E_{n-1}(|D_{out}|)$. If $E_n(|D_{out}|) \leq E_{n-1}(|D_{out}|)$, the arbiter judges that the calibrator is currently working correctly and instructs the calibrator to run the same as the last cycle. In the opposite case, the arbiter instructs the calibrator to operate in reverse to the previous cycle. Then the calibrator controls the VDL to make the sampling clock lead or lag, resulting in timing-skew reduction at $(n+1)^{th}$ cycle. Note that the timing-skew calibration operates in the background to track the voltage–temperature variations.

Meanwhile, to cover the estimated timing skew (3σ = 25 ps) acquired from the Monte-Carlo simulation and post-layout extraction, the VDL's control range is set to ±28 ps, and the accuracy is set to ~1 ps to achieve the SNR above 40 dB at f_{in} = 1.25 GHz. Plus, to avoid too much load on the VDL, it utilizes a coarse-fine structure, allowing the delay to be linearly controlled.

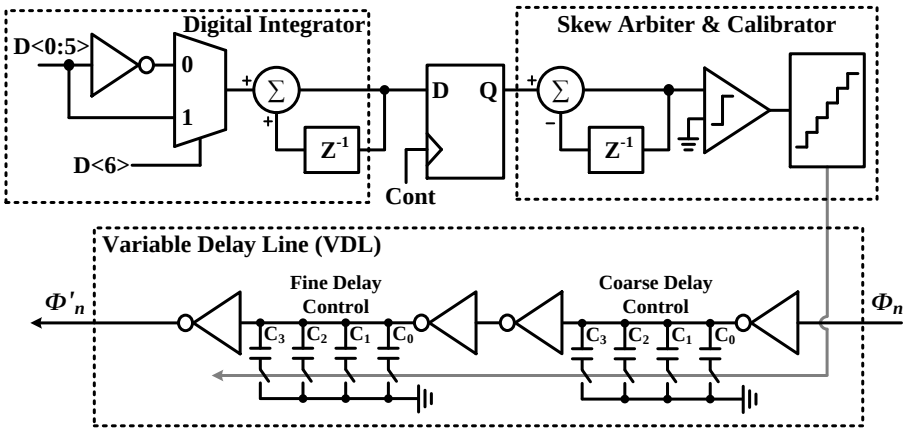

Figure 14. Block diagram of the proposed timing-skew calibration.

4. Results

To verify the proposed timing-skew calibration technique using the comparator offset-based window detector, we have performed intensive works, including designing a 7-bit, 2.5 GS/s 5-channel time-interleaved SAR ADC in 65 nm CMOS process and post-layout simulations. The top layout of the proposed time-interleaved SAR ADC is presented in Figure 15. The active area was 0.4 mm^2, of which the calibration logics and window detector SAR ADC occupied 0.05 mm^2 and 0.026 mm^2, respectively. The proposed window detector only occupied 6.5% of the total area. The total power consumption of the ADC was 24 mW at 1.2 V supply. The proposed window detector only consumes 11% of the total power. The detailed SAR ADC design process and the various works using it are as follows.

In our time-interleaved SAR ADC design, we first focused on minimizing the offset and gain mismatches that cause not only window detection errors but also degrade SNR significantly. To this end, a full-custom metal-oxide-metal (MOM) capacitor was designed for a unit capacitor (~ 4fF) of CDAC to minimize the gain mismatch. Thanks to proper layout and good matching property, the gain mismatch became small enough to ignore the impact on target degradation.

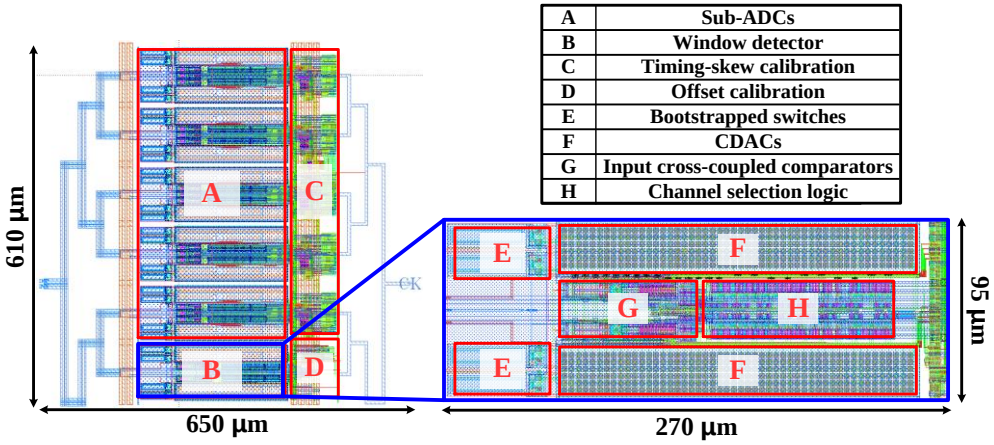

Figure 15. Top layout of the proposed time-interleaved SAR ADC.

Figure 16 shows the differential non-linearity (DNL) and integral non-linearity (INL) with post-layout extraction of CDAC and an additional 1% random mismatch. As shown in simulation results (Figure 16), the DNL and INL were below 0.15 LSB.

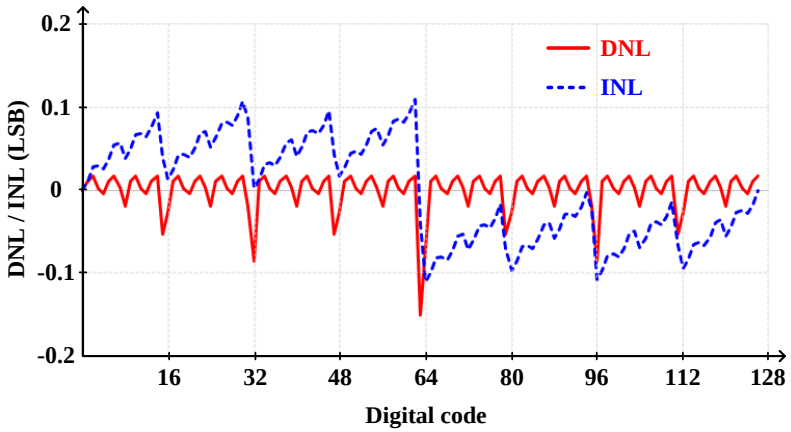

Figure 16. Differential non-linearity (DNL) and integral non-linearity (INL) with post-layout extraction of CDAC and an additional 1% random mismatch.

In addition, regarding the offset mismatch, assuming that the process random mismatch represents a Gaussian distribution, the offset can be predicted by curve-fitting the probability of the comparator output "1" to the normal cumulative distribution function (CDF). The estimated offset through the Monte-Carlo simulation was ±48 mV (3σ).

The offset calibration convergence for DDCs is illustrated in Figure 17. As aforementioned, because single calibration logic calibrated the 17 comparators sequentially, the n^{th} comparator must be calibrated after calibration for $(n\text{-}1)^{th}$. Therefore, the calibrated comparators kept its calibration data in the register, while others that have not yet been calibrated maintain its initial data. The 5-bit calibration with ~5 mV accuracy was used for the DDCs, because they did not need coarse-fine calibration, unlike window detecting comparators. It was enough to achieve the SNR above 40 dB. The offset of each comparator was modeled by the Monte-Carlo simulation. In fact, the 15 DDCs were calibrated, but for easy readability, we only show three representative simulation results in the figure.

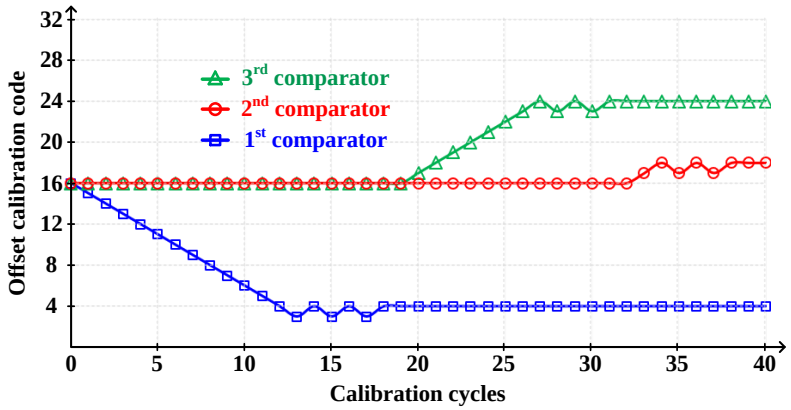

Figure 17. The offset calibration convergence for differential-difference comparators (DDCs).

Figure 18 shows the coarse-fine offset calibration convergence for window detecting comparator, and its corresponding forced offset voltage. To force 15 mV offset, the ~8.5 mV coarse calibration was performed first, followed by ~1.5 mV fine calibration. As the calibration progressed, the offset voltage was forced to ~15 mV corresponding to 1 LSB. Thus, the window width was set to 2 LSB (±15 mV)

In the case of the sub-ADC, Ch.1 and Ch.2 had +23 ps and -20 ps timing skews, respectively, the timing-skew calibration convergence is described in Figure 19. The coarse calibration was performed first with ~3 ps accuracy, followed by fine calibration with ~1 ps accuracy. The total calibration range was ~±28 ps. In total, five sub-ADCs were calibrated, but due to lack of space, we only report two simulation results in this paper.

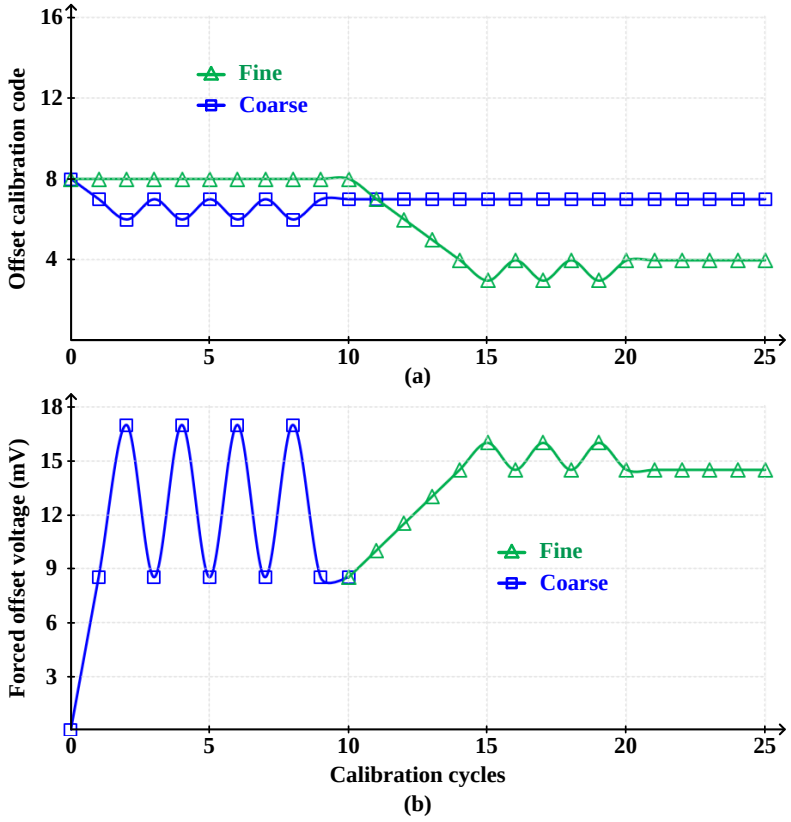

Figure 18. (**a**) The coarse-fine offset calibration convergence for window detecting comparator, and (**b**) its corresponding forced offset voltage.

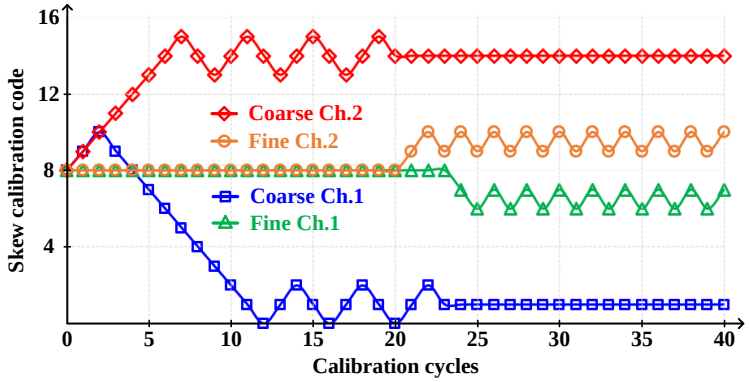

Figure 19. The coarse-fine timing-skew calibration convergence.

We performed the fast Fourier transform (FFT) analysis of a sinusoidal input signal at Nyquist frequency, and the results are shown in Figure 20. Before the calibrations, spurs caused by the offset and timing skew significantly degraded SNDR and SFDR, reaching 17.59 dB and 23.69 dB, respectively, as seen in Figure 20a.

The offset mismatch spurs were suppressed from 2.92 dB to −12.28 dB after offset calibration. However, due to the timing-skew spurs, the SNDR and SFDR were still in 17.84 dB and 23.57 dB, respectively, as shown in Figure 20b.

The timing-skew spurs were suppressed from 12.4 dB to −23.68 dB after timing-skew calibration. After performing both calibrations, even though the spurs were not completely disappeared, they were suppressed enough to achieve 40 dB SNDR. Eventually, the SNDR and SFDR at Nyquist frequency were 40.79 dB and 48.97 dB, respectively, as seen in Figure 20c.

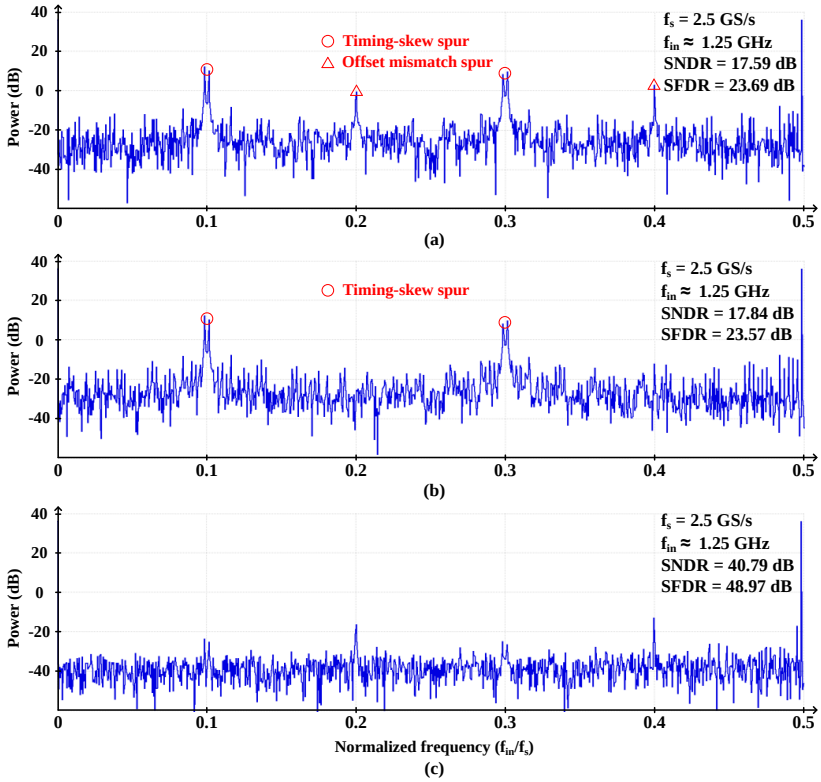

Figure 20. Fast Fourier transform (FFT) analysis of a sinusoidal input signal at Nyquist frequency (**a**) without calibration, (**b**) with offset calibration only, and (**c**) with both offset and timing-skew calibration (4096 points for FFT).

Finally, Table 1 compares the proposed window detector with previous works. Compared to the previously published window detectors, the proposed circuit does not require additional calibration because of immunity to PVT variation and mitigates the burden of extra dummy-ADC. And the digital complexity is lower than a variance-based calibration because MAD does not use a digital multiplier.

Table 2 summarizes and compares the performance of the proposed time-interleaved SAR ADC to previously published time-interleaved ADCs with a similar sampling rate and resolution. The proposed time-interleaved SAR ADC shows the best SNDR among the comparisons and achieves the top-flight Walden figure-of-merit (FoM_w) of 108-fJ/conversion step at the Nyquist frequency.

Table 1. Feature comparison.

	This Work [1]	[20]	[22] [1]	[23]
PVT sensitivity	robust	sensitive	robust	sensitive
Additional calibration	no	needed	no	needed
Area overhead	medium	low	high	low
Calibration method	MAD	variance	variance	MAD
Digital complexity	low	high	high	low

[1] Post-layout simulation results.

Table 2. Performance comparison.

	This Work [1]	[5]	[7]	[17]	[19]
Architecture	TI SAR	TI SAR	TI Subranging	TI SAR	TI SAR
Technology (nm)	65	45	65	40	40
Supply voltage (V)	1.2	1.1	1	1.2	1.1
Sampling rate (GSPS)	2.5	2.5	2.2	2.64	2
Resolution (bit)	7	7	7	8	8
SFDR (dB) at Nyquist	48.97	43	45.95	-	55
SNDR (dB) at Nyquist	40.79	34	37.96	38	39.4
Power (mW)	24	50	40	39	54.2
FoM_w [2] (fJ/conv.-step)	108	480	280	230	355

[1] Post-layout simulation results. [2] FoM_w = power / ($f_s \cdot 2^{ENOB\ at\ Nyquist}$), where ENOB = (SNDR-1.76) / 6.02.

5. Conclusions

Beginning with the thorough analysis of the advantages and disadvantages of previous time-interleaved SAR ADC designs and their indispensable timing-skew calibration techniques, we have proposed the timing-skew calibration technique using the comparator offset-based window detector. With the proposed calibration algorithm, the design methodology and operation principle of the comparator offset-based window detector are provided in detail. To demonstrate the effectiveness of the proposed technique on the timing-skew calibration, a 7-bit, 2.5 GS/s 5-channel time-interleaved SAR ADC was designed using 65 nm CMOS technology and intensive works were performed. It proves that the proposed calibration scheme well suppressed the mismatch spurs and improves the SNDR and SFDR from 17.59 dB and 23.69 dB to 40.79 dB and 48.97 dB, respectively. The calibration only increased by 6.5% effective area and 11% power consumption, which can be translated to achieving the best FoM_w among the comparisons.

Author Contributions: Conceptualization, methodology, validation, K.S; investigation, resources, data curation, D.-K.J., D.-H.Y., J.-S.H., J.-E.K., and T.T.-H.K.; writing—original draft preparation, K.S.; writing—review and editing, W.L. and K.-H.B.; supervision, project administration, K.-H.B. All authors have read and agreed to the published version of the manuscript.

Acknowledgments: This research was supported by the Chung-Ang University Graduate Research Scholarship in 2018 and supported by Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) (N0001883, The Competency Development Program for Industry Specialist)

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Islam, S.M.R.; Kwak, D.; Kabir, M.H.; Hossain, M.; Kwak, K. The Internet of Things for Health Care: A Comprehensive Survey. *IEEE Access* **2015**, *3*, 678–708. [CrossRef]
2. Marjani, M.; Nasaruddin, F.; Gani, A.; Karim, A.; Hashem, I.A.T.; Siddiqa, A.; Yaqoob, I. Big IoT Data Analytics: Architecture, Opportunities, and Open Research Challenges. *IEEE Access* **2017**, *5*, 5247–5261. [CrossRef]
3. Lee, W.; Kang, T.; Lee, J.; Han, K.; Kim, J.; Pedram, M. TEI-ULP: Exploiting Body Biasing to Improve the TEI-Aware Ultralow Power Methods. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2019**, *38*, 1758–1770. [CrossRef]
4. Yoon, D.; Jung, D.; Jung, B.; Choi, J.; Jo, Y.; Lee, S.; Lee, W.; Baek, K. LW-DEM: Designing a Low Power Digital-to-Analog Converter Using Lightweight Dynamic Element Matching Technique. *IEEE Access* **2019**, *7*, 112617–112628. [CrossRef]
5. Alpman, E.; Lakdawala, H.; Carley, L.R.; Soumyanath, K. A 1.1 V 50 mW 2.5 GS/s 7b Time-Interleaved C-2C SAR ADC in 45 nm LP digital CMOS. In Proceedings of the 2009 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 8–12 February 2009; pp. 76–77.
6. Nakajima, Y.; Sakaguchi, A.; Ohkido, T.; Kato, N.; Matsumoto, T.; Yotsuyanagi, M. A Background Self-Calibrated 6b 2.7 GS/s ADC With Cascade-Calibrated Folding-Interpolating Architecture. *IEEE J. Solid-State Circuits* **2010**, *45*, 707–718. [CrossRef]
7. Ku, I.; Xu, Z.; Kuan, Y.; Wang, Y.; Chang, M.F. A 40-mW 7-bit 2.2-GS/s time-interleaved subranging ADC for low-power gigabit wireless communications in 65-nm CMOS. In Proceedings of the 2011 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 19–21 September 2011; pp. 1–4.
8. Sung, B.; Lee, C.; Kim, W.; Kim, J.; Hong, H.; Oh, G.; Lee, C.; Choi, M.; Park, H.; Ryu, S. A 6 bit 2 GS/s flash-assisted time-interleaved (FATI) SAR ADC with background offset calibration. In Proceedings of the 2013 IEEE Asian Solid-State Circuits Conference (A-SSCC), Singapore, 11–13 November 2013; pp. 281–284.
9. Tai, H.; Tsai, C.; Tsai, P.; Chen, H.; Chen, H. A 6-bit 1-GS/s Two-Step SAR ADC in 40-nm CMOS. *IEEE Trans. Circuits Syst. II Express Briefs* **2014**, *61*, 339–343. [CrossRef]
10. Chung, Y.; Rih, W.; Chang, C. A 6-bit 1.3-GS/s Ping-Pong Domino-SAR ADC in 55-nm CMOS. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 999–1003. [CrossRef]
11. Park, S.; Palaskas, Y.; Flynn, M.P. A 4GS/s 4b Flash ADC in 0.18/spl mu/m CMOS. In Proceedings of the 2006 IEEE International Solid State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 6–9 February 2006; pp. 2330–2339.
12. Park, S.; Palaskas, Y.; Ravi, A.; Bishop, R.E.; Flynn, M.P. A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS. In Proceedings of the IEEE Custom Integrated Circuits Conference 2006, San Jose, CA, USA, 10–13 September 2006; pp. 489–492.
13. Deguchi, K.; Suwa, N.; Ito, M.; Kumamoto, T.; Miki, T. A 6-bit 3.5-GS/s 0.9-V 98-mW Flash ADC in 90-nm CMOS. *IEEE J. Solid-State Circuits* **2008**, *43*, 2303–2310. [CrossRef]
14. El-Chammas, M.; Murmann, B. A 12-GS/s 81-mW 5-bit Time-Interleaved Flash ADC With Background Timing Skew Calibration. *IEEE J. Solid-State Circuits* **2011**, *46*, 838–847. [CrossRef]
15. Dortz, N.L.; Blanc, J.; Simon, T.; Verhaeren, S.; Rouat, E.; Urard, P.; Tual, S.L.; Goguet, D.; Lelandais-Perrault, C.; Benabes, P. 22.5 A 1.62 GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70dBFS. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 386–388.
16. Lee, S.; Chandrakasan, A.P.; Lee, H. A 1 GS/s 10b 18.9 mW Time-Interleaved SAR ADC With Background Timing Skew Calibration. *IEEE J. Solid-State Circuits* **2014**, *49*, 2846–2856. [CrossRef]
17. Kundu, S.; Alpman, E.; Lu, J.H.; Lakdawala, H.; Paramesh, J.; Jung, B.; Zur, S.; Gordon, E. A 1.2 V 2.64 GS/s 8 bit 39 mW Skew-Tolerant Time-interleaved SAR ADC in 40 nm Digital LP CMOS for 60 GHz WLAN. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 1929–1939. [CrossRef]
18. Lin, C.; Wei, Y.; Lee, T. 27.7 A 10 b 2.6 GS/s time-interleaved SAR ADC with background timing-skew calibration. In Proceedings of the 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 31 January–4 February 2016; pp. 468–469.

19. Miki, T.; Ozeki, T.; Naka, J. A 2-GS/s 8-bit Time-Interleaved SAR ADC for Millimeter-Wave Pulsed Radar Baseband SoC. *IEEE J. Solid-State Circuits* **2017**, *52*, 2712–2720. [CrossRef]
20. Song, J.; Ragab, K.; Tang, X.; Sun, N. A 10-b 800-MS/s Time-Interleaved SAR ADC With Fast Variance-Based Timing-Skew Calibration. *IEEE J. Solid-State Circuits* **2017**, *52*, 2563–2575. [CrossRef]
21. Kang, H.; Hong, H.; Kim, W.; Ryu, S. A Time-Interleaved 12-b 270-MS/s SAR ADC With Virtual-Timing-Reference Timing-Skew Calibration Scheme. *IEEE J. Solid-State Circuits* **2018**, *53*, 2584–2594. [CrossRef]
22. Liu, J.; Chan, C.; Sin, S.; Seng-Pan, U.; Martins, R.P. Accuracy-Enhanced Variance-Based Time-Skew Calibration Using SAR as Window Detector. *IEEE Trans. Very Large Scale Integr. Syst.* **2019**, *27*, 481–485. [CrossRef]
23. Song, J.; Ragab, K.; Tang, X.; Sun, N. A 10-b 600-MS/s 2-Way Time-Interleaved SAR ADC With Mean Absolute Deviation-Based Background Timing-Skew Calibration. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 2876–2887. [CrossRef]
24. Kurosawa, N.; Kobayashi, H.; Maruyama, K.; Sugawara, H.; Kobayashi, K. Explicit analysis of channel mismatch effects in time-interleaved ADC systems. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **2001**, *48*, 261–271. [CrossRef]
25. Razavi, B. Design Considerations for Interleaved ADCs. *IEEE J. Solid-State Circuits* **2013**, *48*, 1806–1817. [CrossRef]
26. Stepanovic, D.; Nikolic, B. A 2.8 GS/s 44.6 mW Time-Interleaved ADC Achieving 50.9 dB SNDR and 3 dB Effective Resolution Bandwidth of 1.5 GHz in 65 nm CMOS. *IEEE J. Solid-State Circuits* **2013**, *48*, 971–982. [CrossRef]
27. Wei, H.; Zhang, P.; Sahoo, B.D.; Razavi, B. An 8 Bit 4 GS/s 120 mW CMOS ADC. *IEEE J. Solid-State Circuits* **2014**, *49*, 1751–1761. [CrossRef]
28. Sung, B.; Jo, D.; Jang, I.; Lee, D.; You, Y.; Lee, Y.; Park, H.; Ryu, S. 26.4 A 21fJ/conv-step 9 ENOB 1.6 GS/S 2× time-interleaved FATI SAR ADC with background offset and timing-skew calibration in 45 nm CMOS. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.
29. Wang, X.; Li, F.; Wang, Z. A novel autocorrelation-based timing mismatch C alibration strategy in Time-Interleaved ADCs. In Proceedings of the 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, Canada, 22–25 May 2016; pp. 1490–1493.
30. Song, J.; Sun, N. A 10-b 600-MS/s 2-way time-interleaved SAR ADC with mean absolute deviation based background timing-skew calibration. In Proceedings of the 2018 IEEE Custom Integrated Circuits Conference (CICC), 8–11 April 2018; pp. 1–4.
31. Hong, H.; Kim, W.; Kang, H.; Park, S.; Choi, M.; Park, H.; Ryu, S. A Decision-Error-Tolerant 45 nm CMOS 7b 1 GS/s Nonbinary 2b/Cycle SAR ADC. *IEEE J. Solid-State Circuits* **2015**, *50*, 543–555. [CrossRef]
32. Cao, Z.; Yan, S.; Li, Y. A 32 mW 1.25 GS/s 6b 2b/Step SAR ADC in 0.13$\ \mu$m CMOS. *IEEE J. Solid-State Circuits* **2009**, *44*, 862–873. [CrossRef]
33. Wei, H.; Chan, C.; Chio, U.; Sin, S.; Seng-Pan, U.; Martins, R.P.; Maloberti, F. An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC. *IEEE J. Solid-State Circuits* **2012**, *47*, 2763–2772. [CrossRef]
34. Sackinger, E.; Guggenbuhl, W. A versatile building block: The CMOS differential difference amplifier. *IEEE J. Solid-State Circuits* **1987**, *22*, 287–294. [CrossRef]
35. Kuttner, F. A 1.2 V 10 b 20 MSample/s non-binary successive approximation ADC in 0.13/spl mu/m CMOS. In Proceedings of the 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), San Francisco, CA, USA, 7 February 2002; Volume 171, pp. 176–177.
36. Razavi, B. The StrongARM Latch [A Circuit for All Seasons]. *IEEE Solid-State Circuits Mag.* **2015**, *7*, 12–17. [CrossRef]
37. Harpe, P.; Cantatore, E.; Roermund, A.V. A 10b/12b 40 kS/s SAR ADC With Data-Driven Noise Reduction Achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step. *IEEE J. Solid-State Circuits* **2013**, *48*, 3011–3018. [CrossRef]