Invitation to submit

Wide and Ultrawide Band Gap Semiconductors: Materials and Devices
Guest Editors: Prof. Dr. Wenrui Zhang and Prof. Dr. Wei Guo
Deadline: 15 April 2024

Recent Advances in Wide Bandgap Semiconductors
Guest Editors: Dr. Zhihua Dong, Dr. Kai Fu and Dr. Dawei Yan
Deadline: 31 May 2024

Nitride Semiconductor Devices and Applications
Guest Editors: Prof. Dr. Weijun Luo and Dr. Yangfeng Li
Deadline: 31 May 2024

Advanced Electronic Packaging Technology
Guest Editor: Prof. Dr. Daquan Yu
Deadline: 30 June 2024

Superconducting Machines Performance Optimization
Guest Editor: Dr. Dong Liu
Deadline: 15 July 2024

2D Materials-Based Devices and Applications
Guest Editors: Dr. Mingyuan Chen, Dr. Feng Wu, Dr. Qijun Zong, Dr. Jialiang Shen and Dr. Nurul Azam
Deadline: 20 August 2024

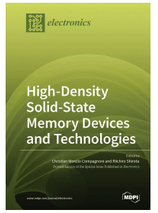
Wide Bandgap Semiconductor: From Epilayer to Devices
Guest Editors: Prof. Dr. Ray-Hua Horng, Dr. Giovanna Mura, Prof. Dr. Qixin Guo, Prof. Dr. Chin-Han(King) Chung and Dr. Ching-Lien Hsiao
Deadline: 31 August 2024

Feature Papers in Semiconductor Devices
Guest Editors: Dr. Frédérique Ducroquet, Prof. Dr. Yi Gu, Prof. Dr. Jae-Hyung Jang, Prof. Dr. Tao Wang and Dr. Hongtao Li
Deadline: 31 August 2024

Special Issue Book

Advanced CMOS Devices and Applications

High-Density Solid-State Memory Devices and Technologies



Design, Technologies and Applications of High Power Vacuum Electronic Devices from Microwave to THz Band

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Section Editor-in-Chief

Prof. Dr. Ray-Hua Horng

Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

Section Information

This section publishes original and significant contributions to the theory and performance of semiconductor devices and related materials, including devices, fabrication process, simulation, quantum devices, hybrid devices, flexible electronic devices, novel semiconductors, semiconductor material, and device physics. Reviews on these subjects are published and Special Issues dealing with specific topics are also published.

Topics of interest include but are not limited to the following:

- Semiconductor device applications
- Fabrication processing
- Simulation (theory)
- Quantum devices
- Hybrid electronic and semiconductor devices
- Semiconductor devices for energy
- Flexible devices
- Semiconductor material and device physics
- Novel semiconductor
- 2D materials for devices
- New technology for semiconductor devices
- Semiconductor optoelectronic and photonic devices and processing

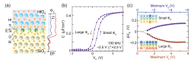
Section Semiconductor Devices

Selected Papers

DOI:10.3390/electronics13040726

Nonlinear Dynamics in HfO_2/SiO_2-Based Interface Dipole Modulation Field-Effect Transistors for Synaptic Applications

Author: Noriyuki Miyata

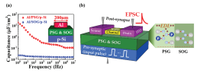


Abstract: In the pursuit of energy-efficient spiking neural network (SNN) hardware, synaptic devices leveraging emerging memory technologies hold significant promise. This study investigates the application of the recently proposed HfO_2/SiO_2-based interface dipole modulation (IDM) memory for synaptic spike timing-dependent plasticity (STDP) learning. Firstly, through pulse measurements of IDM metal–oxide–semiconductor (MOS) capacitors, we demonstrate that IDM exhibits an inherently nonlinear and near-symmetric response. Secondly, we discuss the drain current response of a field-effect transistor (FET) incorporating a multi-stack IDM structure, revealing its nonlinear and asymmetric pulse response, and suggest that the degree of the asymmetry depends on the modulation current ratio. Thirdly, to emulate synaptic STDP behavior, we implement double-pulse-controlled drain current modulation of IDMFET using a simple bipolar rectangular pulse. Additionally, we propose a double-pulse-controlled synaptic depression that is valuable for optimizing STDP-based unsupervised learning. Integrating the pulse response characteristics of IDMFETs into a two-layer SNN system for synaptic weight updates, we assess training and classification performance on handwritten digits. Our results demonstrate that IDMFET-based synaptic devices can achieve classification accuracy comparable to previously reported simulation-based results.

DOI:10.3390/electronics13040737

Enhancement of the Synaptic Performance of Phosphorus-Enriched, Electric Double-Layer, Thin-Film Transistors

Authors: Dong-Gyun Mah, Hamin Park and Won-Ju Cho

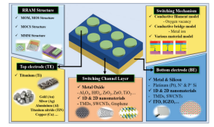


Abstract: The primary objective of neuromorphic electronic devices is the implementation of neural networks that replicate the memory and learning functions of biological synapses. To exploit the advantages of electrolyte gate synaptic transistors operating like biological synapses, we engineered electric double-layer transistors (EDLTs) using phosphorus-doped silicate glass (PSG). To investigate the effects of phosphorus on the EDL and synaptic behavior, undoped silicate spin-on-glass-based transistors were fabricated as a control group. Initially, we measured the frequency-dependent capacitance and double-sweep transfer curves for the metal-oxide-semiconductor (MOS) capacitors and MOS field-effect transistors. Subsequently, we analyzed the excitatory post-synaptic currents (EPSCs), including pre-synaptic single spikes, double spikes, and frequency variations. The capacitance and hysteresis window characteristics of the PSG for synaptic operations were verified. To assess the specific synaptic operational characteristics of PSG-EDLTs, we examined EPSCs based on the spike number and established synaptic weights in potentiation and depression (P/D) in relation to pre-synaptic variables. Normalizing the P/D results, we extracted the parameter values for the nonlinearity factor, asymmetric ratio, and dynamic range based on the pre-synaptic variables, revealing the trade-off relationships among them. Finally, based on artificial neural network simulations, we verified the high-recognition rate of PSG-EDLTs for handwritten digits. These results suggest that phosphorus-based EDLTs are beneficial for implementing high-performance artificial synaptic hardware.

DOI:10.3390/electronics12224650

Self-Rectifying Resistive Switching Memory Based on Molybdenum Disulfide for Reduction of Leakage Current in Synapse Arrays

Authors: DongJun Jang and Min-Woo Kwon



Abstract: Resistive random-access memory has emerged as a promising non-volatile memory technology, receiving substantial attention due to its potential for high operational performance, low power consumption, temperature robustness, and scalability. Two-dimensional nanostructured materials play a pivotal role in RRAM devices, offering enhanced electrical properties and physical attributes, which contribute to overall device improvement. In this study, the self-rectifying switching behavior in RRAM devices is analyzed based on molybdenum disulfide nanocomposites decorated with Pd on SiO_2/Si substrates. The switching layer integration of Pd and MoS_2 at the nanoscale effectively mitigates leakage currents decreasing from cross-talk in the RRAM array, eliminating the need for a separate selector device. The successful demonstration of the expected RRAM switching operation and low switching dispersion follows the application of a Pd nanoparticle embedding method. The switching channel layer is presented as an independent (Pd nanoparticle coating and MoS_2 nanosheet) nanocomposite. The switching layer length (4000 μm) and width (7000 μm) play an important role in a lateral-conductive-filament-based RRAM device. Through the bipolar switching behavior extraction of RRAM, the formation of the conductive bridges via electronic migration is explained. The fabricated Pd-MoS_2 synaptic RRAM device results in a high resistive current ratio for a forward/reverse current higher than 60 at a low resistance state and observes a memory on/off ratio of 103, exhibiting stable resistance switching behavior.

DOI:10.3390/electronics12183968

Soft Error Simulation of Near-Threshold SRAM Design for Nanosatellite Applications

Authors: Laurent Artola, Benjamin Ruard, Julien Forest and Guillaume Hubert

Abstract: This paper presents the benefit of the near-threshold design of random-access memory (SRAM) design to reduce software errors during very low-power operations in nanosatellites. The near-threshold design is based on an optimization of the use of the Schmitt trigger structure for a 45 nm technology. The results of the soft error susceptibility of the optimized design are compared to a standard 6T SRAM cell. These two designs are modeled and validated by comparing the results with experimental measurements of both static noise margin (SNM) and single event upset (SEU). The optimized circuit reduces the multiple upsets occurrence from 95% down to 14%. Based on the use of simulation tools, the paper demonstrates that the near-threshold design of SRAM is an excellent candidate for the radiation point of view for agile nanosatellites. The results computed for the near-threshold SRAM device demonstrate an improvement of a factor of up to 25 of the soft error rate (SER) in a GEO orbit.