Invitation to Submit

Automotive Cyber Security
Guest Editors: Dr. Ioanna Kantzavelou, Prof. Dr. Leandros Maglaras and Prof. Dr. Grammati Pantziou
Deadline: 15 June 2024

Machine Learning Techniques in Autonomous Driving
Guest Editor: Dr. Ali Riza Ekti
Deadline: 15 July 2024

MEPT (Maximum Efficiency Point Tracking) Techniques for Wireless Electric Vehicle Battery Charging
Guest Editors: Prof. Dr. Carlo Petrarca and Prof. Dr. Marco Balato
Deadline: 20 August 2024

Electro-Thermal Modelling, Status Estimation and Thermal Management of Electric Vehicles
Guest Editors: Dr. Yi Xie, Dr. Dan Dan and Dr. Jiahao Liu
Deadline: 15 September 2024

Autonomous and Connected Vehicles
Guest Editor:Dr. Piotr Borkowski
Deadline: 30 November 2024

SI Book

Artificial Intelligence and Ambient Intelligence
Guest Editors: **Matjaz Gams and Martin Gjoreski**

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Artificial Intelligence Circuits and Systems

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Department Theoretical Electrical Engineering, Technical University of Sofia, Bulgaria

Section Information

During the last decade, there has been increasing use of artificial intelligence tools in almost all areas of human activity. Artificial intelligence (AI) is not only at the heart of the current rise in information technology, but in all areas of life. In this regard, new algorithms and systems with the power of AI are being developed. Therefore, new hardware and computer platforms are needed to support emerging AI algorithms and applications, from cloud servers to circuits. Facing these new challenges and opportunities the Artificial Intelligence Circuits and Systems section has been established to facilitate state-of-the-art research, innovation, and development activities in the areas of artificial intelligence circuits and systems. It serves as the best platform for scholars, technological researchers, and industry professionals to publish their studies and further advance artificial intelligence technologies on circuits and systems.

The Artificial Intelligence Circuits and Systems section is focused on publications that are related to circuits and systems for artificial intelligence. The section covers topics of interest within hardware-based deep learning AI and algorithmic deep learning AI using machine learning. It is dedicated to the publication of articles not only from the listed areas but also from similar or related areas. We encourage the submission of original contributions derived from theoretical and/or application-oriented research studies.

Section Artificial Intelligence Circuits and Systems

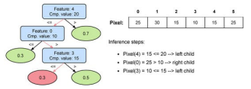
Selected Papers

DOI:10.3390/electronics10030314

FPGA Accelerator for Gradient Boosting Decision Trees

Authors: Adrián Alcolea and Javier Resano

Abstract: A decision tree is a well-known machine learning technique. Recently their popularity has increased due to the powerful Gradient Boosting ensemble method that allows to gradually increasing accuracy at the cost of executing a large number of decision trees. In this paper we present an accelerator designed to optimize the execution of these trees while reducing the energy consumption. We have implemented it in an FPGA for embedded systems, and we have tested it with a relevant case-study: pixel classification of hyperspectral images. In our experiments with different images our accelerator can process the hyperspectral images at the same speed at which they are generated by the hyperspectral sensors. Compared to a high-performance processor running optimized software, on average our design is twice as fast and consumes 72 times less energy. Compared to an embedded processor, it is 30 times faster and consumes 23 times less energy.



DOI:10.3390/electronics10020182

Design and Implementation of Deep Learning Based Contactless Authentication System Using Hand Gestures

Authors: Aveen Dayal, Naveen Paluru, Linga Reddy Cenkeramaddi, Soumya J. and Phaneendra K. Yalavarthy

Abstract: Hand gestures based sign language digits have several contactless applications. Applications include communication for impaired people, such as elderly and disabled people, health-care applications, automotive user interfaces, and security and surveillance. This work presents the design and implementation of a complete end-to-end deep learning based edge computing system that can verify a user contactlessly using 'authentication code'. The 'authentication code' is an 'n' digit numeric code and the digits are hand gestures of sign language digits. We propose a memory-efficient deep learning model to classify the hand gestures of the sign language digits. The proposed deep learning model is based on the bottleneck module which is inspired by the deep residual networks. The model achieves classification accuracy of 99.1% on the publicly available sign language digits dataset. The model is deployed on a Raspberry pi 4 Model B edge computing system to serve as an edge device for user verification. The edge computing system consists of two steps, it first takes input from the camera attached to it in real-time and stores it in the buffer. In the second step, the model classifies the digit with the inference rate of 280 ms, by taking the first image in the buffer as input.

DOI:10.3390/electronics10141715

Recurrent Neural Network for Human Activity Recognition in Embedded Systems Using PPG and Accelerometer Data

Authors: Michele Alessandrini, Giorgio Biagetti, Paolo Crippa, Laura Falaschetti and Claudio Turchetti

Abstract: Photoplethysmography (PPG) is a common and practical technique to detect human activity and other physiological parameters and is commonly implemented in wearable devices. However, the PPG signal is often severely corrupted by motion artifacts. The aim of this paper is to address the human activity recognition (HAR) task directly on the device, implementing a recurrent neural network (RNN) in a low cost, low power microcontroller, ensuring the required performance in terms of accuracy and low complexity. To reach this goal, (i) we first develop an RNN, which integrates PPG and tri-axial accelerometer data, where these data can be used to compensate motion artifacts in PPG in order to accurately detect human activity; (ii) then, we port the RNN to an embedded device, Cloud-JAM L4, based on an STM32 microcontroller, optimizing it to maintain an accuracy of over 95% while requiring modest computational power and memory resources. The experimental results show that such a system can be effectively implemented on a constrained-resource system, allowing the design of a fully autonomous wearable embedded system for human activity recognition and logging.

DOI:10.3390/electronics10182272

An Efficient FPGA-Based Convolutional Neural Network for Classification: Ad-MobileNet

Authors: Safa Bouguezzi, Hana Ben Fredj, Tarek Belabed, Carlos Valderrama, Hassene Faiedh and Chokri Souani

Abstract: Convolutional Neural Networks (CNN) continue to dominate research in the area of hardware acceleration using Field Programmable Gate Arrays (FPGA), proving its effectiveness in a variety of computer vision applications such as object segmentation, image classification, face detection, and traffic signs recognition, among others. However, there are numerous constraints for deploying CNNs on FPGA, including limited on-chip memory, CNN size, and configuration parameters. This paper introduces Ad-MobileNet, an advanced CNN model inspired by the baseline MobileNet model. The proposed model uses an Ad-depth engine, which is an improved version of the depth-wise separable convolution unit. Moreover, we propose an FPGA-based implementation model that supports the Mish, TanhExp, and ReLU activation functions. The experimental results using the CIFAR-10 dataset show that our Ad-MobileNet has a classification accuracy of 88.76% while requiring little computational hardware resources. Compared to state-of-the-art methods, our proposed method has a fairly high recognition rate while using fewer computational hardware resources. Indeed, the proposed model helps to reduce hardware resources by more than 41% compared to that of the baseline model.