Invitation to Submit

Memristors beyond the Limitations: Novel Methods and Materials
Guest Editor: Niloufar Raeis-Hosseini
Deadline: 15 June 2024

Embedded FET for Application as a Biosensor
Guest Editors: Agnes Purwidyantri and Inmaculada Ortiz-Gómez
Deadline: 16 August 2024

Advanced Materials for Thermal Management of Electronics
Guest Editors: Hafiz Muhammad Ali, Hongwei Wu and Mehdi Khiadani
Deadline: 16 August 2024

Advanced Materials for Intelligent Electronics
Guest Editor: Hyojung Kim
Deadline: 15 October 2024

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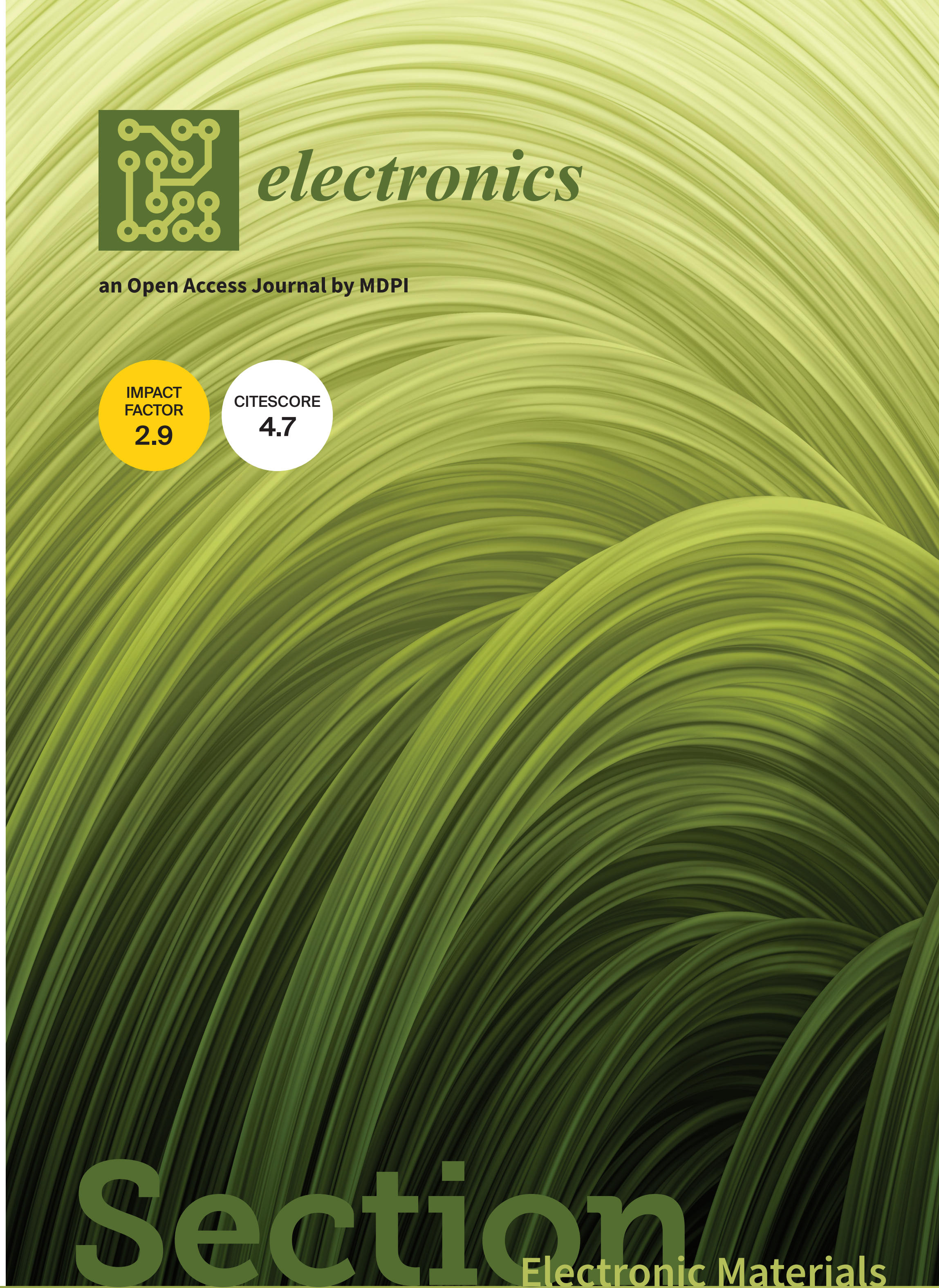

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Section Information

The Section “Electronic Materials” reports on the science, technology, and applications of electronic materials which are used in electrical industries, electronics and microelectronics, and the substances used in construction of integrated circuits, circuit boards, packaging materials, communication cables, optical fibers, displays, and various controlling and monitoring devices.

The main topics of this section include but are not limited to the following:

- Electronic materials science and technology
- Energy storage and conversion materials
- Nanoscale science and technology
- Organic materials and thin-film technology
- Oxide semiconductors and dielectrics
- Wide bandgap semiconductors

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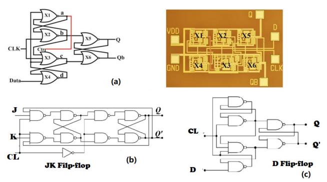
Section Electronic Materials

Selected Papers

DOI:10.3390/electronics11060960

Strategies for Applications of Oxide-Based Thin Film Transistors

Authors: Lirong Zhang, Huaming Yu, Wenping Xiao, Chun Liu, Junrong Chen, Manlan Guo, Huayu Gao, Baiquan Liu and Weijing Wu

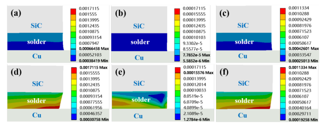


Abstract: Due to the untiring efforts of scientists and researchers on oxide semiconductor materials, processes, and devices, the applications for oxide-based thin film transistors (TFTs) have been researched and promoted on a large scale. With the advantages of relatively high carrier mobility, low off-current, good process compatibility, optical transparency, low cost, and especially flexibility, oxide-based TFTs have already been adapted for not only displays (e.g., liquid crystal display (LCD), organic light emitting diode (OLED), micro-light-emitting diode (Micro-LED), virtual reality/augmented reality (VR/AR) and electronic paper displays (EPD)) but also large-area electronics, analog circuits, and digital circuits. Furthermore, as the requirement of TFT technology increases, low temperature poly-silicon and oxide (LTPO) TFTs, which combine p-type LTPS and n-type oxide TFT on the same substrate, have drawn further interest for realizing the hybrid complementary metal oxide semiconductor (CMOS) circuit. This invited review provides the current progress on applications of oxide-based TFTs. Typical device configurations of TFTs are first described. Then, the strategies to apply oxide-based TFTs for improving the display quality with different compensation technologies and obtaining higher performance integrated circuits are highlighted. Finally, an outlook for the future development of oxide-based TFTs is given.

DOI:10.3390/electronics11010062

Study of Thermal Stress Fluctuations at the Die-Attach Solder Interface Using the Finite Element Method

Authors: Luchun Yan, Jiawen Yao, Yu Dai, Shanshan Zhang, Wangmin Bai, Kewei Gao, Huisheng Yang and Yanbin Wang

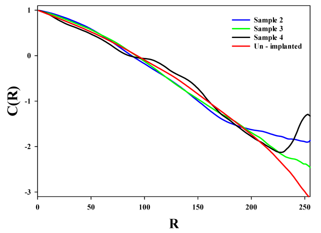


Abstract: Solder joints in electronic packages are frequently exposed to thermal cycling in both real-life applications and accelerated thermal cycling tests. Cyclic temperature leads the solder joints to be subjected to cyclic mechanical loading and often accelerates the cracking failure of the solder joints. The cause of stress generated in thermal cycling is usually attributed to the coefficients of thermal expansion (CTE) mismatch of the assembly materials. In a die-attach structure consisting of multiple layers of materials, the effect of their CTE mismatch on the thermal stress at a critical location can be very complex. In this study, we investigated the influence of different materials in a die-attach structure on the stress at the chip–solder interface with the finite element method. The die-attach structure included a SiC chip, a SAC solder layer and a DBC substrate. Three models covering different modeling scopes (i.e., model I, chip–solder layer; model II, chip–solder layer and copper layer; and model III, chip–solder layer and DBC substrate) were developed. The 25–150 °C cyclic temperature loading was applied to the die-attach structure, and the change of stress at the chip–solder interface was calculated. The results of model I showed that the chip–solder CTE mismatch, as the only stress source, led to a periodic and monotonic stress change in the temperature cycling. Compared to the stress curve of model I, an extra stress recovery peak appeared in both model II and model III during the ramp-up of temperature. It was demonstrated that the CTE mismatch between the solder and copper layer (or DBC substrate) not only affected the maximum stress at the chip–solder interface, but also caused the stress recovery peak. Thus, the combined effect of assembly materials in the die-attach structure should be considered when exploring the joint thermal stresses.

DOI:10.3390/electronics10232941

Microstructural and Energy-Dispersive X-ray Analyses on Argon Ion Implantations in Tantalum Thin Films for Microelectronic Substrates

Authors: PAmir Hoshang Ramezani, Siamak Hoseinzadeh, Zhaleh Ebrahiminejad, Milad Sangashekan and Saim Memon

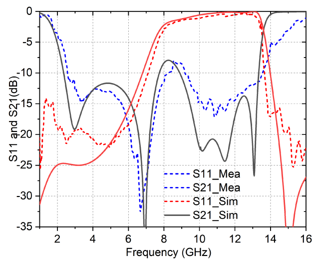


Abstract: In the present study, the microstructural and statistical properties of unimplanted in comparison to argon ion-implanted tantalum-based thin film surface structures are investigated for potential application in microelectronic thin film substrates. In the study, the argon ions were implanted at the energy of 30 keV and the doses of 1 × 1017, 3 × 1017, and 7 × 1017 (ion/cm2) at an ambient temperature. Two primary goals have been pursued in this study. First, by using atomic force microscopy (AFM) analysis, the roughness of samples, before and after implantation, has been studied. The corrosion apparatus wear has been used to compare resistance against tantalum corrosion for all samples. The results show an increase in resistance against tantalum corrosion after the argon ion implantation process. After the corrosion test, scanning electron microscopy (SEM) analysis was applied to study the sample morphology. The elemental composition of the samples was characterized by using energy-dispersive X-ray (EDX) analysis. Second, the statisticalcharacteristics of both unimplanted and implanted samples, using the monofractal analysis with correlation function and correlation length of samples, were studied. The results show, however, that all samples are correlated and that the variation of ion doses has a negligible impact on the values of correlation lengths. Moreover, the study of height distribution and higher-order moments show the deviation from Gaussian distribution. The calculations of the roughness exponent and fractal dimension indicates that the implanted samples are the self-affine fractal surfaces.

DOI:10.3390/electronics11091418

Broadband-Transmissive, Frequency-Selective Rasorber Design Using Characteristic Mode Analysis

Authors: Jie Xiong, Baoping Yang, Yanjie Wu, Xiongwei Zeng, Qiuyu Li, Rongxin Tang and Hai Lin



Abstract: This article designs a frequency-selective rasorber (FSR) with a broadband transmission window. It is synthesized by a broadband absorber and a frequency-selective surface (FSS). The resistive layer achieves broadband absorption by introducing a tortuous Jerusalem cross load with lumped resistors, and the lossless FSS adopts a three-layer metal structure to realize the broadband transmission window. The absorption mechanism of the resistive layer is analyzed using the theory of characteristic mode. The position of the resistor is determined according to the analysis of mode current distribution and parameter optimization. Prototypes of the structure were fabricated and measured, and the simulation results show that the 1 dB transmission window and the absorption band with |S11|< −1 dB are 36.4% and 97%, respectively. Therefore, the designed FSR has potential application prospects in electromagnetic stealth technology and radar cross-section reduction.