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Common Grounded H-Type Bidirectional DC-DC Converter with a Wide Voltage Conversion Ratio for a Hybrid Energy Storage System

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Abstract: Hybrid energy storage systems (HESS) play an important role in maintaining the power balance of a direct current (DC) micro-grid. A HESS is mainly composed of high power density super-capacitors (SCs) and high energy density batteries. According to the operational requirements of an SC, a bidirectional DC-DC converter with the characteristics of a good dynamic response and a wide voltage conversion ratio is needed to interface the SC and a high-voltage DC bus. In this paper, a novel common grounded H-type bidirectional converter characterized by a good dynamic response, a low inductor current ripple, and a wide voltage conversion ratio is proposed. In addition, it can avoid the narrow pulse of pulse width modulation (PWM) voltage waveforms when a high voltage conversion ratio is achieved. All of these features are beneficial to the operation of the SC connected to a DC bus. The operating principle and characteristics of the proposed converter are presented in this paper. A 320 W prototype with a wide voltage conversion ranging from 3.3 to 8 in step-up mode and 1/8 to 1/3 in step-down mode has been constructed to validate the feasibility and effectiveness of the proposed converter.

Keywords: H-type bidirectional DC-DC converter; good dynamic response; hybrid energy storage system; wide voltage conversion ratio

1. Introduction

With the high penetration of direct current (DC) energy sources, storage, and loads, DC micro-grids are becoming more prevalent due to a lower number of power converters compared with an alternating current (AC) micro-grid [1–3]. Because of the intermittent nature of renewable energy sources and unpredictable load fluctuations in DC micro-grids, the problem of power imbalance may appear and affect the operation of DC micro-grids. Therefore, energy storage systems (ESs) are always installed to maintain the power balance of the DC micro-grid [4,5]. ESs can be divided into a power density type and an energy density type based on their characteristics [6,7]. Unfortunately, there is no single type of ES that fulfills all expected features [8]. Therefore, it is an economic and effective solution to use a hybrid energy storage system (HESS) composed by different characteristics of ESs [9–11]. Generally, a HESS is mainly composed of high power density super-capacitors (SCs) and high energy density batteries. It is desirable to balance the steady-state power imbalance by the batteries and compensate for the transient power imbalance by an SC with fast dynamics [12–14]. As a result, the degradation impact on the batteries caused by sudden load changes can be greatly reduced, and the dynamic response of the whole DC micro-grid can also be improved [15,16].

As mentioned above, high power density SCs play an important role in a HESS. However, the output voltage of an SC is relatively low and changes widely. In order to connect the SC to a high voltage level DC bus and to achieve a bidirectional power flow for the SC, a wide voltage conversion

ratio bidirectional DC-DC converter is needed. Considering that the SC needs to compensate for transient power, the bidirectional DC-DC converter needs to have the feature of an outstanding dynamic response.

Many isolated and non-isolated bidirectional converters present in the literature can achieve a wide voltage conversion ratio. Due to using a high-frequency transformer, the isolated bidirectional converters can obtain a wide voltage conversion ratio in the step-up and step-down modes by adjusting the turns ratio of the transformer. Because of the use of a transformer and a high number of switching devices, the cost and switching losses of these converters will be increased and the control schemes will be more complicated [17–20]. From the viewpoint of system cost-saving and improving system efficiency, a non-isolated DC-DC converter is more suitable for HESS applications [21,22].

Research on non-isolated converters is focused on coupled-inductor, switched-capacitor, switched-inductor, voltage-multiplier, and multi-stage/-level techniques [23]. The coupled-inductor-based converter in [24] can have a higher voltage gain, and also reduce the reverse recovery losses of the diodes. However, the current ripple of the low-voltage side is relatively large, which may damage the low-voltage side source. With a simple structure, switched-capacitor converters are easy to expand. At the same time, the control methods of these converters are also simple. In different switching states, the energy of the capacitors in these converters can be delivered through different paths, making it easier for these converters to achieve a high voltage gain [25–28]. Switched-inductor converters can also achieve a wide voltage conversion ratio while avoiding extreme duty cycles. At the same time, the voltage stress of the power semiconductors in these converters can be reduced. However, more inductors affect the power density of these converters [29,30]. In [31], a new non-isolated single capacitor bidirectional DC-DC converter with a simple structure and a wide voltage conversion ratio is presented. However, the voltage stress of the power semiconductor is relatively high. A common ground switched-quasi-Z-source bidirectional DC-DC converter is presented in [32]. The advantages of this converter are a wide voltage conversion ratio and a lower voltage stress across the power switches. However, with the low voltage level (240 V) and low rated power (300 W), the volume of the capacitors (470/520 uF) and inductors (434/600 uH) is high, which results in a lower power density for this converter.

This paper presents a novel common grounded H-type bidirectional DC-DC converter, which not only achieves a wide voltage conversion ratio, but also has the advantages of a low inductor current ripple and a good dynamic response. In addition, a clamp capacitor is used in this converter to keep all of the power switches turned on and off only once during each switching period, aiming at reducing switching losses and avoiding narrow pulses of the pulse width modulation (PWM) voltage waveform at high voltage gain. These features are beneficial to improve the efficiency and reliability of this converter and its suitability for HESS applications.

As shown in Figure 1, a HESS contains a battery and an SC. The SC outputs are varying low dc voltages (25–60 V) which cannot be used directly, and must be regulated via the bidirectional converter. The proposed converter can fulfill the task well. The remainder of this paper is structured as follows. In Section 2, the novel H-type bidirectional DC-DC converter topology and operating principles are proposed. In Section 3, the characteristics of the proposed converter are analyzed and its small signal model is established. Experimental results for the proposed converter are provided in Section 4. The conclusion of this paper is introduced in Section 5.

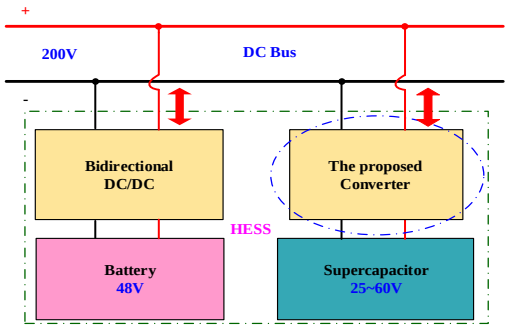


Figure 1. Configuration of the hybrid energy storage system (HESS). DC: direct current.

2. Operating Principles of the Proposed Converter

2.1. Configuration of the Proposed Converter

The configuration of the proposed converter is depicted in Figure 2. This converter is composed of a capacitor-clamped H-type structure (Q_1–Q_4 and C_1), an inductor, a power switch Q_5, and two filter capacitors C_{high} and C_{low}. To simplify the analysis, it is assumed that the capacitors and inductor are large enough and all of the power semiconductors are ideal. In order to protect the SC, the proposed converter operates in the input current continuous model (CCM).

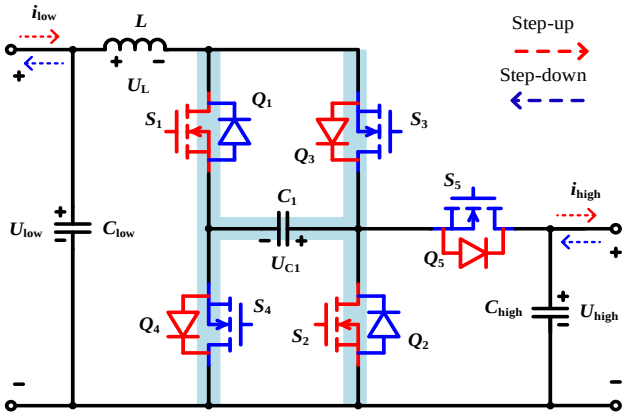


Figure 2. Configuration of the proposed converter.

2.2. Operating Principles

2.2.1. Step-Up Mode of the Proposed Converter

As shown in Figure 2, U_{low} can be stepped-up to U_{high} by controlling the power semiconductors Q_1, and Q_2. The relationship between d_1 and d_2 can be written as $d_1 = d_2 = d_{Boost}$, where d_1 and d_2 are the duty cycles of Q_1 and Q_2, respectively. The phase difference between the gate-driving signals S_1 and S_2 is 180°. During one switching period, the converter has three switching states, and their sequence is "10-00-01-00-10". Figure 3 shows the energy flow paths and Figure 4 shows the typical waveforms. Due to using the clamp capacitor C_1, all of the power semiconductors turn on and off only once during each switching period.

When S_1S_2 = 10: As shown in Figure 3a, where switch S_1 is *ON* and S_2 is *OFF*. The anti-parallel diodes of Q_4 and Q_5 are forward biased, while the anti-parallel diode of Q_3 is reverse biased. The inductor L is charged from the input source. Current i_L rises linearly. The load is supplied by C_1 and C_{high}. Clamp capacitor C_1 maintains the forward bias of the anti-parallel diodes of Q_5.

When S_1S_2 = 00: As shown in Figure 3b, both switches S_1 and S_2 are *OFF*. The anti-parallel diodes of Q_3, Q_4, and Q_5 are forward biased. Capacitors C_1 and C_{high} are charged from L. The load is supplied by L. There is no energy exchange between capacitors C_1 and C_{high}.

When S_1S_2 = 01: As shown in Figure 3c, where switch S_1 is *OFF* and S_2 is *ON*. The anti-parallel diode of Q_3 is forward biased, while the anti-parallel diodes of Q_4 and Q_5 are reverse biased. Inductor L is charged from the input source. Current i_L rises linearly. The load is supplied by output capacitor C_{high}. In this case, the voltage of capacitor C_1 remains steady.

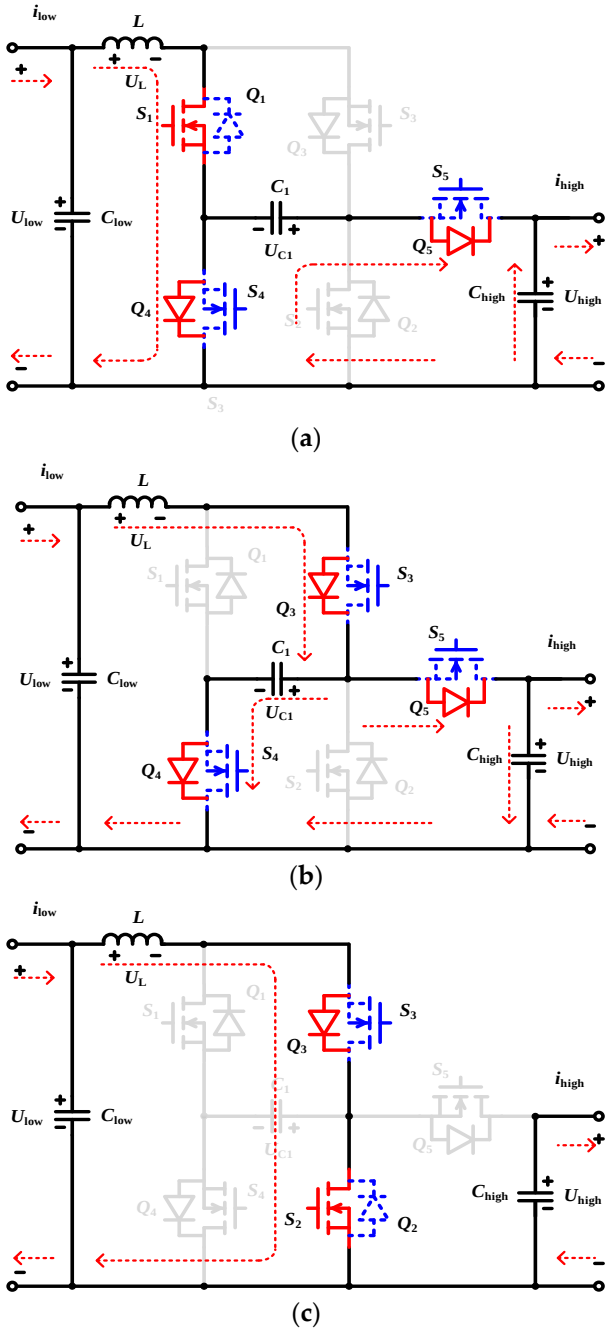


Figure 3. Energy flow paths of the proposed converter in the step-up mode; (**a**) S_1S_2 = 10; (**b**) S_1S_2 = 00; (**c**) S_1S_2 = 01.

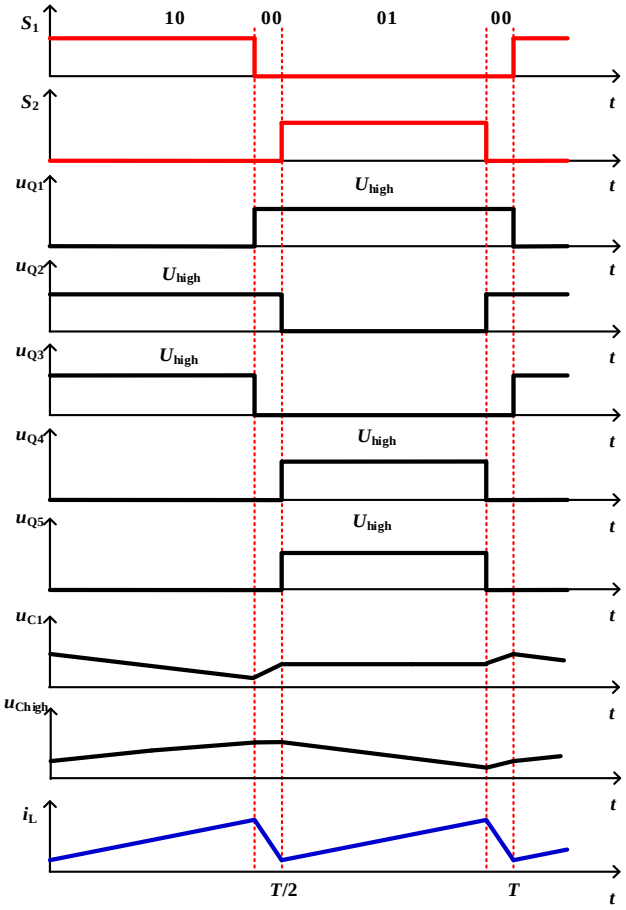


Figure 4. Typical waveforms of the proposed converter in the step-up mode.

2.2.2. Step-Down Mode of the Proposed Converter

As shown in Figure 2, U_{high} can be stepped down to U_{low} by controlling the power semiconductors Q_3, Q_4, and Q_5. The relationship between d_3, d_4, and d_5 can be written as $d_3 = d_4 = d_5 = d_{Buck}$, where d_3, d_4, and d_5 are the duty cycles of Q_3, Q_4, and Q_5, respectively. The phase difference between the gate-driving signals S_3 and S_4 is 180°. The gate-driving signal $S_5 = S_4$. During one switching period, the converter has three switching states, and their sequence is "111-100-111-011-111". Figure 5 shows the energy flow paths and Figure 6 shows the typical waveforms. During each switching period, all of the power semiconductors also turn on and off once.

When $S_3S_4S_5$ = 111: The switching state is shown in Figure 5a, where switches S_3, S_4, and S_5 are *ON*. The anti-parallel diodes of Q_1 and Q_2 are forward biased. The high-voltage side U_{high} and capacitor C_1 charge the inductor L, and simultaneously provide energy to the load in the low-voltage side. The current i_L rises linearly.

When $S_3S_4S_5$ = 100: The switching state is shown in Figure 5b, where switch S_3 is *ON* and switches S_4 and S_5 are *OFF*. The anti-parallel diode of Q_2 is forward biased, while the anti-parallel diode of Q_1 is reverse biased. Inductor L provides energy to the load in the low-voltage side. The current i_L decreases linearly.

When $S_3S_4S_5$ = 011: The switching state is shown in Figure 5c, where switches S_4 and S_5 are *ON* and S_3 is *OFF*. The anti-parallel diode of Q_1 is forward biased, while the anti-parallel diode of Q_2 is reverse biased. Inductor L provides energy to the load in the low-voltage side. The current i_L decreases linearly. Capacitor C_1 is charged by the high-voltage side U_{high}. The clamp capacitor C_1 maintains the power switch Q_5 *ON*.

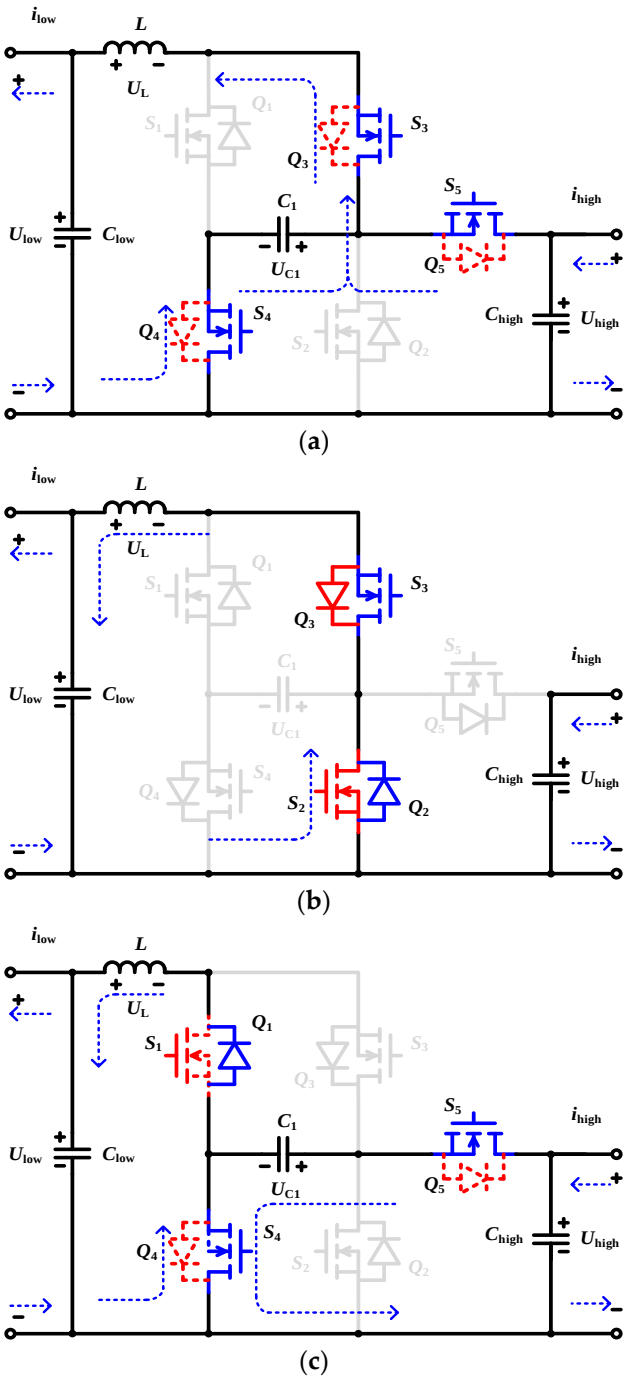


Figure 5. Energy flow paths of the proposed converter in the step-down mode; (**a**) $S_3S_4S_5$ = 111; (**b**) $S_3S_4S_5$ = 100; (**c**) $S_3S_4S_5$ = 011.

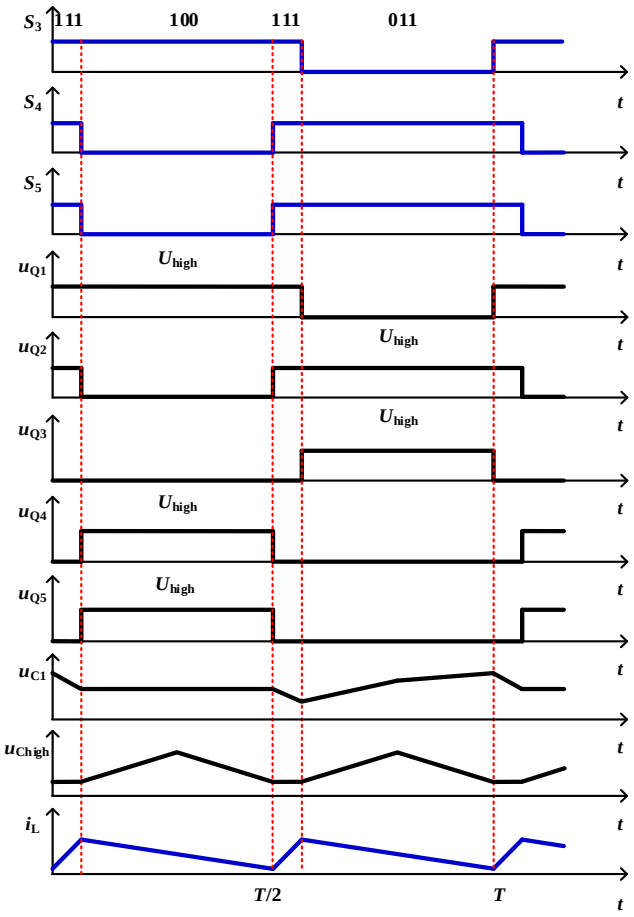


Figure 6. Typical waveforms of the proposed converter in the step-down mode.

2.2.3. Synchronous Rectification Mode of the Proposed Converter

The on-state resistance of the power switch is lower than its corresponding anti-parallel diode. As mentioned above, current flow into the corresponding anti-parallel diodes of the slave power switches will result in higher conduction losses and lower efficiency. In order to improve the efficiency, the proposed converter uses synchronous rectifier technology [33,34].

The synchronous rectification operation principle of the proposed converter is shown in Figure 7. Figure 7a shows the gate signals of S_1–S_5 in step-up mode and Figure 7b shows the gate signals of S_1–S_5 in step-down mode. In step-up mode, the current has to fully flow into the corresponding anti-parallel diodes of the slave power switches Q_3, Q_4, and Q_5 at the dead time t_d. When the slave power switches are *ON*, the current almost flows into the MOSFETS due to their lower on-resistance as shown in Figure 7c. In step-down mode, the current flow path is the same as with the step-up mode as shown in Figure 7d. The only difference is that the slave power switches are Q_1 and Q_2.

When the current flows into the corresponding anti-parallel diodes of the slave power switches at dead time, the forward voltage drops of the anti-parallel diodes are close to zero. As a result, the slave active power switches turn on and turn off with zero voltage. The turn on/off losses of the slave active power switches will not be increased and the efficiency of the converter can be improved.

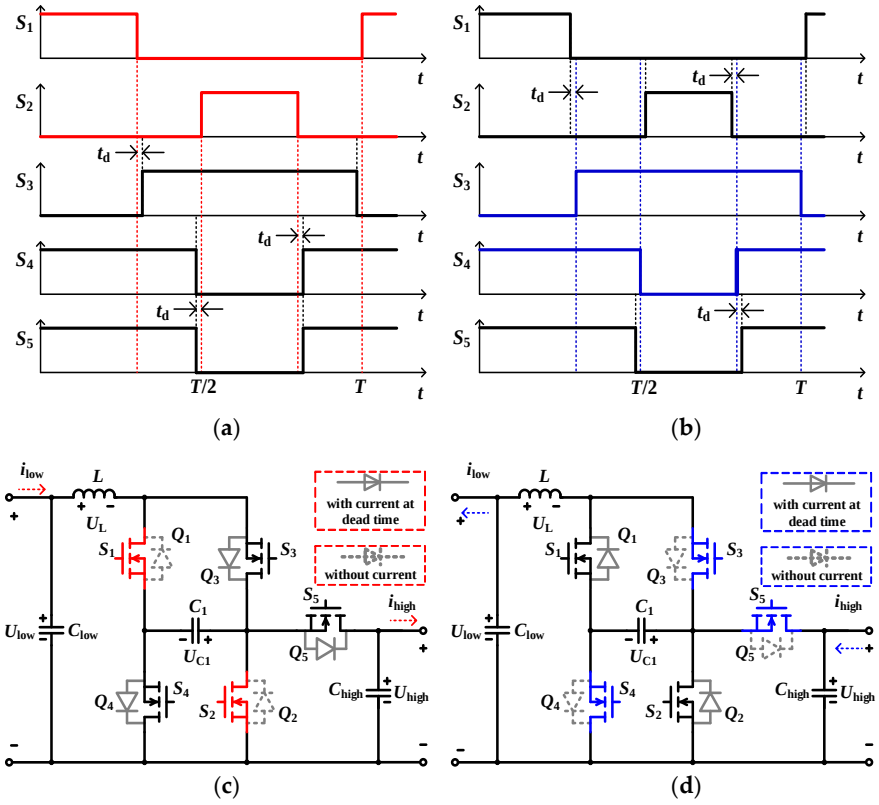


Figure 7. Synchronous rectification operation principle of the proposed converter; (**a**) Gate signals and dead time in step-up mode; (**b**) Gate signals and dead time in step-down mode; (**c**) Current flow path in step-up mode; (**d**) Current flow path in step-down mode.

2.3. Control Strategy for Bidirectional Power Flow

For a HESS, the SC interface converter should be able to respond to fast bidirectional power fluctuations immediately. Therefore, a virtual capacitor droop (VCD) control is adopted for this converter. At the same time, the battery interface converter uses a virtual resistance droop (VRD) control to make the battery provide total power at steady state. Due to using the VCD and VCR control, the HESS can adapt to the distributed nature of the DC micro-grid and increase system reliability and scalability [35,36]. The specific control strategy is shown in Figure 8. As shown in Figure 8, the voltage controller is used to follow the reference voltage U_{ref}. The voltage U_{high} and the currents $i_{high\text{-}sc}$ and $i_{high\text{-}bat}$ are obtained by the sensor samplings. $i_{high\text{-}sc}$ refers to the output current of the SC interface converter and $i_{high\text{-}bat}$ refers to the output current of the battery interface converter.

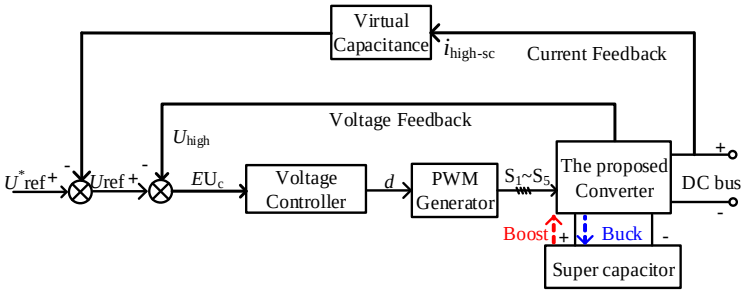
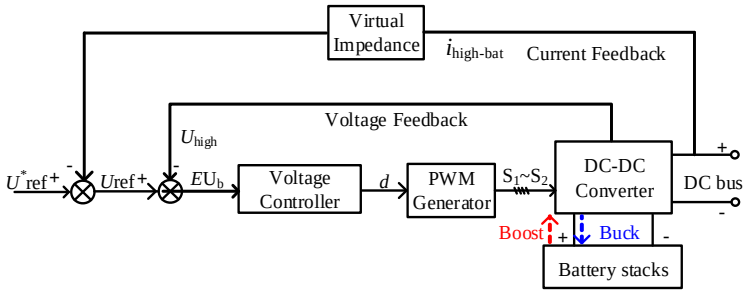


Figure 8. *Cont.*



(**b**)

Figure 8. Control strategy for bidirectional power flow; (**a**) virtual capacitor droop (VCD) control; (**b**) virtual resistance droop (VRD) control.

The operation modes of the proposed converter switch between the step-down and step-up modes according to the necessary conditions of a general load. The current relationship at the DC bus is expressed as

$$i_{\mathrm{HESS}} = i_{\mathrm{high-sc}} + i_{\mathrm{high-bat}} \tag{1}$$

where i_{HESS} is the equivalent load current of the HESS and can be either positive or negative. The output voltage–current (V–I) relationship of the battery interface converter under the VRD control and that of the SC interface converter under the VCD control are given by

$$\begin{cases} U_{\mathrm{high}} = U*_{\mathrm{ref}} - R_{\mathrm{vb}} i_{\mathrm{high-bat}} \\ U_{\mathrm{high}} = U*_{\mathrm{ref}} - \frac{1}{sC_{\mathrm{vc}}} i_{\mathrm{high-sc}} \end{cases} \tag{2}$$

where R_{vb} is the virtual resistance and C_{vc} is the virtual capacitance. Based on (1) and (2), the current-sharing relationship between battery and SC is derived as

$$\begin{cases} i_{\mathrm{high-bat}} = \frac{1}{sR_{\mathrm{vb}}C_{\mathrm{vc}}+1} i_{\mathrm{HESS}} \\ i_{\mathrm{high-sc}} = \frac{sR_{\mathrm{vb}}C_{\mathrm{vc}}}{sR_{\mathrm{vb}}C_{\mathrm{vc}}+1} i_{\mathrm{HESS}} \end{cases}. \tag{3}$$

3. Characteristics of the Proposed Converter

3.1. Wide Voltage Conversion Ratio

3.1.1. Voltage Conversion Ratio in Step-Up Mode

For the proposed converter shown in Figure 2, the voltage conversion ratio can be derived from the volt-sec balance of the inductor L. According to Figure 3a, Q_4 and Q_5 are ON, so that the voltages of C_1 and C_{high} are equal. In the low-voltage side current continuous model, the equations can be obtained as follows:

$$\begin{cases} 2U_{\mathrm{low}} d_{\mathrm{Boost}} + (U_{\mathrm{low}} - U_{\mathrm{high}})(1 - 2d_{\mathrm{Boost}}) = 0 \\ U_{\mathrm{C1}} = U_{\mathrm{high}} \end{cases} \tag{4}$$

where U_{C1} is the voltage over C_1. By simplifying (1), the following equation can be derived:

$$\begin{cases} U_{\mathrm{high}} = \frac{1}{1-2d_{\mathrm{Boost}}} U_{\mathrm{low}} \\ U_{\mathrm{C1}} = U_{\mathrm{high}} \end{cases}. \tag{5}$$

The voltage conversion ratio M_{Boost} of the proposed converter is

$$M_{\text{Boost}} = \frac{1}{1 - 2d_{\text{Boost}}} \tag{6}$$

where $0 < d_{\text{Boost}} < 0.5$.

3.1.2. Voltage Conversion Ratio in Step-Down Mode

According to Figure 5c, the power switches Q_4 and Q_5 are *ON*, so that the voltages of C_1 and C_{high} are equal. By applying the volt-second balance principle on L, the voltage conversion ratio in CCM can be obtained as

$$\begin{cases} (U_{\text{low}} - U_{\text{high}})(2d_{\text{Buck}} - 1) + 2U_{\text{low}}(1 - d_{\text{Buck}}) = 0 \\ U_{\text{C1}} = U_{\text{high}} \end{cases}. \tag{7}$$

By simplifying (7), the following equation can be derived:

$$\begin{cases} U_{\text{low}} = (2d_{\text{Buck}} - 1)U_{\text{high}} \\ U_{\text{C1}} = U_{\text{high}} \end{cases} \tag{8}$$

The voltage conversion ratio M_{Buck} in step-down mode is

$$M_{\text{Buck}} = 2d_{\text{Buck}} - 1 \tag{9}$$

where $0.5 < d_{\text{Buck}} < 1$.

Under the same voltage conversion ratio, 0 shows the comparison between the proposed and the traditional two-level bidirectional converters. According to Figure 9, when the voltage conversion ratio is 8 in the step-up mode, the duty cycles of the proposed and the traditional converters are 0.4375 and 0.875, respectively; in step-down mode, when the voltage conversion ratio is 0.125, the duty cycles of the proposed and the traditional converters are 0.5625 and 0.125, respectively. Compared with the traditional converter, the proposed one can avoid the extreme duty cycle while achieving a high voltage conversion ratio. What is more, the higher the voltage conversion ratio, the closer the duty cycle is to 0.5. When the duty cycle approaches 0.5, the time used to maintain the *ON* and *OFF* state for all power semiconductors is nearly equal in each period, which is beneficial to avoid the narrow pulse of PWM voltage waveforms while the high voltage conversion ratio is achieved.

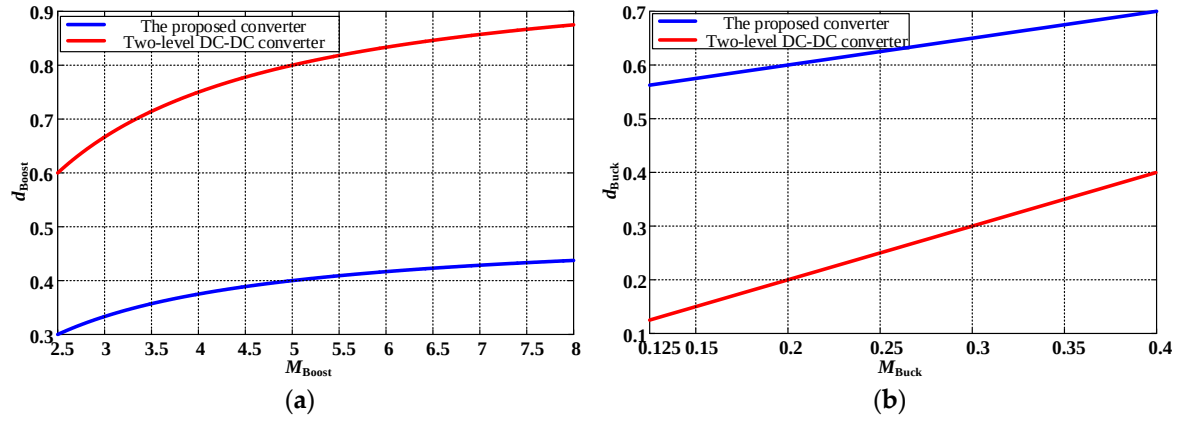


Figure 9. Comparisons of duty cycle against voltage gain; (**a**) Step-up mode; (**b**) Step-down mode.

3.2. Low Inductor Current Ripple

3.2.1. The Average Inductor Current and Inductor Current Ripple in Step-Up Mode

The average inductor current can be derived from the ampere-second balance of the capacitors C_1 and C_{high} in CCM.

$$\begin{cases} d_{\text{Boost}} I_{\text{c1a}} + (1 - 2d_{\text{Boost}}) I_{\text{c1b}} = 0 \\ -d_{\text{Boost}}(2I_{\text{high}} + I_{\text{c1a}}) + (1 - 2d_{\text{Boost}})(I_{\text{L}} - I_{\text{high}} - I_{\text{c1b}}) = 0 \end{cases} \tag{10}$$

where I_{C1a} and I_{C1b} are the average currents across C_1 in state 10 and 00, respectively. It follows from (10) that the average inductor current I_{L} can be obtained as follows:

$$I_{\text{L}} = \frac{1}{1 - 2d_{\text{Boost}}} \times I_{\text{high}}. \tag{11}$$

In the state 10, the inductor current increases linearly, and (12) can be obtained as

$$i_{\text{L}(d_{\text{Boost}}T)} = i_{\text{L}(0)} + \frac{1}{L}\int_0^{d_{\text{Boost}}T} U_{\text{low}} dt \Rightarrow \Delta i_{\text{L}} = \frac{1}{L}\int_0^{d_{\text{Boost}}T} U_{\text{low}} dt = \frac{d_{\text{Boost}} \times U_{\text{low}}}{Lf} \tag{12}$$

where f is the switching frequency and Δi_{L} is the inductor current ripple. It follows from (11) and (12) that the current ripple ratio r_{Boost} of the inductor can be obtained as

$$r_{\text{Boost}} = \frac{\Delta i_{\text{L}}}{I_{\text{L}}} = \frac{d_{\text{Boost}}(1 - 2d_{\text{Boost}})^2 \times R_{\text{high}}}{Lf} \tag{13}$$

where R_{high} is the equivalent load of the high-voltage side.

3.2.2. The Average Inductor Current and Inductor Current Ripple in Step-Down Mode

The average inductor current I_{L} can be obtained as follows:

$$I_{\text{L}} = I_{\text{low}}. \tag{14}$$

In the state 100, the inductor current decreases linearly, and (15) can be obtained as

$$i_{\text{L}(d_{\text{Buck}}T)} = i_{\text{L}(0)} + \frac{1}{L}\int_{(d_{\text{Buck}}-0.5)T}^{0.5T} U_{\text{low}} dt \Rightarrow \Delta i_{\text{L}} = \frac{1}{L}\int_{(d_{\text{Buck}}-0.5)T}^{0.5T} U_{\text{low}} dt = \frac{(1 - d_{\text{Buck}}) \times U_{\text{low}}}{Lf}. \tag{15}$$

It follows from (14) and (15) that the current ripple ratio r_{Buck} of the inductor can be obtained as follows:

$$r_{\text{Buck}} = \frac{\Delta i_{\text{L}}}{I_{\text{L}}} = \frac{(1 - d_{\text{Buck}}) \times R_{\text{low}}}{Lf} \tag{16}$$

where R_{low} is the equivalent load of the low-voltage side.

The inductor current ripple ratios of a traditional two-level bidirectional converter are:

$$\begin{cases} r\prime_{\text{Boost}} = \frac{d\prime_{\text{Boost}}(1 - d\prime_{\text{Boost}})^2 \times R_{\text{high}}}{Lf} \\ r\prime_{\text{Buck}} = \frac{(1 - d_{\text{Buck}}\prime) \times R_{\text{low}}}{Lf} \end{cases} \tag{17}$$

where $d\prime_{\text{Boost}}$ and $d_{\text{Buck}}\prime$ are the duty cycles of that converter in step-up and step-down mode, respectively. $r\prime_{\text{Boost}}$ and $r\prime_{\text{Buck}}$ are the current ripple ratios of that converter in step-up and step-down mode, respectively.

Supposing that the output power, inductor, and switching frequency of the proposed converter and the traditional two-level converter are equal, it can be obtained that

$$\frac{r_{\text{Boost}}}{r\prime_{\text{Boost}}} = \frac{r_{\text{Buck}}}{r\prime_{\text{Buck}}} = \frac{1}{2}. \tag{18}$$

It can be concluded from (18) that the inductor current ripple ratio in the proposed converter is lower than that in the traditional two-level converter. On the other hand, if the inductor current ripple ratios are equal, the inductor of the proposed converter is only half that of the traditional one, which means that the proposed converter has outstanding dynamic response.

3.3. Good Dynamic Performance

The proposed converter can work in both the step-up and step-down modes. In order to save paper space, only the dynamic performance in step-down mode is analyzed. Before analyzing the dynamic performance, a small-signal model of step-down mode is needed.

When the proposed converter operates in the range $0.5 < d_{\text{Buck}} < 1$, the main power switches Q_3, Q_4, and Q_5 have three effective switching states: $S_3S_4S_5$ = [111, 100, 011]. u_{high}, u_{low}, and d_{Buck} are the input, the output, and the control variables, respectively. i_{L}, u_{C1}, and u_{Clow} are the state variables. r is the equivalent series resistance for C_1.

When $S_3S_4S_5$ = 111, the operating time of the proposed converter is $(2d_{\text{Buck}} - 1) \times$ T. The state space average model in this operating time is

$$\begin{cases} \begin{bmatrix} \dot{i}_{\text{L}} \\ \dot{u}_{\text{C}_1} \\ \dot{u}_{\text{Clow}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L} \\ 0 & -\frac{1}{C_1 r} & 0 \\ -\frac{1}{C_{low}} & 0 & -\frac{1}{C_{low}R} \end{bmatrix} \begin{bmatrix} i_{\text{L}} \\ u_{\text{C}_1} \\ u_{\text{Clow}} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} \\ \frac{1}{C_1 r} \\ 0 \end{bmatrix} u_{\text{high}} \\ u_{\text{low}} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{\text{L}} & u_{\text{C}_1} & u_{\text{Clow}} \end{bmatrix}^T \end{cases}. \tag{19}$$

When $S_3S_4S_5$ = 100, the operating time of the proposed converter is $(1 - d_{\text{Buck}}) \times$ T. The state space average model in this operating time is

$$\begin{cases} \begin{bmatrix} \dot{i}_{\text{L}} \\ \dot{u}_{\text{C}_1} \\ \dot{u}_{\text{Clow}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L} \\ 0 & 0 & 0 \\ -\frac{1}{C_{low}} & 0 & -\frac{1}{C_{low}R} \end{bmatrix} \begin{bmatrix} i_{\text{L}} \\ u_{\text{C}_1} \\ u_{\text{Clow}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} u_{\text{high}} \\ u_{\text{low}} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{\text{L}} & u_{\text{C}_1} & u_{\text{Clow}} \end{bmatrix}^T \end{cases}. \tag{20}$$

When $S_3S_4S_5$ = 011, the operating time of the proposed converter is $(1 - d_{\text{Buck}}) \times$ T. The state space average model in this operating time is

$$\begin{cases} \begin{bmatrix} \dot{i}_{\text{L}} \\ \dot{u}_{\text{C}_1} \\ \dot{u}_{\text{Clow}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L} \\ 0 & -\frac{1}{C_1 r} & 0 \\ -\frac{1}{C_{low}} & 0 & -\frac{1}{C_{low}R} \end{bmatrix} \begin{bmatrix} i_{\text{L}} \\ u_{\text{C}_1} \\ u_{\text{Clow}} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{C_1 r} \\ 0 \end{bmatrix} u_{\text{high}} \\ u_{\text{low}} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{\text{L}} & u_{\text{C}_1} & u_{\text{Clow}} \end{bmatrix}^T \end{cases}. \tag{21}$$

Combining (19) and (20) with (21), the average model of the proposed converter is

$$\begin{cases} \begin{bmatrix} \dot{i}_{\mathrm{L}} \\ \dot{u}_{\mathrm{C}_1} \\ \dot{u}_{\mathrm{Clow}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L} \\ 0 & -\frac{d_{\mathrm{Buck}}}{C_1 r} & 0 \\ -\frac{1}{C_{low}} & 0 & -\frac{1}{C_{low}R} \end{bmatrix} \begin{bmatrix} i_{\mathrm{L}} \\ u_{\mathrm{C}_1} \\ u_{\mathrm{Clow}} \end{bmatrix} + \begin{bmatrix} \frac{1-2d_{\mathrm{Buck}}}{L} \\ \frac{d_{\mathrm{Buck}}}{C_1 r} \\ 0 \end{bmatrix} u_{\mathrm{high}} \\ u_{\mathrm{low}} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{\mathrm{L}} & u_{\mathrm{C}_1} & u_{\mathrm{Clow}} \end{bmatrix}^T \end{cases}. \tag{22}$$

The state, the input, the output, and the control variables can be described by using the small-signal disturbance variables as:

$$\begin{cases} i_{\mathrm{L}} = I_{\mathrm{L}} + \hat{i}_{\mathrm{L}} \\ u_{\mathrm{C1}} = U_{\mathrm{C1}} + \hat{u}_{\mathrm{C1}} \\ u_{\mathrm{Clow}} = U_{\mathrm{Clow}} + \hat{u}_{\mathrm{Clow}} \\ u_{\mathrm{high}} = U_{\mathrm{high}} + \hat{u}_{\mathrm{high}} \\ u_{\mathrm{low}} = U_{\mathrm{low}} + \hat{u}_{\mathrm{low}} \\ d_{\mathrm{Buck}} = D_{\mathrm{Buck}} + \hat{d}_{\mathrm{Buck}} \end{cases} \tag{23}$$

where I_{L}, U_{C1}, U_{Clow}, U_{low}, U_{high}, and D_{Buck} are steady state components, and $\hat{i}_{\mathrm{L}}$, $\hat{u}_{\mathrm{C1}}$, $\hat{u}_{\mathrm{Clow}}$, $\hat{u}_{\mathrm{low}}$, and $\hat{d}_{\mathrm{Buck}}$ are their corresponding small-signal disturbance variables.

As a result, the small-signal model of the proposed converter is

$$\begin{cases} \begin{bmatrix} \dot{\hat{i}}_{\mathrm{L}} \\ \dot{\hat{u}}_{\mathrm{C1}} \\ \dot{\hat{u}}_{\mathrm{Clow}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L} \\ 0 & -\frac{d_{\mathrm{Buck}}}{C_1 r} & 0 \\ -\frac{1}{C_{low}} & 0 & -\frac{1}{C_{low}R} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{L}} \\ \hat{u}_{\mathrm{C1}} \\ \hat{u}_{\mathrm{Clow}} \end{bmatrix} + \begin{bmatrix} \frac{1-2d_{\mathrm{Buck}}}{L} \\ \frac{d_{\mathrm{Buck}}}{C_1 r} \\ 0 \end{bmatrix} \hat{u}_{\mathrm{high}} + \left\{ \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{C_1 r} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{L}} \\ u_{\mathrm{C}_1} \\ u_{\mathrm{Clow}} \end{bmatrix} + \begin{bmatrix} -\frac{2}{L} \\ \frac{1}{C_1 r} \\ 0 \end{bmatrix} u_{\mathrm{high}} \right\} \hat{d} \\ \hat{u}_{\mathrm{low}} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{L}} & \hat{u}_{\mathrm{C1}} & \hat{u}_{\mathrm{Clow}} \end{bmatrix}^T \end{cases}. \tag{24}$$

Using the parameters shown in Table 1, when the output voltage is 25 V, the control-to-output transfer function can be expressed as

$$G_{\mathrm{C}} = \left. \frac{\hat{u}_{\mathrm{low}}(s)}{\hat{d}_{\mathrm{Buck}}(s)} \right|_{\hat{u}_{\mathrm{high}}(s)=0} = \frac{6.52 \times 10^7 s + 1.5 \times 10^{13}}{s^3 + 3.32 \times 10^5 s^2 + 2.55 \times 10^8 s + 7.52 \times 10^{12}}. \tag{25}$$

Assume that the proposed converter and the traditional two-level converter have the same output power, inductor current ripple ratio, and switching frequency. Then, the inductor of the traditional two-level converter is double that of the proposed converter. The control-to-output transfer function of the traditional two-level converter in step-down mode can be expressed as

$$G_{\mathrm{C}}\prime = \left. \frac{\hat{u}_{\mathrm{low}}(s)}{\hat{d}_{\mathrm{Buck}}(s)} \right|_{\hat{u}_{\mathrm{high}}(s)=0} = \frac{200}{6.14 \times 10^{-8} s^2 + 59 \times 10^{-6} s + 1}. \tag{26}$$

The Bode diagram of the duty cycle to output voltage open-loop transfer function is shown in Figure 10. According to Figure 10, the crossover frequency of the proposed converter is higher than that of the traditional two-level converter due to smaller inductance.

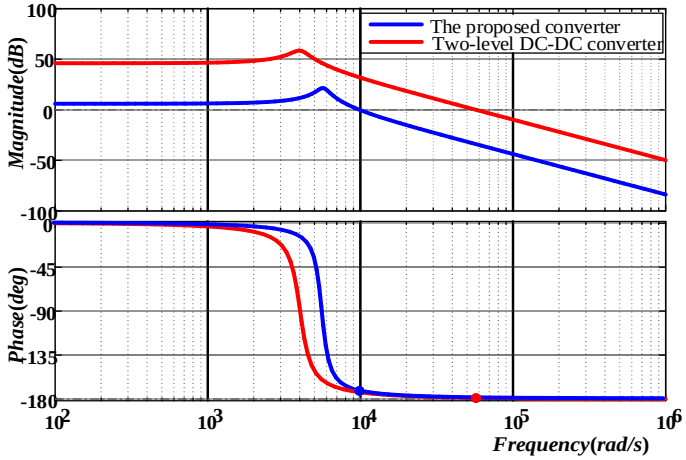


Figure 10. Bode diagram of the open-loop system.

The switching frequency of the traditional two-level converter can be chosen to be five times the crossover frequency. At this point, the equivalent switching frequency of the proposed converter is twice that of the switching frequency. The side-band effect has been eliminated due to interleave control. Therefore, the crossover frequency of the proposed converter can be increased to two-fifths of f. It means that the proposed converter can push to a higher control bandwidth, which leads to better dynamic performance.

In step-up mode, small inductance and a higher equivalent switching frequency lead to better dynamic performance too.

The control-to-output transfer function derived above is helpful to design the voltage controller shown in Figure 8. The voltage controller is a PI (proportional integral) regulator and it can be expressed as

$$G_{\mathrm{PI}}(s) = k_p + k_i \frac{1}{s}. \tag{27}$$

Using the control-to-output transfer function, k_{p} and k_{i} can be deduced.

Due to the use of the capacitor-clamped H-type structure, the proposed converter has the following advantages:

- Avoiding the narrow pulse of PWM voltage waveforms when a high voltage conversion ratio is achieved: It costs a little time to turn a power semiconductor on and off, thus the ideal narrow pulse of the PWM voltage waveform is difficult to realize. The higher the voltage conversion ratio of the proposed converter is, the closer the duty cycle is to 0.5. When the duty cycle approaches 0.5, the time used to maintain the *ON* and *OFF* state for all power semiconductors is nearly equal in each period, which is beneficial to avoid the narrow pulse of PWM voltage waveforms while a high voltage conversion ratio is achieved.
- Reducing inductor current ripple: The inductor L is charged and discharged twice during each switching period, as 0 and 0 show. With a small duty cycle in step-up mode, the charging time of the inductor is short. The charging time of the inductor in step-down mode is short too. Then, the inductor current ripple will decrease.
- Good dynamic performance: Due to using small inductance and a higher equivalent switching frequency, the proposed converter has a better dynamic performance.

3.4. Voltage and Current Stress on the Power Switches

According to the current flow path of the proposed converter in step-up mode, as shown in 0 (or the current-flow path of the step-down mode, as shown in Figure 5), using the *KVL* (Kirchhoff's voltage law), the voltage stress on Q_1–Q_5 in the step-up and the step-down modes can be obtained as

$$U_{Q1} = U_{Q2} = U_{Q3} = U_{Q4} = U_{Q5} = U_{high}. \tag{28}$$

The voltage stress on Q_1–Q_5 in the step-up and step-down modes is the same.

Similarly, according to current-flow path in step-up mode, as shown in Figure 3 (or the current-flow path in step-down mode, as shown in Figure 5), and the *KCL* (Kirchhoff's current law), the current stress (namely average currents when the switch is *ON*) on Q_1–Q_5 in the step-up and the step-down modes can be obtained as

$$\begin{cases} I_{Q1} = I_{Q2} = I_{Q3} = \frac{1}{1-2d_{Boost}} \times I_{high} \\ I_{Q4} = \frac{d_{Boost}}{(1-d_{Boost})(1-2d_{Boost})} \times I_{high} \\ I_{Q5} = \frac{1}{1-d_{Boost}} \times I_{high} \end{cases}. \tag{29}$$

The current stress on Q_1–Q_5 in the step-up and step-down modes is also identical.

4. Experimental Result and Analyses

In order to verify the feasibility of the theoretical analysis, an experimental prototype with the parameters shown in Table 1 has been developed.

Table 1. Experiment parameters.

Parameters	Values
Rated power P_n	320 W
Storage/filter capacitor C_{low} and C_{high}	260 uF
Clamp capacitor C_1	260 uF
Storage/filter inductor L	114 uH
High-voltage side U_{high}	200 V
Low-voltage side U_{low}	25~60 V
Switching frequency f	20 kHz
Power semiconductors Q_1–Q_5	IXTH 88N30P

4.1. Experimental Results in the Step-Up Mode

The PWM voltages of power semiconductors and the inductor current waveforms are shown in Figures 11 and 12. The PWM voltage of each power semiconductor is about 200 V, approximately equal to the high-voltage side U_{high}, which validates the analysis in Section 3. According to Figures 11 and 12, the voltage gain M_{Boost} of the proposed converter is 8 and the duty cycle d_{Boost} is about 0.44. The *ON* state time of the power switches Q_1–Q_2 is about 0.44 T and the *ON* state time of the power switches Q_3–Q_5 is about 0.56 T. At that high voltage gain, both the *ON* and *OFF* state times of those power switches are close to 0.5 T, which is effective for avoiding the narrow pulse of the PWM voltage waveforms. Due to using the synchronous rectification, the turn on and turn off of the controlled MOSFETs Q_3, Q_4, and Q_5 realize the ZVS (zero voltage switching), e.g., the gate signal S_4 and the voltage stress of Q_4 as shown in Figure 13. According to Figure 11, the inductor L is charged and discharged twice during each switching period. Therefore, the equivalent switching frequency of the proposed converter is double that of the real switching frequency f. This feature is beneficial to improve the dynamic performance and reduce the inductor current ripple of this converter.

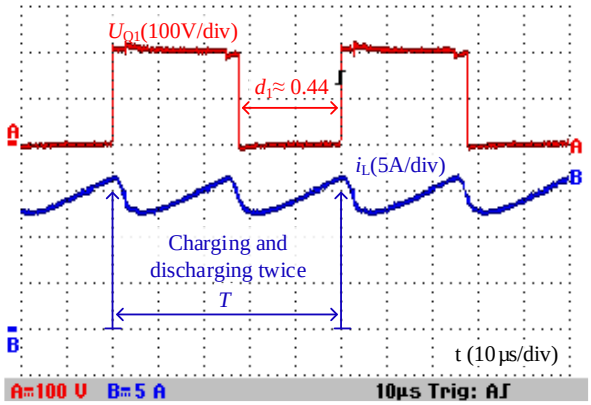


Figure 11. PWM voltage of power semiconductor Q_1 and inductor current i_L.

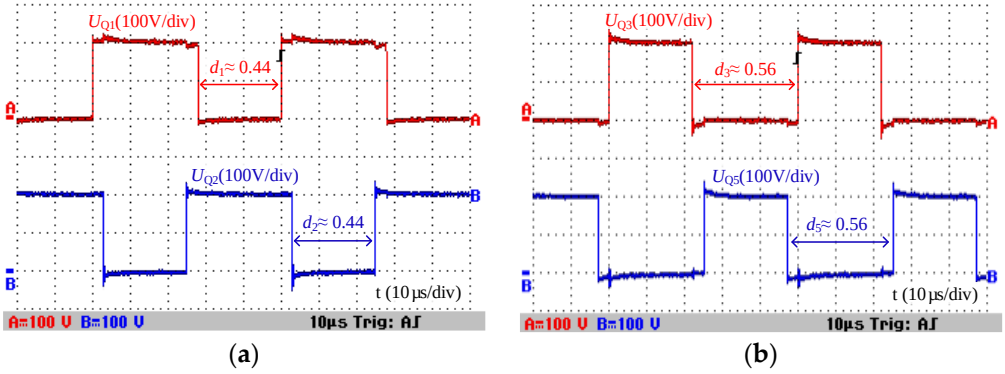


Figure 12. PWM voltages of power semiconductors; (**a**) U_{Q1} and U_{Q2}; (**b**) U_{Q3} and U_{Q5}.

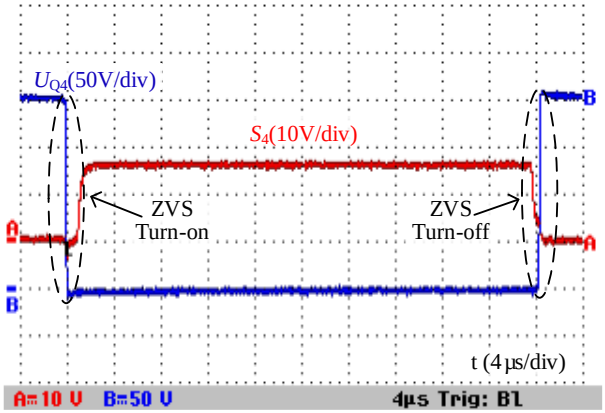


Figure 13. Voltage stress and gate signal of synchronous rectification power switch Q_4.

The voltage across clamp capacitor C_1 is approximately 200 V, being well-consistent with U_{high} as shown in Figure 14. Therefore, in the switching state 01, the clamp capacitor C_1 can maintain the forward bias of the anti-parallel diode of Q_5. The feature that all power semiconductors turn on and off only once during each switching period can be achieved. This is beneficial to avoid narrow pulses of the PWM voltage waveform at high voltage gain.

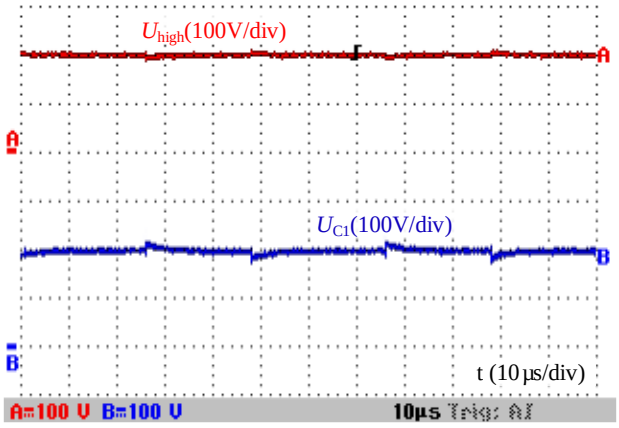


Figure 14. Output voltage and capacitor voltage stress when U_{low} = 25 V.

In the step-up mode, U_{low} and U_{high} are the input and output voltage, respectively. The output voltage can stay around the reference value of 200 V. The output/input voltage waveforms shown in Figure 15 can be obtained when changing the input voltage dynamically. According to Figure 15, when the input voltage varies continuously from 25 V to 60 V, the output voltage can stay around 200 V. The conclusion can be obtained from Figure 15 that the proposed converter can obtain a wide voltage conversion ratio from 3.3 to 8 in step-up mode.

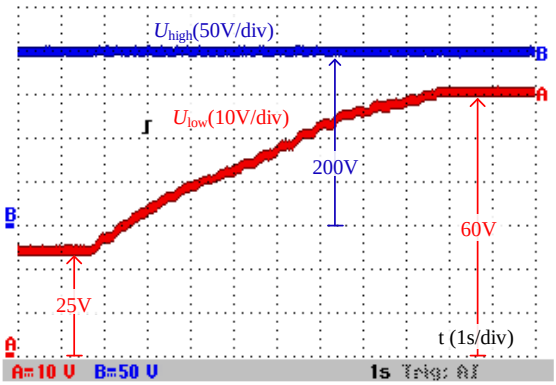


Figure 15. The output voltage and the wide-range changed input voltage from 25 V to 60 V in step-up mode.

4.2. Experimental Results in the Step-Down Mode

Figures 16 and 17 show the voltage waveforms of power semiconductors in the step-down operation mode. According to Figures 16 and 17, the PWM voltage of each power semiconductor is about 200 V, approximately equaling the high-voltage side U_{high}. The voltage gain M_{Buck} of the proposed converter is 1/8 and the duty cycle d_{Buck} is about 0.56. The *ON* state time of the power switches Q_3–Q_5 is about 0.56 T and the *ON* state time of the power switches Q_1–Q_2 is about 0.44 T. At that high voltage conversion ratio, both the *ON* and *OFF* state times of those power switches are close to 0.5 T, which is effective for avoiding the narrow pulse of the PWM voltage waveforms. In addition, the slave power semiconductors Q_1 and Q_2 also acted in the synchronous rectification operation, which turned on and turned off with ZVS, e.g., the gate signal S_1 and the voltage stress of Q_1, as shown in Figure 18. According to Figure 16, the inductor L is also charged and discharged twice during each switching period. The dynamic performance of the proposed converter in step-down mode is also improved.

According to Figure 19, the voltage across clamp capacitor C_1 is approximately 200 V, being well-consistent with U_{high}. Therefore, in the switching state 011, the clamp capacitor C_1 can maintain the power switch Q_5 *ON*. The feature that all power semiconductors turn on and off only once during each switching period can be achieved. This is also beneficial to avoid narrow pulses of the PWM voltage waveform at a high voltage conversion ratio, just like in step-up mode.

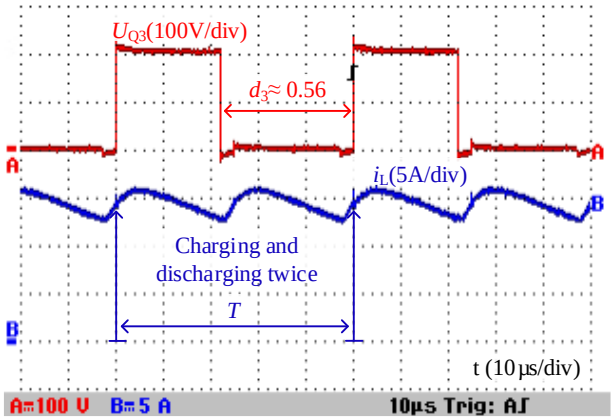


Figure 16. The PWM voltage of power semiconductor Q_3 and inductor current i_{L1}.

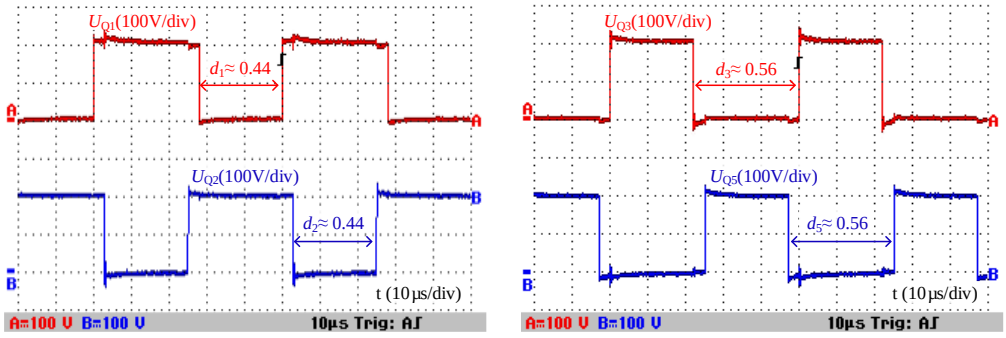


Figure 17. The PWM voltages of power semiconductors; (**a**) U_{Q1} and U_{Q2}; (**b**) U_{Q3} and U_{Q5}.

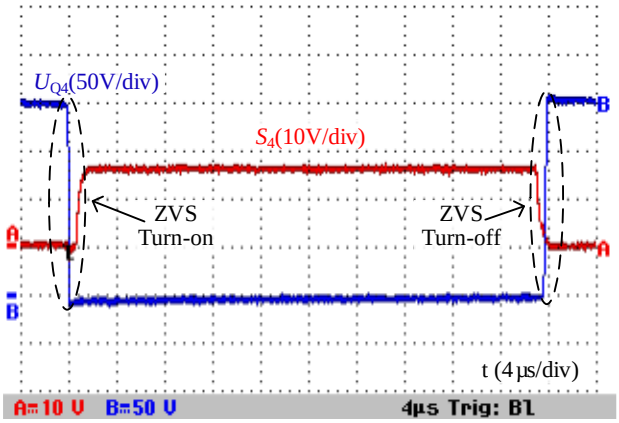


Figure 18. Gate signal and voltage stress of synchronous rectification power semiconductor Q_1.

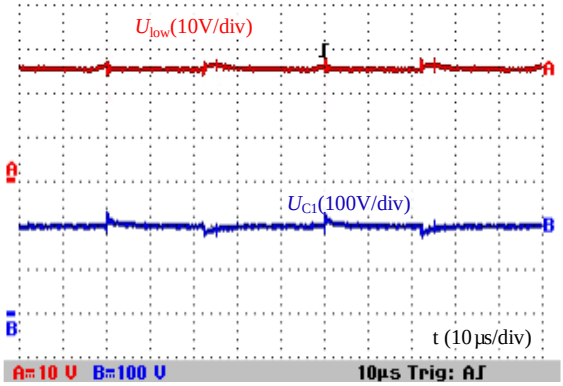


Figure 19. Output voltage and capacitor voltage stress when U_{high} = 200 V.

In the step-down mode, the input voltage is U_{high} and the output voltage is U_{low}. The output voltage can also stay around the reference value of 25 V with the action of the voltage control loop. The output/input voltage waveforms shown in Figure 20 can be obtained when changing the input voltage dynamically. According to Figure 20, when the input voltage varies continuously from 200 V to 75 V, the output voltage can stay around 200 V. The conclusion can be obtained from Figure 20 that the proposed converter can obtain a wide voltage conversion ratio from 1/8 to 1/3 in step-down mode.

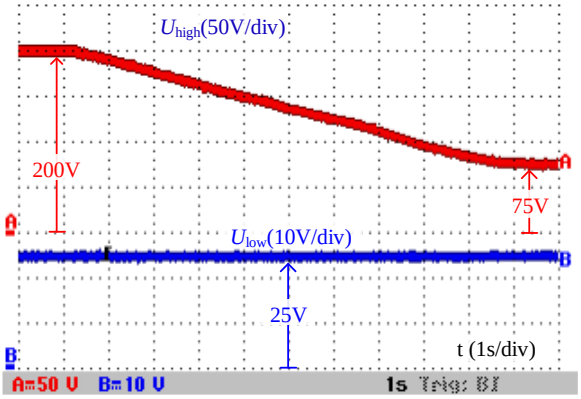


Figure 20. The output voltage and the wide-range changed input voltage from 200 V to 75 V in step-down mode.

4.3. Bidirectional Power Flow Experiment

In order to verify the performance of the proposed converter in a HESS, the related experiments are carried out using the HESS shown in Figure 1. The output voltages of the SC and battery are about 42 V and 50 V, respectively, and the DC load power varies with a step change between 400 W and 650 W. The proposed converter is used as the power interface between the SC and the DC bus.

With the DC load being suddenly increased and decreased, changes in the output currents are shown in Figure 21, where i_{bat} and i_{sc} denote the output currents of the battery and the SC, respectively. When the DC load required power changes from 400 W to 650 W suddenly, the SC compensates for the required power immediately by increasing the current i_{sc} from 0 to 6 A in 20 ms approximately, which protects the battery by avoiding a sudden change in current and prolongs its life. Gradually, the task of supplying the power shortage is transferred from the SC to the battery. The i_{sc} falls to 0 from 6 A along with the i_{bat} rising from 8 A to 13 A. Similarly, when the DC load required power changes from 650 W to 400 W suddenly, the current i_{sc} varies from 0 to −6 A in 20 ms approximately. As a result, the current from the battery decreases from 13 A to 8 A gradually, and the current of the SC returns to 0 from −6 A. When the DC load required power suddenly increases or decreases,

the SC can respond quickly to compensate for the power gap between the battery and the DC load. In this situation, the service life of the battery is extended because of the slow changes in its output current. It can be concluded from Figure 21 that the proposed converter can cooperate well in the HESS whether the load is suddenly changed or not.

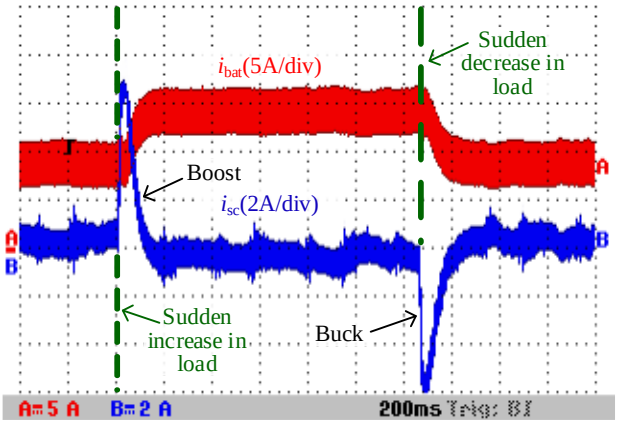


Figure 21. The output current waveforms of the battery and the super-capacitor (SC).

The efficiencies of the proposed converter in the step-up and step-down modes are shown in Figure 22. In step-up mode, U_{high} is 200 V and U_{low} varies from 25 V to 60 V continuously; in step-down mode, U_{low} is 25 V and U_{high} varies from 80 V to 200 V continuously. According to Figure 22, the efficiency varies from 91.52% to 94.80% in step-up mode, which is slightly lower than that in the step-down mode (varies from 92.01% to 95.30%). With the constant load power in step-up mode, the efficiency decreases accompanied by the input voltage declining due to the increasing losses caused by the growing input current. In the step-down mode, the efficiency decreases with the increase of high side voltages. Due to the increase in the high side voltages, the voltage stresses of the power semiconductors increase. Therefore, the turn on/off losses of the power semiconductors will increase.

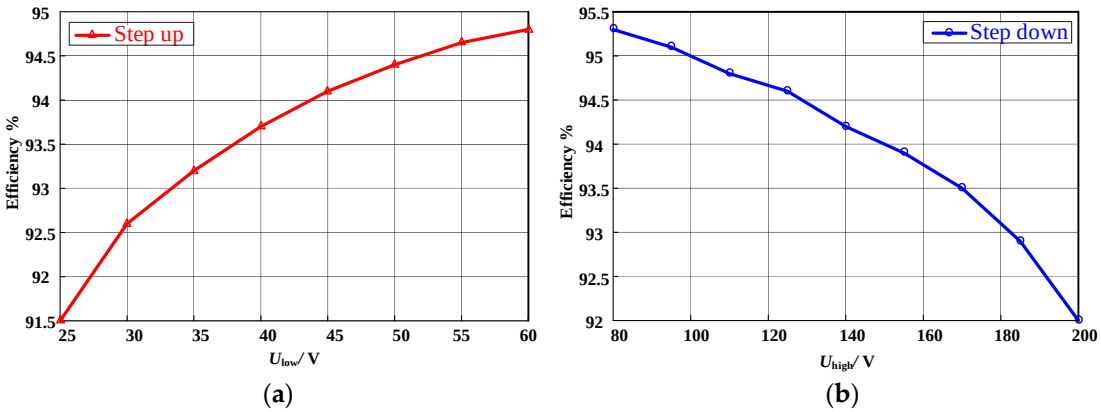


Figure 22. Efficiencies with different input voltages; (**a**) Step-up mode; (**b**) Step-down mode.

5. Conclusions

A new common grounded H-type bidirectional converter was proposed in this paper. It has the advantages of a wide voltage conversion ratio and a good dynamic response in both step-down and step-up operation modes. In addition, only one inductor is used in this converter, and the inductor is charged and discharged twice during each switching period, which results in a low inductor current ripple and a small size for this converter. Due to the use of a capacitor-clamped H-type structure,

the proposed converter can avoid the narrow pulse of the PWM voltage waveforms while achieving a high voltage conversion ratio. Besides, the efficiency of the converter is improved because the slave active power switches turn on and turn off with zero voltage. In order to prove the feasibility, the proposed converter was implemented in the laboratory with the proper voltage conversion ratio (3.3–8 in step-up mode and 1/8–1/3 in step-down mode). A theoretical analysis and experimental results proved that the proposed converter is suitable for connecting a low-voltage SC to a high-voltage DC bus.

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Author Contributions: Huakun Bi and Ping Wang designed the main parts of the study, including the operating principles analysis, characteristics analysis, and experiment. Zhishuang Wang helped in the hardware development, experiment, and some theoretical analysis.

Conflicts of Interest: The authors declare no conflict of interest.

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