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Switched-Capacitor-Based High Boost DC-DC Converter

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Abstract: A non-isolated high boost DC-DC converter topology based on a switched-capacitor (SC) structure is introduced in this paper. By controlling the duty cycle in each period, the voltage gain of the converter is adjusted. The main features of the proposed SC converter are the continuous input current, achieving high voltage gain with low voltage and current stress on the power components, no use of a high-frequency transformer, and easy to increase the voltage by adding the SC cell. To correct the operating analysis, a 200-W output power prototype was built with the input voltage in the range of [25 V, 50 V] and the output voltage of 200 V. The proposed inverter reaches a maximum efficiency of 93% at the input voltage of 25 V and the output power of 150 W. The simulation and experimental verifications match the analysis.

Keywords: non-isolated DC-DC converter; high boost converter; switched-capacitor

1. Introduction

Recently, with the development of industrialization, the use of the renewable resources—photovoltaic arrays, fuel cells, etc.—have been a most effective solution. However, they are DC sources with low voltage, low current, and instability. To link them to loads or grid applications, the power conversion generation in Figure 1 was developed. To convert the low voltage of the renewable sources into 200 V or 400 V DC voltage, a high step-up DC-DC stage [1–3] is set up as the first stage in the power-conversion system. The second-stage DC-AC converter can provide 110 Vrms or 220 Vrms AC volts for the grid-connected application.

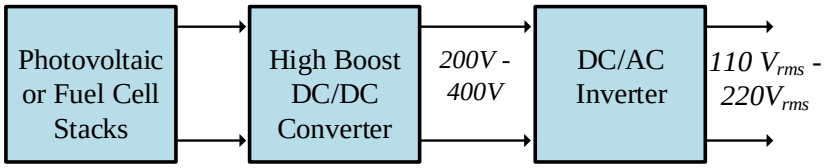


Figure 1. Power-conversion system.

Since the components have an equivalent series resistance (ESR), the traditional boost converter is difficult to step up a large gain voltage. When the high boost voltage is required, the boost converter needs to have a large duty cycle, which leads to high conduction loss and reducing efficiency [4–6]. Moreover, in order to achieve the high boost voltage gain, the various DC-DC converters have been presented, including isolated and non-isolated topologies. The isolated topology [7–10] can provide the isolation between input and output terminals, which is based on a high-frequency

transformer. Since the isolated topologies include a DC-AC stage and an AC-DC stage, they required a number of components, which increase the circuit's size. If the leakage inductances are designed carelessly, the switches appear as a voltage spike. The non-isolated topologies [11–19] can achieve a high efficiency with a simple circuit because of the lack of a transformer. In the non-isolated topologies, the high step-up voltage gain can be achieved by using the following techniques: cascade boost, switched-capacitor, switched-inductor, coupled inductor, and a mixture of them. The coupled-inductor-based converters [12–14] have a large voltage conversion ratio with increasing efficiency and reduces the voltage/current stress on switches and diodes. However, the circuits are complex to design and the leakage problem of the coupled inductor causes a high voltage spike on semiconductor components. The dual-switch-based converters [15–17] present a high voltage gain with high input current ripple. In these topologies, an additional active switch is required with the increasing gate drive. The SC structure was proposed in [18]. By charging the capacitors in parallel and discharging them in series the SC-based converter produces a high voltage at the output side. In [19], an interleaved DC-DC multilevel converter was proposed by combining a multilevel boost structure and a single inductor multiplier Cuk converter to achieve a minimum input current ripple. A non-isolated high step-up DC-DC converter with single-inductor-energy-storage cell-based SCs (SIESC-SCs) was introduced in [20]. By changing the SC cell connection, various converter topologies are obtained.

To decrease the converter's size and obtain a high voltage gain, the cascade boost converter, the voltage multiplier cells (VMC) boost converter, and the dual boost converter were proposed, as shown in Figure 2. The cascade boost converter, as shown in Figure 2a, can provide a high ratio, but the circuit is complex, and the size and cost of the converter are increased. The cascade converter can reduce switch S_1 and diode D_1 voltage stress, high flexibility, and suitability for high power applications. However, the switch S_2 and diode D_2 voltage stress are high. The VMC boost converter were presented in [5] and is shown in Figure 2b. The voltage ratio of the VMC boost converter can achieve a larger gain voltage by increasing the N cell of the VMC. The switches' and diodes' voltage stresses are decreased, and the diodes are turned off with ZCS. However, the duty cycle is limited and the switches' current stress is large, and the voltage stress is dependent on the number of VMC. The dual converter was quoted from [6], as shown in Figure 2c. Similarly, the dual boost converter decreases the voltage stress on the switches, the inductor current is rated roughly at half of the total input current, and the isolated gate driver is needed for the dual boost converter.

This paper proposes a new boost converter based on a switched-capacitor structure. The proposed SC converter has a large step-up gain with continuous input current. The operating principles and circuit analysis in continuous conduction mode (CCM) and discontinuous mode (DCM) are presented. The parameters selection of the proposed SC converter and a comparison with conventional converters are shown. Simulation and experiment verifications prove the correctness of the operating analysis.

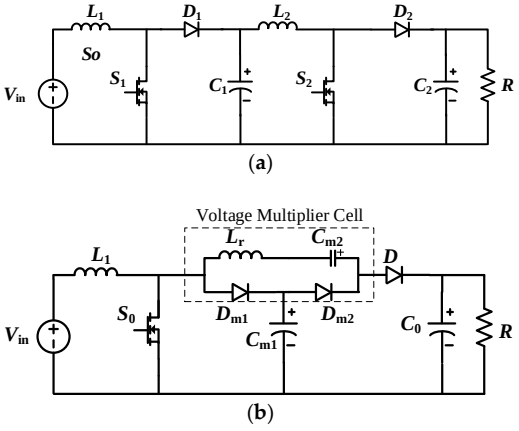


Figure 2. *Cont.*

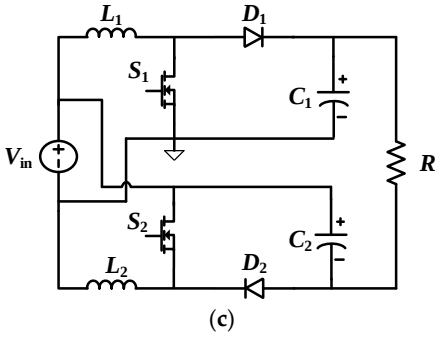


Figure 2. Conventional boost converter topologies. (**a**) The cascade boost topology; (**b**) the boost topology with voltage multiplier cells (VMC); and (**c**) dual boost converter.

2. Proposed SC Converter Topology

2.1. Proposed Topology

The proposed SC non-isolated boost DC-DC converter is presented in Figure 3, which includes a SC structure and multilevel-boost converter. It uses a single switch, five diodes, single inductor, five capacitors and load. Figure 4 shows a detailed PWM algorithm for the proposed SC converter. The switch S_0 is controlled by comparing the reference voltage, V_{ref} to the triangle waveform with the amplitude of "1".

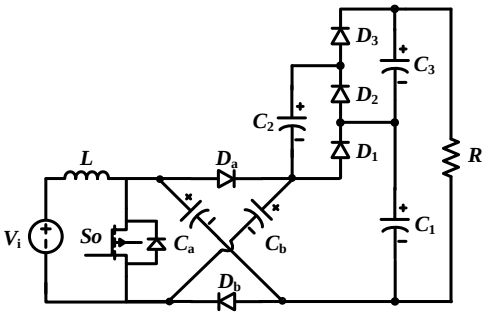


Figure 3. Proposed SC boost DC-DC.

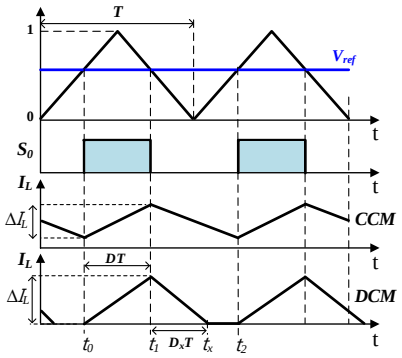


Figure 4. Key waveforms of the proposed SC DC-DC converter.

2.2. Circuit in CCM Operation

To facilitate the circuit analysis of the proposed converter, the following conditions are guaranteed as all components seem ideal and reflect no losses, the voltage of capacitors is constant, and the inductor current is increased and decreased linearly.

Mode 1 [t_0–t_1, Figure 5a]: The time interval in this mode is DT, where D is the duty cycle of switch S_0 in one switching period T. The MOSFET S_0 is turned on. The diodes D_1 and D_3 are forward-biased. The inductor is charged. We have the equivalent equations:

$$\begin{cases} V_L = V_i \\ V_{C1} = V_{Ca} + V_{Cb} \\ V_{C2} = V_{C3} \end{cases} \quad (1)$$

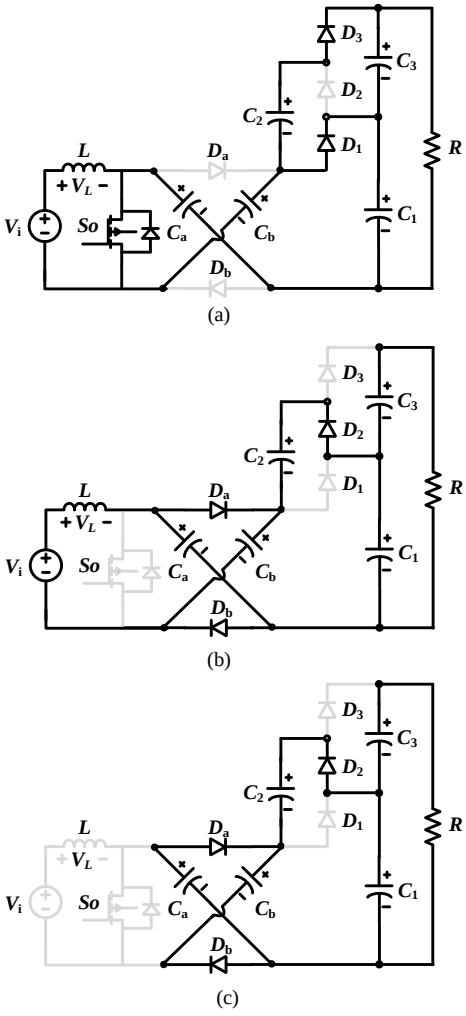


Figure 5. The operating mode of the proposed converter: (**a**) S_0 on; (**b**) S_0 off; and (**c**) the circuit in DCM.

Mode 2 [t_1–t_2, Figure 5b]: This interval time in mode 2 is $(1 - D)T$. Switch S_0 is turned off. The diodes D_a, D_b, and D_2 are forward-biased. The inductor delivers the stored energy to the load. We have:

$$\begin{cases} V_L = V_i - V_{Ca} \\ V_{Ca} = V_{Cb} \\ V_O = V_{C1} + V_{C3} \end{cases} \quad (2)$$

The average voltage across the inductor in period switching is zero:

$$\overline{V}_L = D \cdot V_i + (1 - D) \cdot (V_i - V_{Ca}) = 0 \quad (3)$$

In the steady state, the capacitor voltage and output voltage are calculated as:

$$\begin{cases} V_C = V_{Ca} = V_{Cb} = V_{C2} = V_{C3} = \frac{1}{1-D} V_i \\ V_{C1} = 2V_C = \frac{2}{1-D} V_i \\ V_O = 3V_C = \frac{3}{1-D} V_i \end{cases} \tag{4}$$

2.3. Circuit in DCM Operation

When the power load is reduced to a light load, the converter works in CCM. Then, the inductor current goes to zero and stays there until the new switching period starts. The inductor current waveform is the last one sketched in Figure 4. The inverter has one more mode, as shown in Figure 5c.

Mode 1 [t_0–t_1, Figure 5a] and mode 2 [t_1–t_x, Figure 5b]: These modes are the same as modes 1 and 2 in the CCM. The interval time in modes 1 and 2 is DT and $(1 - D - D_x)T$, respectively.

Mode 3 [t_x–t_2, Figure 5c]: The interval time in this mode is D_xT. The switch S_0 is still off. The inductor current is zero. The equivalent circuit is shown in Figure 5c. The switching ripple of peak amplitude is:

$$\Delta I_L = \frac{V_i}{L} \cdot DT \tag{5}$$

If the power losses of circuit are equal to zero, the average input current is calculated as:

$$\bar{I}_i = \frac{P_o}{V_i} = \frac{V_o^2}{RV_i} = \frac{9V_i}{(1-D)^2 R} \tag{6}$$

where P_o and R are the power and the resistance of the load, respectively.

The condition of the proposed converter in the discontinuous conduction mode is:

$$\bar{I}_L < (\Delta I_L / 2) \tag{7}$$

Substituting Equations (5) and (6) into (7), we have:

$$K < K_{crit}(D) \tag{8}$$

where $K = 18L/(RT)$, and $K_{crit}(D) = D \cdot (1 - D)^2$.

Applying the inductor volt-second balance, the D_x was obtained as:

$$D_x = \frac{DV_i}{V_C - V_i} \tag{9}$$

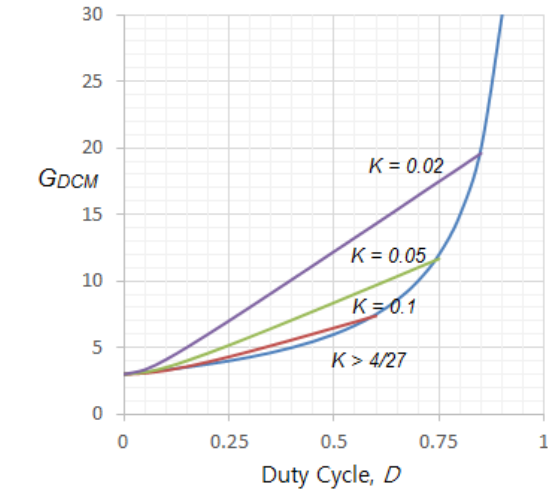
From Figure 5, the average inductor current is easily evaluated:

$$\bar{I}_L = \frac{V_i}{2L} \cdot D \cdot (D + D_x) \cdot T = \frac{V_o^2}{V_i R} \tag{10}$$

From Equations (8)–(10), we have:

$$G_{DCM} = \frac{V_o}{V_i} = \frac{3 + \sqrt{9 + \frac{36D^2}{K}}}{2} \tag{11}$$

Figure 6a gives the voltage gain of the proposed SC converter in DCM/CCM. The output voltage gain in the DCM is higher in the CCM. The converter works in the CCM when Kcrit > 0.148. Figure 6b shows the relationship between K_{crit} and D at CCM/DCM boundary.



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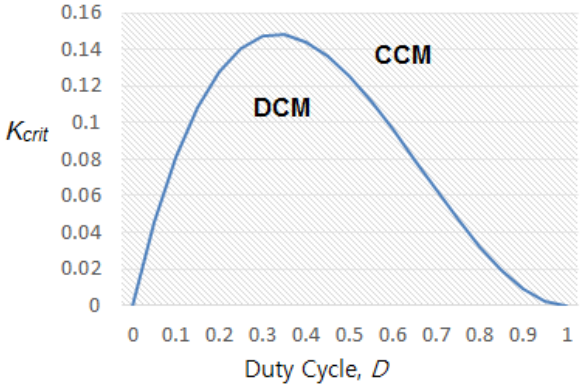


(**b**)

Figure 6. Curves in DCM/CCM operation. (**a**) Voltage gain of the proposed SC converter in DCM/CCM; (**b**) K_{crit} and D at the CCM/DCM boundary.

3. Capacitance and Inductance Selections

3.1. Inductance Selection

The inductor is chosen based on the current ripple through it. From Figure 5a, we have:

$$V_L = L\frac{di}{dt} = V_i \tag{12}$$

where di/dt is the variation of the inductor current. Equation (12) can be rewritten as:

$$V_L = L\frac{\Delta i}{\Delta t} = V_i \tag{13}$$

The inductor current ripple is calculated as:

$$\Delta i = a\% \cdot I_L = \frac{H \cdot P}{V_i} \tag{14}$$

where H (%) and $a\%$ are the converter efficiency and the inductor current ripple, respectively.

Based on the inductor current ripple in DT interval and Equations (13) and (14), the inductance is calculated as:

$$L = \frac{V_i^2}{a \cdot H \cdot P_o} \cdot DT \tag{15}$$

3.2. Capacitance Selection

In mode 2, the peak current flows to capacitor C_3 calculated as:

$$I_{C3} = C_3 \frac{dv}{dt} = I_o \tag{16}$$

The capacitance is chosen as $C = C_a = C_b = C_2 = C_3 = 0.5C_1$. From Equation (16), we obtain:

$$C = \frac{3DT}{\%bR} \tag{17}$$

where $\%b$ is the capacitor C_3 voltage ripple.

3.3. Calculation of Power Loss

Power Loss of Switch:

The power loss of switch are the conduction loss and the switching loss. The MOSFET conduction loss of switch S_0 is:

$$P_{cS} = R_{DSon} \cdot D \cdot I_{in}^2/4 \tag{18}$$

where R_{DSon} is the drain-source resistance of the MOSFET.

The MOSFET switching loss is determined as [21]:

$$P_{swS} = V_C \cdot \frac{I_{in}}{2} \cdot f_s \cdot \left(\frac{tru + tfi}{2} + \frac{tri + tfu}{2} \right) \tag{19}$$

where tru, tfu, tri, and tfi are the rising time, falling time of voltage, rising time, and falling time of current, respectively, and the parameters are obtained from the datasheet.

Power Loss of the Diodes:

The conduction loss of diodes D_0, D_1, and D_2 is:

$$\begin{aligned} P_{CD} &= 2 \cdot \left[u_{Dx} \cdot I_{in}/2 + R_{Dx} \cdot I_{in}^2/4 \right] \cdot (1 - D) \\ &+ 2\left(u_{Dx} \cdot I_o/2 + R_{Dx} \cdot I_o^2/4 \right) \cdot D \\ &+ \left(u_{Dx} \cdot I_o/2 + R_{Dx} \cdot I_o^2/4 \right) \cdot (1 - D) \end{aligned} \tag{20}$$

where u_{Dx} and R_{Dx} are the drop voltage and the resistance of the D_a, D_b, D_1–D_3, respectively.

The reverse recovery loss of the diodes is:

$$P_{rrD} = 5Q_{rrf} \cdot V_C \cdot f_s \tag{21}$$

where Q_{rrf} is the reverse recovery charge of diodes.

Power Loss in the Capacitor:

The capacitor power loss is calculated by:

$$P_C = r_{Ca} \cdot I_{Ca}^2 + r_{Cb} \cdot I_{Cb}^2 + r_{C1} \cdot I_{C1}^2 + r_{C2} \cdot I_{C2}^2 + r_{C3} \cdot I_{C3}^2 \tag{22}$$

where r_{Ca}, r_{Cb}, r_{C1}, r_{C2}, and r_{C3} are the internal resistances of C_1, C_2, and C_3 capacitors.

The current of capacitors C_a, C_b, C_1, C_2, and C_3 are defined by:

$$\begin{cases} I_{Ca} = I_{Cb} = \frac{I_{in}}{2} \\ I_{C1} = \sqrt{(I_o - I_{in}/2)^2 \cdot D + \left(\frac{I_o}{2}\right)^2 \cdot (1-D)} \\ I_{C2} = \frac{I_o}{2} \\ I_{C3} = \sqrt{\left(\frac{I_o}{2}\right)^2 \cdot D + I_o^2 \cdot (1-D)} \end{cases} \quad (23)$$

Power Loss of the Inductor:

The power loss of the inductor is such as the loss of core and copper wire. The inductor core loss is expressed as:

$$P_{fe} = K_{fe} \cdot \Delta B^{\beta} \cdot A_c \cdot l_m \quad (24)$$

where K_{fe} is a constant, β is selected from the core datasheet; A_c is the core cross-sectional area; and l_m is the core mean magnetic path length.

The inductor copper losses are given by:

$$P_{cu} = R_L \cdot I_{L\_RMS}^2 \quad (25)$$

where R_L is the resistance wire.

The power loss is calculated and shown in Figure 7a at V_i = 25 V, V_o = 200 V and P_o = 200 W. The parameters of device are used to calculate the power loss, are shown in Tables 1 and 2. The total power loss is 13.55 W and the calculated efficiency of the proposed SC converter is 93.23%. Figure 7b shown the calculated efficiency comparison between the proposed converter and SIESC-SCs [20] when V_i = 25 V and V_o = 200 V. The power loss of both proposed converter and SIESC-SCs are determined based on the parameters in Table 2. As shown in Figure 7b, the calculated efficiency of the proposed SC converter is slightly lower than that of the SIESC-SCs [20]. This is because the proposed inverter uses two more diodes and capacitors to obtain the high voltage gain. As shown in Figure 7a, the major loss contributions are from diodes and capacitors. Note that the parameters for power loss calculation in Table 2 are chosen from devices those are available in the laboratory for the experimental test. Therefore, these parameters are not optimally selected for efficiency consideration. The devices including MOSFET and diodes with lower voltage rating should be selected to reduce the power loss of the proposed converter.

Table 1. Conducting current of the devices in the proposed SC converter.

Devices	Conducting Current	Conducting Time
S_o	$I_L/2$	$D{\cdot}T$
D_a, D_b	$I_L/2$	$(1-D){\cdot}T$
D_1, D_3	$I_o/2$	$D{\cdot}T$
D_2	$I_o/2$	$(1-D){\cdot}T$
L	I_L	T
C_a, C_b	$I_L/2$	T
C_1	$I_o - I_L/2$	$D{\cdot}T$
	$-I_o/2$	$(1-D){\cdot}T$
C_2	$-I_o/2$	T
C_3	$-I_o/2$	$D{\cdot}T$
	$-I_o$	$(1-D){\cdot}T$

Table 2. Parameters of the devices.

Devices	SIESC-SCs [20]	Proposed SC Converter
MOSFET S_0	STW88N65M5 (650 V, 84 A, 24 m Ω)	
Diodes	DSEI30-06A (600 V, 37 A)	DSEI30-06A (600 V, 37 A)
ESR of capacitors	280 mΩ	280 mΩ
ESR of C1 (470 µF/400 VDC)	130 mΩ	130 mΩ
Inductor core	CM777125 (142 nH/N^2)	CM777125 (142 nH/N^2)
Copper wire resistivity (ρ)	1.724 µΩ-cm	1.724 µΩ-cm

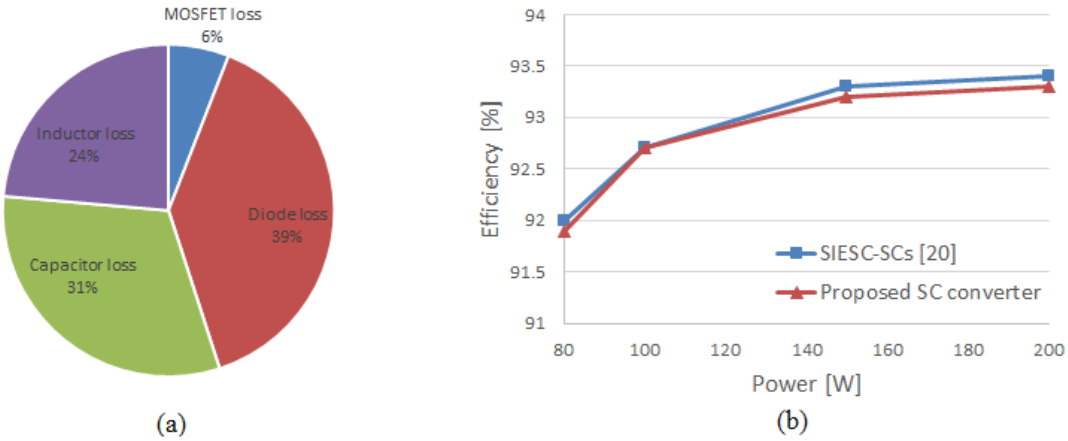


Figure 7. Power loss calculation. (**a**) Power loss of the proposed SC converter; and (**b**) comparison of the calculated efficiency.

4. Comparison with Other High Voltage Gain Converters

The comparison between the proposed SC converter and other converters, including the dual boost converter (DBC) [3], the cascade boost converter (CBC) [5], the boost voltage multiplier cell (B-VMC) (n = 2) [6], the single inductor multiplier Cuk converter (SLMC) [19], and the converter with the SIESC-SCs [20], are shown in Tables 3 and 4. In the comparison to DBC [3], B-VMC [6], and CBC [5], the proposed SC converter saves one inductor. Moreover, the voltage stress on diodes and switches of the proposed SC converter is small. Similar to the CBC [5] and B-VMC [6], the proposed SC converter uses one active switch. Compared to the DBC [3], B-VMC [6], CBC [5], and SIESC-SCs [20], the proposed SC converter uses two more diodes and capacitors, but the voltage gain of the proposed SC converter is higher. When the gain and voltage stress of active components are considered, the SLMC [19] is an interesting topology. However, the proposed SC converter has the same advantages with SLMC [19] and uses one less capacitor and one less diode.

Table 3. Comparison of topologies.

Converter	*L*	*C*	Switches	Diodes
DBC [3]	2	2	2	2
B-VMC (n = 2) [6]	2	3	1	3
CBC [5]	2	2	1	2
SLMC [19]	1	6	1	6
SIESC-SCs [20]	1	3	1	3
Proposed	1	5	1	5

Table 4. Comparison voltage stress and gain of topologies.

Converter	Switched Stress	Diode Stress	Voltage Gain
DBC [3]	$V_o/2$	$V_o/2$	$G = (1 + D)/(1 - D)$
B-VMC ($n = 2$) [6]	$V_o/2$	$V_o/2$	$G = 2/(1 - D)$
CBC [5]	$V_o/2$	$V_o/2$	$G = 1/(1 - D)^2$
SLMC [19]	$V_o/3$	$V_o/3$	$3/(1 - D)$
SIESC-SCs [20]	$V_o/2$	$V_o/2$	$2/(1 - D)$
Proposed	$V_o/3$	$V_o/3$	$G = 3/(1 - D)$

Figure 8 shows the voltage gain comparison between the proposed SC converter and the other non-isolated converters in the CCM. The voltage gain of the proposed SC converter is the same as that of SLMC [19] and is highest when $D < 2/3$. Therefore, the proposed configuration is more profitable than other non-isolated configurations of the boost coefficient.

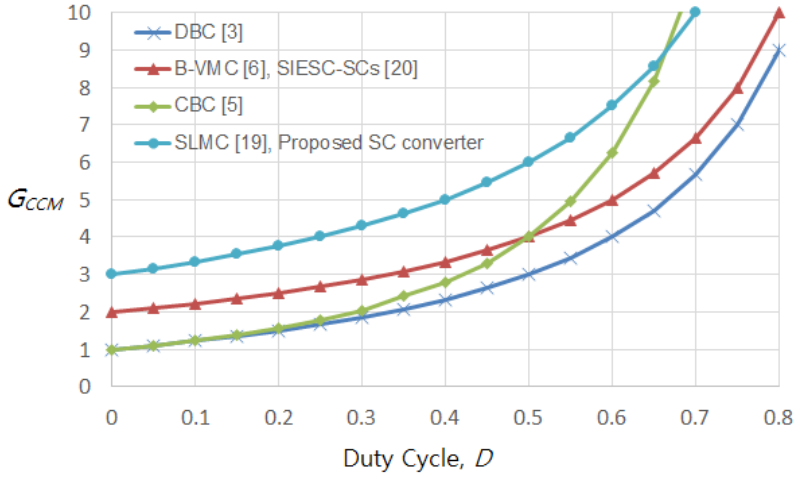


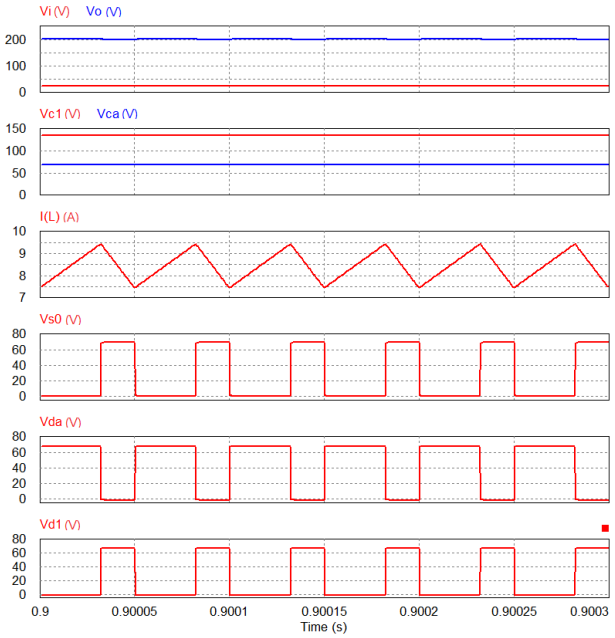
Figure 8. Voltage gain comparison with other non-isolated converters.

5. Simulation and Experimental Verifications

5.1. Simulation Verification

To confirm the operating principle of the proposed DC-DC converter, PSIM simulation software was used to prove the correctly of the operating principle with the parameters as $L = 0.4$ mH, $C_1 = 470$ µF, $C_a = C_b = C_2 = C_3 = 220$ µF. The on-resistance of the MOSFET is 24 mΩ. The forward-voltage of diodes is set to 1.4 V. The switching frequency of semiconductor components is 20 kHz. The input DC source is used to adjust from 25 V to 50 V. The output voltage is stepped up to 200 V.

Figure 9a shows the simulation results for the proposed SC converter when $V_i = 25$ V and $D = 0.644$. As shown in Figure 9a, the input current is continuous and the peak-to-peak inductor current is 1.96 A. The capacitor voltages are boosted to $V_{Ca} = V_{Cb} = 68$ V, $V_{C1} = 134$ V, and $V_{C2} = V_{C3} = 66$ V. Then, the input voltage is increased to 50 V and the duty cycle is decreased to 0.282, while the output voltage is still 200 V, as shown in Figure 9b. The input current in this case is also continuous with the peak-to-peak inductor current of 1.7 A.



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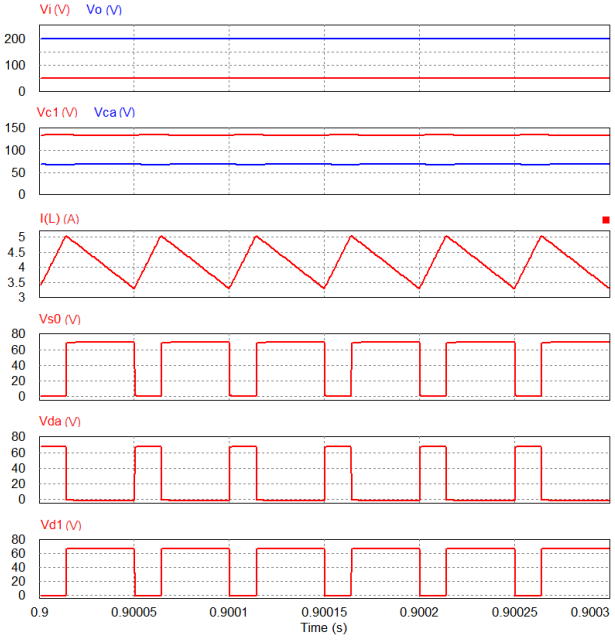


(**b**)

Figure 9. Simulation waveforms when (**a**) V_i = 25 V and (**b**) V_i = 50 V. Waveforms: input voltage, output voltage, capacitor C_1, C_2, C_3, C_a and C_b voltages, input current, drain-source voltage of S_0, and diode D_a and D_1 voltages.

5.2. Experimental Verifications

The experiment results are implemented by using a TMS320F28335 DSP kit with experimental parameters as shown in Tables 5 and 6. One MOSFET is STW88N65M5 and five diodes are DSEI30-06A. The output voltage and output powers are 214 V and 200 W, respectively. Figure 10 shows a photograph of the converter prototype.

Table 5. Parameters for verification.

Parameter	Values
Output power, P_o	200 W
Input voltage, V_i	25 V
Output voltage, V_o	200 V
Switching frequency	20 Khz
The ripple of inductor current (a%)	≤20%
The ripple of capacitor voltage (b%)	≤5%

Table 6. Accessories used for experiments.

Number	Component	Values
1	Inductor L	0.4 mH; 20 A
2	Capacitor C_a, C_b, C_2, C_3	220 μF; 400 V
3	Capacitor C_1	470 μF; 400 V
4	Diode D_a, D_b, D_1, D_2, D_3	DSEI30-06A
5	Mosfet S_0	STW88N65M5
6	Load (R)	200 Ω

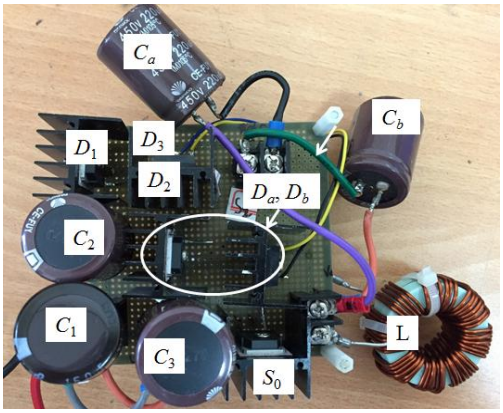
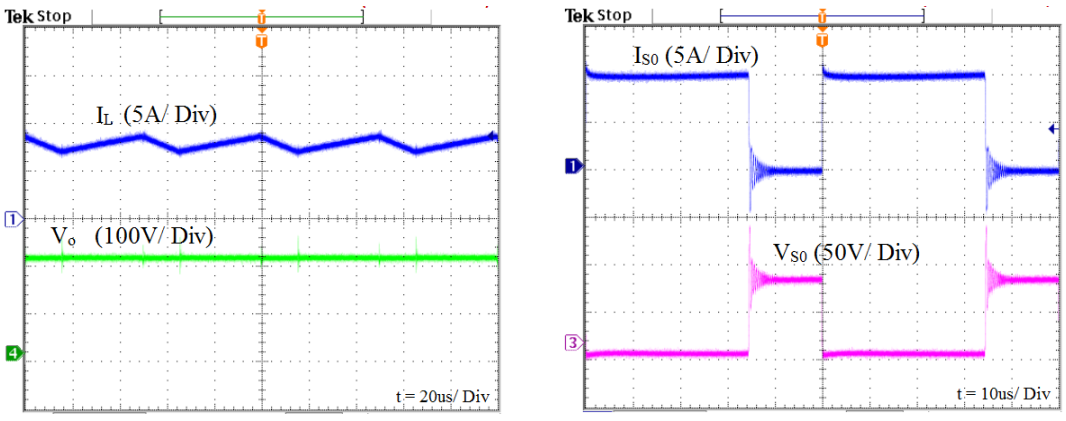


Figure 10. Prototype of the converter.

Figure 11 shows the experimental results of the proposed SC converter in CCM when V_i = 25 V. The output voltage is boosted to 200 V when the input voltage is 25 V. The peak-to-peak ripple input current is 2 A, which is close to the simulation value.



(**a**) (**b**)

Figure 11. *Cont.*

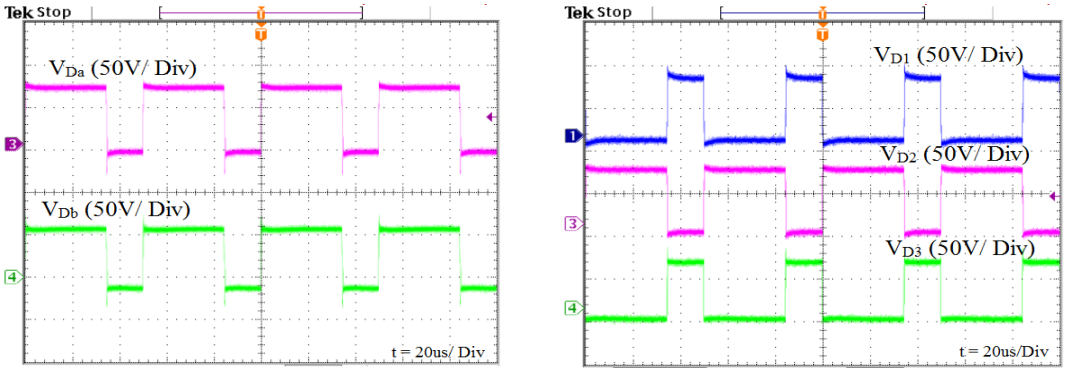


Figure 11. Experimental results when V_i = 25 V and D = 0.65. From top to bottom: (**a**) input current and output voltage; (**b**) drain-source current and voltage of switch S_0; and (**c**,**d**) all diodes' voltage.

Figure 12 shows the measured efficiency of the proposed SC converter when the output power is changed from 80 W to 200 W. The WT230 digital power meter is set up to connect the input and output. The maximum measured efficiency is 93% at 150 W. The efficiency for the experiment can be improved with the optimal selection of components. The experimental results are slightly similar from the theoretical and simulation results.

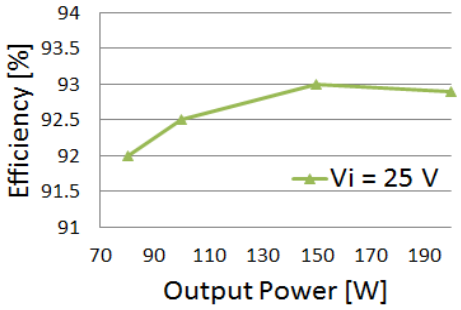


Figure 12. Converter efficiency with different output powers.

Figure 13 shows the voltage gain between the calculated values and simulated values. The simulated values are slightly lower than the calculated values because the parasitics on the devices were set in the simulation.

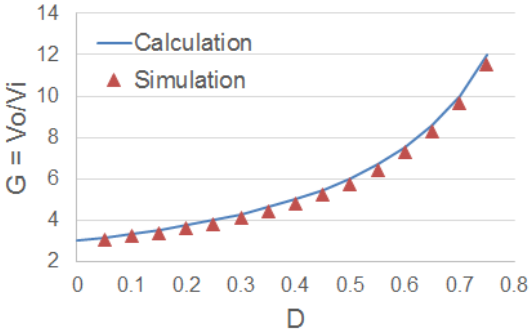


Figure 13. Voltage gain comparison between calculation and simulation.

6. Conclusions

A non-isolated boost DC-DC converter was proposed in this paper. The major advantages of the proposed SC converter are as follows: high voltage gain; decrease voltage and current stress

on the power device, which helps reduce the loss; and being easy to increase the voltage gain and control using one switch. The operating principles in the CCM and DCM, parameters design, power loss analyses, and the comparison with the other non-isolated high boost converters are discussed. The experimental results of the proposed converter at 25 V input voltage are presented to produce the output voltage of 200 V. The maximum measured efficiency of the converter is 93% at 150 W. The experimental and simulation verifications were shown to verify the theoretical analysis.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

B-VMC	Boost voltage multiplier cell
CBC	Cascade boost converter
CCM	Continuous conduction mode
D	Duty cycle
DBC	Dual boost converter
DCM	Discontinuous conduction mode
ESR	Equivalent series resistance
PWM	Pulse width modulation
SC	Switched-capacitor
SCs	Switched-capacitor based
SIESC	Single-inductor-energy-storage cell-based
SLMC	Single inductor multiplier Cuk converter
T	Period time
VMC	Voltage multiplier cells
VMC	Voltage multiplier cells
ZCS	Zero current switching

References

1. Toffoli, F.L.; Pereira, D.C.; Paula, W.J.; Junior, D.S.O. Survey on non-isolated high-voltage step-up DC–DC topologies based on the boost converter. *IET Power Electron.* **2015**, *8*, 2044–2057. [CrossRef]
2. Nymand, M.; Andersen, M.A.E. High-efficiency isolated boost DC–DC converter for high-power low-voltage fuel-cell applications. *IEEE Trans. Ind. Electron.* **2010**, *57*, 505–514. [CrossRef]
3. Jin, K.; Yang, M.; Ruan, X.; Xu, M. Three-level bidirectional converter for fuel-cell/battery hybrid power system. *IEEE Trans. Ind. Electron.* **2010**, *57*, 1976–1986. [CrossRef]
4. Li, W.; He, X. Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications. *IEEE Trans. Ind. Electron.* **2011**, *58*, 1239–1250. [CrossRef]
5. Bratcu, A.I.; Munteanu, I.; Bacha, S.; Picault, D.; Raison, B. Cascaded DC–DC converter photovoltaic systems: power optimization issues. *IEEE Trans. Ind. Electron.* **2011**, *58*, 403–411. [CrossRef]
6. Garcia, F.S.; Pomilio, J.A.; Spiazzi, G. Modeling and control design of the interleaved double dual boost converter. *IEEE Trans. Ind. Electron.* **2013**, *60*, 3283–3290. [CrossRef]
7. Nguyen, M.K.; Lim, L.C.; Choi, J.H.; Cho, G.B. Isolated High Step-up DC-DC Converter Based on Quasi-Switched-Boost Network. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7553–7562. [CrossRef]
8. Ouyang, Z.; Sen, G.; Thomsen, O.C.; Andersen, M.A.E. Analysis and design of fully integrated planar magnetics for primary–parallel isolated boost converter. *IEEE Trans. Ind. Electron.* **2013**, *60*, 494–508. [CrossRef]

9. Nguyen, M.K.; Duong, T.D.; Lim, L.C.; Kim, Y.J. Isolated boost DC–DC converter with three switches. *IEEE Trans. Power Electron.* **2018**, *33*, 1389–1398. [CrossRef]
10. Shi, X.; Jiang, J.; Guo, X. An efficiency-optimized isolated bidirectional DC-DC converter with extended power range for energy storage systems in microgrids. *Energies* **2013**, *6*, 27–44. [CrossRef]
11. Prudente, M.; Pfitscher, L.L.; Emmendoerfer, G.; Romaneli, E.F.; Gules, R. Voltage multiplier cells applied to non-isolated DC-DC converters. *IEEE Trans. Power Electron.* **2008**, *23*, 871–887. [CrossRef]
12. Hsieh, Y.P.; Chen, J.F.; Yang, L.S.; Wu, C.Y.; Liu, W.S. High-conversion-ratio bidirectional DC/DC converter with couple inductor. *IEEE Trans. Ind. Electron.* **2014**, *61*, 1311–1319. [CrossRef]
13. Tang, Y.; Fu, D.; Kan, J.; Wang, T. Dual switches DC/DC converter with three-winding-coupled inductor and charge pump. *IEEE Trans. Power Electron.* **2016**, *31*, 461–469. [CrossRef]
14. Padmanaban, S.; Bhaskar, M.S.; Maroti, P.K.; Blaabjerg, F.; Fedák, V. An original transformer and switched-capacitor (T & SC)-based extension for DC-DC boost converter for high-voltage/low-current renewable energy applications: hardware implementation of a new T & SC boost converter. *Energies* **2018**, *11*, 783. [CrossRef]
15. Tang, Y.; Wang, T.; Fu, D. Multicell switched-inductor/switched-capacitor combined active-network converters. *IEEE Trans. Power Electron.* **2015**, *30*, 2063–2072. [CrossRef]
16. Yang, L.S.; Liang, T.J.; Chen, J.F. Transformerless DC-DC converters with step-up voltage gain. *IEEE Trans. Ind. Electron.* **2009**, *56*, 3144–3152. [CrossRef]
17. Nguyen, M.K.; Duong, T.D.; Lim, L.C. Switched-capacitor-based dual-switch high-boost DC–DC converter. *IEEE Trans. Power Electron.* **2018**, *33*, 4181–4189. [CrossRef]
18. Axelrod, B.; Berkovich, Y.; Ioinovici, A. Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters. *IEEE Trans. Circuits Syst. I* **2008**, *55*, 687–696. [CrossRef]
19. Hernandez, C.A.V.; Maldonado, J.C.M.; Resendiz, J.E.V.; Caro, J.C.R. Modeling and control of an interleaved DC-DC multilevel boost converter. In Proceedings of the IEEE 18th Workshop on Control and Modeling for Power Electronic (COMPEL), Stanford, CA, USA, 9–12 July 2017; pp. 1–6. [CrossRef]
20. Wu, G.; Ruan, X.; Ye, Z. Nonisolated high step-up DC-DC converters adopting switched-capacitor cell. *IEEE Trans. Ind. Electron.* **2015**, *62*, 383–393. [CrossRef]
21. Graovac, D.; Pürschel, M.; Kiep, A. MOSFET power losses calculation using the datasheet parameters. *Infineon Appl. Note* **2006**, *1*, 1–23.