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Low Cost Test Pattern Generation in Scan-Based BIST Schemes

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Abstract: This paper proposes a low-cost test pattern generator for scan-based built-in self-test (BIST) schemes. Our method generates broadcast-based multiple single input change (BMSIC) vectors to fill more scan chains. The proposed algorithm, BMSIC-TPG, is based on our previous work multiple single-input change (MSIC)-TPG. The broadcast circuit expends MSIC vectors, so that the hardware overhead of the test pattern generation circuit is reduced. Simulation results with ISCAS'89 benchmarks and a comparison with the MSIC-TPG circuit show that the proposed BMSIC-TPG reduces the circuit hardware overhead about 50% with ensuring of low power consumption and high fault coverage.

Keywords: test pattern generation; built-in self-test; broadcast circuit; low cost

1. Introduction

Nowadays VLSI testing is always used to ensure the correctness and reliability of the finished chip [1], but we encountered some problems during VLSI testing. In the process of chip testing, the test power consumption is two to four times greater compared with the normal power consumption [2,3]. This excessive power consumption will limit the stability of the circuit and it will also increase the cost of packaging [4]. In consideration of the economics of design for testability, we need to balance the cost and interest [5]. Therefore, this paper aims to find a low-cost test pattern generation method based on our previous work multiple single-input change (MSIC)-TPG [6].

The built-in self-test (BIST) method can effectively reduce the difficulty and complexity of VLSI testing. The BIST technology can be roughly divided into two categories: logic BIST (LBIST) and memory BIST (MBIST) [7,8]. The test pattern generation method proposed in this paper is based on the LBIST method. The traditional LBIST technology is based on the pseudo-random test patterns generated by the linear feedback shift register (LFSR) [9]. This will lead to a large test power consumption during the test. To solve this problem, a method of MSIC test pattern generation combining a pseudo-random sequence with a low-transition sequence has been proposed in paper [6]. It can consider both high fault coverage and low power consumption [10,11]. However, this method increases the area of circuits. To overcome the limitations, a novel low-cost BIST architecture using test pattern broadcast circuits called broadcast-based multiple single input charge (BMSIC)-TPG has been developed. This method reduces the area overhead, and it scores well in power consumption and fault coverage.

The rest of this paper is organized as follows. In Section 2, the proposed BMSIC-TPG scheme is presented. The mathematical features of the new BMSIC sequences is described in Section 3. In Section 4, the performance of the BMSIC sequences are analyzed. Conclusions are given in Section 5.

2. BMSIC-TPG Structure

2.1. BMSIC-TPG

The BMSIC-TPG structure includes a clock control module, an original scan chain generation module, and a broadcast module [12–15], as shown in Figure 1. The square A is the clock control module, which is used to generate a slow clock (CLK1) and a fast clock (CLK2). CLK1 is used to drive LFSR to update seed vectors [16], and CLK2 is used to drive reconstructed Johnson counter to update Johnson vectors and generate the vector J [17]. The square B is the original scan chain generation module, which is composed of the LFSR, the reconfigurable Johnson counter, and the exclusive OR (XOR) network [18]. The LFSR is used to generate the seed vector. The reconfigurable Johnson counter is used to generate the Johnson vector, and the XOR network generates the original scan chain vector by bitwise XOR operation of the seed vector S and the vector J. The square C is the broadcast module, which will broadcast m original scan chains to 4m broadcast scan chains [14]. The specific circuit is shown in Figure 3.

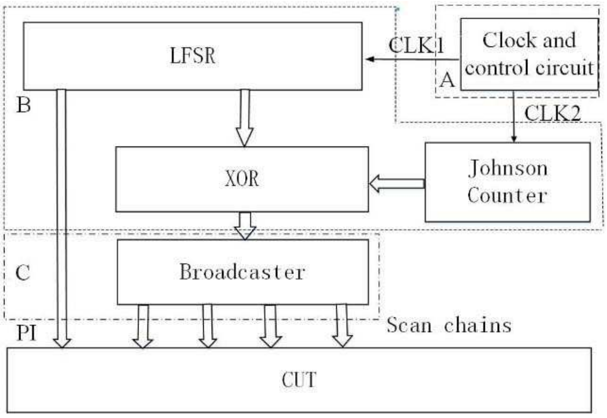


Figure 1. Broadcast-based multiple single input charge (BMSIC)-TPG structure.

Suppose that there are m scan chains before broadcast and M scanning chains after broadcast, and each scanning chain has l scanning cells in a full scan design. The bits of seed vector S generated by LFSR is m. The bits of the vector J generated by reconfigurable Johnson counter is L.

Through many mathematical analyses and experiments, we know the solution to optimize the configuration of BMSIC-TPG is $L = l$, which is called the test convention constraint. Due to test pattern generation algorithm, the test pattern generator is constrained to have $L \geq m$, which is called the test generation constraint, and must be satisfied compared with the test convention constraint. The test convention constraint is an optimal to generate the test pattern under the premise of satisfying the test generation constraint. Obviously, the two constraints are satisfied if $L \geq m$. The configuration is the optimal configuration if $L = l$. If $l < m$, it just satisfies the test generation constraint $L \geq m$ (in this article $L = m$). According to these constraints and the broadcast of test patterns we studied, we can find $M = 4m$, the bits of the seed vector is m, the bits of the Johnson vector is $L(L = l)$, this is the premise of the follow-up contents. The above analysis result is also easy to understand. Under the premise that $L \geq m$, the filling of the scan chain is realized by cyclic shifting of the updated current Johnson vector. The period of the cyclic shift is L. If $L < l$, the cyclic shift of the Johnson vector needs several shifting cycles, and the filling value will correspondingly appear repetitive parts. So the possibility of transition between adjacent bits of vectors generated after encoding will increase. If $L = l$, the cyclic shift of the Johnson vector is exactly a shift period, and the filled value is just all the bits of the Johnson vector. So this configuration can ensure low possibility of transition. If $L > l$, the cyclic shift of the Johnson vector is less than one shift period, and the filling value is part of the bits of Johnson vector. Thus, the possibility of transition will decrease. But this configuration will increase the area of the circuits. In this paper, the bits of seed vector and Johnson vector are always equal which is called the same scan configuration.

2.2. LFSR Structure and Johnson Counter Structure

The LFSR is composed of multiple shift registers and XOR gates connected in a certain way. The m-bit linear feedback shift register can generate $(2^m - 1)$ different states at most [19]. If the m-bit linear feedback shift register generates $(2^m - 1)$ different states and begins to repeat periodically, the $(2^m - 1)$ different states of the sequence is called the maximum length sequence, which is also known as the M sequence.

Because the number of transitions between adjacent bits of the test vector is positively correlated with the power consumption of the test [20], the Johnson counter can generate Johnson vectors that has low transition properties between adjacent vectors and adjacent bits of the same vector. The Johnson sequence is a single input change sequence (SIC). The vector generated by the next clock in the sequence is a one-bit change from the previous clock generation vector. Johnson sequences consist of a series of "0" and a series of "1". So we choose a Johnson counter to reduce power consumption. But a simple Johnson counter can not complete the data shift loading process. We reconstruct the Johnson counter according to the test pattern generation method.

The L-bit reconfigurable Johnson counter is shown in Figure 2. When the mode is set to one, the counter implements the counting function. Under this mode, the initialization of all flip-flops will be completed after running L clocks if the Rst signal is set to zero. If the Rst signal is set to one, the counter implements the normal counting function. When the mode is set to zero, the counter implements a shift function and feeds the last bit of the counted vector back to the first bit. The adjacent bit of each Johnson vector jumps to zero or one, so the sequence generated by the reconfigurable Johnson counter still holds the single-hop characteristic.

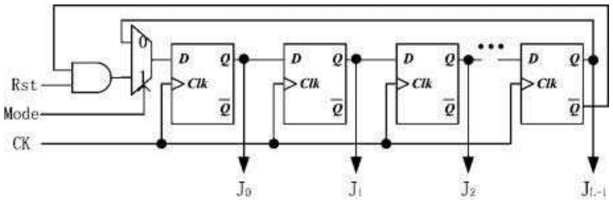


Figure 2. L-bit reconfigurable Johnson counter structure.

2.3. XOR Network

The XOR network generates the original scan chain vector by bitwise XOR operation of the seed vector S which is generated by the LFSR and the vector J which is generated by the reconfigurable Johnson counter. The LFSR generates an m-bit seed vector $S = [S_0, S_1, S_2, \ldots, S_{m-1}]$. The reconfigurable Johnson counter generates a L-bit vector $J = [J_0, J_1, J_2, \ldots, J_{L-1}]$. The result of the bit-wise XOR operation is $X = [X_1, X_{L+1}, X_{2L+1}, \ldots, X_{(m-1)L+1}]$.

2.4. Broadcaster

A broadcaster [12–14] distributes test patterns from a MSIC-TPG [6] module to fill multiple scan chains in a minimally constrained manner. The specific structure is shown in Figure 3. The broadcast circuit extends the original scan chains from two to eight. S_1 and S_2 are original scan chains. B_0 and B_1 are broadcast vectors which are generated by the two-bit LFSR. The post-broadcast seed vectors S_{11}, S_{12}, S_{13}, S_{14} and S_{21}, S_{22}, S_{23}, S_{24} to be applied to the scan chains are generated by bit-XOR the original scan chains S_1 and S_2 and the broadcast vectors B_0 and B_1. Suppose the number of original scan chains is m, so the number of seed vectors after broadcast is M and $M = 4m$.

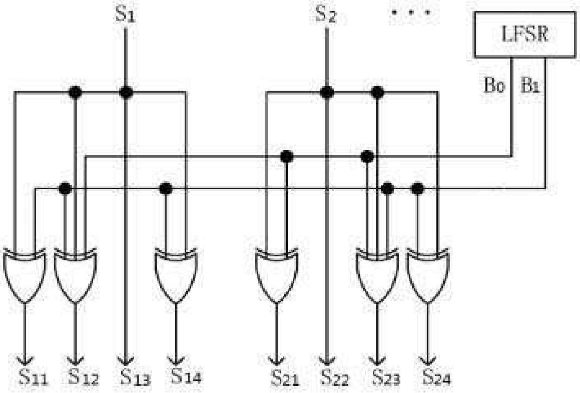


Figure 3. Broadcast circuit.

2.5. The Process of BMSIC-TPG

What follows are the operation mode of the BMSIC-TPG.

1. Clock control module generates CLK1 and CLK2. CLK1 drives the LFSR to update the seed vector, and CLK2 drives the reconfigurable Johnson counter to update the J vector and enables the scan to move in.
2. Original scan chain generation module is made up of the LFSR, reconfigurable Johnson counter, and XOR network. The LFSR generates the S vector. The reconfigurable Johnson counter generates the J vector. The XOR network operates the bit-XOR between the S vector and the J vector to generate the original scan chain data.
3. Broadcast module is used to extend the original scan chain.

3. BMSIC-TPG Mathematical Features

3.1. Periodicity

Since the seed vectors, broadcast vectors, and original scan chain vectors before the broadcast are all periodic and the XOR operation is a linear operation, the BMSIC test pattern is also assumed to have periodic characteristics [6]. Suppose the seed vector is $S = [S_0, S_1, S_2, \ldots, S_{m-1}]$. The vector J is $J = [J_0, J_1, J_2, \ldots, J_{L-1}]$, and the broadcast vector B is $B = [B_0, B_1]$. Then at time t, S, J, and B can be expressed as:

$$\begin{aligned}
\mathbf{S}(t,x) &= S_0(t)x^0 + S_1(t)x^1 + \ldots + S_m(t)x^m \\
\mathbf{J}(t,x) &= J_0(t)x^0 + J_1(t)x^1 + \ldots + J_{L-1}(t)x^{L-1} \\
\mathbf{B}(t,x) &= B_0(t)x^0 + B_1(t)x^1.
\end{aligned} \tag{1}$$

According to the generation algorithm, the original input test vector consists of parts or all bits of the seed vector or multiplexing of seed vectors, which can be expressed as:

$$\begin{aligned}
\mathbf{V}_{in}(t,x) = {} & S_0(t)x^0 + S_1(t)x^1 + \ldots + S_{m-1}(t)x^{m-1} + \\
& S_0(t)x^m + S_1(t)x^{m+1} + \ldots + S_{m-1}(t)x^{2m-1} + \ldots + S_h(t)x^{N-1}.
\end{aligned} \tag{2}$$

In Equation (2), $1 \le h \le m$ and h is an integer. The specific value depends on the number of the original inputs N and the number of seed vectors m. At the same time, the k-th original scan chain vector can be expressed as:

$$\mathbf{C}_k(t,x) = [\sum_{i=0}^{L-1} S_{k-1}(t)x^i \oplus J_k(t,x)]x^{N+(k-1)L}. \tag{3}$$

The vector in Equation (3) represents the J vector applied to the k-th scan chain.

Assume that the two pre-broadcast original scan chain vectors S_1, S_2 of the broadcaster shown in Figure 3 are denoted as $C_q(t,x)$, $C_{q+1}(t,x)$. The test vector of the i-th scan chain after broadcasting is $V_i(t,x)$, then the eight scan chain vectors S_{11}, S_{12}, S_{13}, S_{14}, S_{21}, S_{22}, S_{23}, S_{24} after broadcasting can be expressed as:

$$\begin{aligned}
\mathbf{S}_{11} &= V_{4q-3}(t,x) = C_q(t,x) \oplus \sum_{j=1}^{L} B_1(t)x^j \\
\mathbf{S}_{12} &= V_{4q-2}(t,x) = C_q(t,x) \oplus \sum_{j=1}^{L}[B_0(t) \oplus B_1(t)]x^j \\
\mathbf{S}_{13} &= V_{4q-1}(t,x) = C_q(t,x) \\
\mathbf{S}_{14} &= V_{4q-3}(t,x) = C_q(t,x) \oplus \sum_{j=1}^{L} B_0(t)x^j \\
\mathbf{S}_{21} &= V_{4q+1}(t,x) = C_{q+1}(t,x) \oplus \sum_{j=1}^{L} B_0(t)x^j \\
\mathbf{S}_{22} &= V_{4q+2}(t,x) = C_{q+1}(t,x) \\
\mathbf{S}_{23} &= V_{4q+3}(t,x) = C_{q+1}(t,x) \oplus \sum_{j=1}^{L}[B_0(t) \oplus B_1(t)]x^j \\
\mathbf{S}_{24} &= V_{4q+4}(t,x) = C_{q+1}(t,x) \oplus \sum_{j=1}^{L} B_1(t)x^j.
\end{aligned} \tag{4}$$

Considering the above, the ω complete scan chain vector loaded into the circuit under test can be expressed as:

$$\mathbf{P}(\omega) = P(t_\omega, x) = V_{in}(t_\omega, x) + \sum_{i=1}^{M} V_i(t_\omega, x). \tag{5}$$

Bit-XOR the ωth test pattern with the dth test pattern can be expressed as:

$$\mathbf{P}(\omega) \oplus \mathbf{P}(d) = V_{in}(t_\omega, x) \oplus V_{in}(t_d, x) + \sum_{i=1}^{M}[V_i(t_\omega, x) \oplus V_i(t_d, x)]. \tag{6}$$

Only if $S(t_\omega, x) = S(t_d, x)$, $B(t_\omega, x) = B(t_d, x)$, and $\sum_{l=1}^{m} C_l(t_\omega, x) = \sum_{l=1}^{m} C_l(t_d, x)$ are established at the same time, then $\mathbf{P}(\omega) \oplus \mathbf{P}(d) = 0$ is established. It is known that the period of seed vector S is $T_S = 2^m - 1$. The period of the broadcast vector B is $T_B = 2^2 - 1 = 3$. It is known from the literature [6] that the period of original scan chain vector S before broadcast is $T_{MSIC} = (2^m - 1)2L$. So the BMSIC test pattern is also periodic, and the period is the least common multiple of the period of seed vector, the broadcast vector and the original scan chain vector. It can be expressed as:

$$\mathbf{T}_{BMSIC} = \begin{cases} (2^m - 1)2L & (T_{MSIC}\%3 = 0) \\ (2^m - 1)6L & (T_{MSIC}\%3 \neq 0). \end{cases} \tag{7}$$

From Equation (7), the period of the BMSIC test pattern is related to the number of bits of the seed vector and the J vector. Under the same configuration, the T_{BMSIC} is larger than the T_{MSIC} [6]. The greater the period of the test pattern is, the better the pseudo-randomness of the test pattern sample is, and the higher the fault coverage is. The number of bits in the seed vector S and J vectors directly affects the hardware overhead. The exponential relationship and multiple relationship of the Equation (7) make it possible to obtain a test pattern with large period and good pseudo-randomness with fewer vector bits, so BMSIC test patterns can reduce hardware overhead on the premise of achieving satisfactory fault coverage.

3.2. Transition

The number of transitions between adjacent bits of the test pattern is positively correlated with the power consumption of the test [20], so it can be used to quantitatively analyze the transition properties of the BMSIC test pattern. We take some test patterns under different scanning configurations as the samples and count the transition numbers for the BMSIC test generation method. We have obtained some statistical laws after our analysis. The results are shown in Table 1, and the "transition period" indicates how many test patterns the transition characteristics will repeat. "Pattern transitions" indicates the total transitions of a single test pattern.

Table 1. Transition of the broadcast-based multiple single input charge (BMSIC)-TPG.

Seed Vector Bits	Johnson Vector Bits	Transition Period	Pattern Numbers	Pattern Transitions
8	8	8	1 7	0 56
8	17	17	1 8 8	0 60 64
8	20	20	1 8 11	0 60 64
10	10	10	1 9	0 90
10	36	36	1 10 25	0 76 80
10	44	44	1 10 33	0 76 80

We can make a conclusion from Table 1: (1) the transitions of per test pattern repeats with L for the transition period. (2) If $L = m$, the transition of one pattern is zero, and the transition of $L - 1$ patterns is $8(m-1)$. (3) If $L > m$, the transition of one pattern is zero. The transition of m patterns is $8(m-1)+4$, and the transition of $(L-m-1)$ patterns is $8m$. The above conclusion is derived because the BMSIC test pattern needs to satisfy both the test generation constraints and the test convention constraints. The average transition between the adjacent slices of the BMSIC test pattern is calculated as Equation (8), which is almost equivalent to the average transition of the MSIC [4] test pattern (shown in Equation (9)).

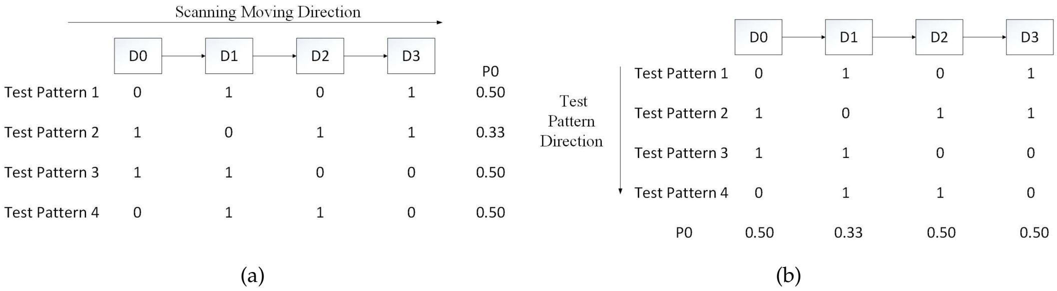
$$\mathbf{C}_{BMSIC\_ave} = \begin{cases} \frac{8(m-1)}{L} & (L = m) \\ \frac{8m(L-1)-4m}{L(L-1)} & (L > m). \end{cases} \tag{8}$$

$$\mathbf{C}_{MSIC\_ave} = \begin{cases} \frac{2(M-1)}{L} & (L = m) \\ \frac{2M(L-1)-M}{L(L-1)} & (L > m). \end{cases} \tag{9}$$

3.3. Randomness

The random sequence can detect most of the faults in CUT. Therefore, this paper discusses the randomness of the "0", "1" distribution of BMSIC test patterns that have been generated to evaluate its capability to detect faults. The generated test pattern is evaluated from the scanning moving direction and the test pattern direction respectively according to the scanning test scheme and the scanning design technique.

As shown in Figure 4a, the randomness of scan moving direction is to calculate the probability of “0” or “1” of a given scan chain under each test pattern, which reflects the randomness of the same test pattern between its scan units on this scan chain. However, the randomness of scan moving direction does not reflect the randomness of the same scanning unit in the designated scan chain being filled with “0” or “1” under different test patterns, thus introducing the randomness of test pattern direction as shown in Figure 4b. The randomness of test pattern direction is to calculate the probability of “0” or “1” being filled in different test patterns for each scan unit in the specified scan chain, which reflects the difference between test patterns. We take 10,000 BMSIC test patterns and each test pattern has 32 scan chains as the samples and choose one chain to study. Then compare with LFSR and MSIC test patterns in the same configuration to reflect the performance of randomness. Other chains also has the similar result. The probability distribution of logic “0” in the scan moving direction is shown in Figure 5. It can be concluded BMSIC has a large fluctuation in randomness and has periodicity. The probability distribution of logic “0” in the test pattern direction is shown in Figure 6. It can be concluded the randomness of the test sequence arranged from good to bad is MSIC, BMSIC and LFSR, but the distributions are basically between 0.495 and 0.505, all have good randomness. So we consider the BMSIC test patterns have good fault detection capability.



	D0	D1	D2	D3	P0
Test Pattern 1	0	1	0	1	0.50
Test Pattern 2	1	0	1	1	0.33
Test Pattern 3	1	1	0	0	0.50
Test Pattern 4	0	1	1	0	0.50

	D0	D1	D2	D3
Test Pattern 1	0	1	0	1
Test Pattern 2	1	0	1	1
Test Pattern 3	1	1	0	0
Test Pattern 4	0	1	1	0
P0	0.50	0.33	0.50	0.50

Figure 4. (**a**) Scan moving direction randomness analysis diagram. (**b**) Test pattern direction randomness analysis diagram.

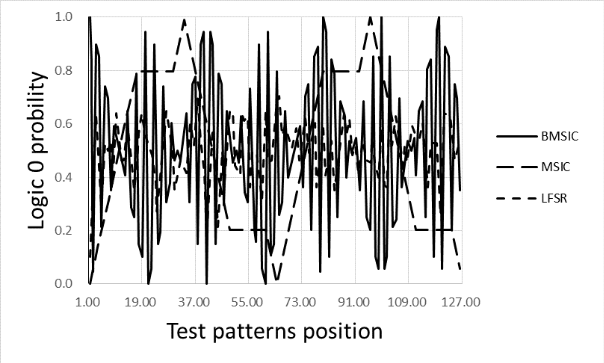


Figure 5. Scan moving direction Logic “0” probability distribution.

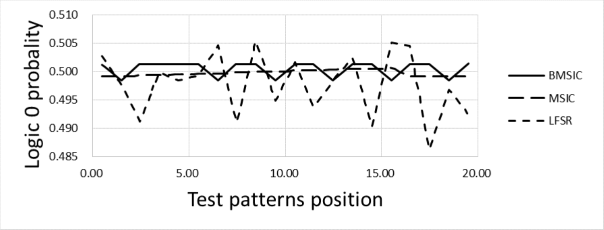


Figure 6. Test pattern direction Logic “0” Probability distribution.

The above analysis shows that BMSIC test patterns are good in randomness. Although it is based on a statistical approximation, it is necessary to evaluate the fault detection capability of test pattern. Therefore, it is speculated that BMSIC test patterns can achieve satisfactory fault coverage.

4. BMSIC-TPG Performance Analysis

BMSIC test patterns had low power consumption and low area overhead and it can achieve satisfactory fault coverage from theoretical analysis. This section verifies its fault coverage, power consumption, and area cost performance through the specific simulation experiments and performance estimates. The circuit under test (CUT) in the experiment are five circuits in ISCAS'89 series, using Nangate 45 nm process library. The synthesis of CUT were carried out with DFT_Compiler of Synopsys. Test generation and test application were carried out with Perl. The fault simulation was carried out with TetraMAX. The power consumption simulation was carried out with the Synopsys Design Analyzer and Prime Power. Because the BMSIC-TPG proposed in this paper was designed to overcome the drawback of the previous method [6], we compare the performance of BMSIC with our previous method [6].

4.1. Fault Simulation

The fault simulation results of the BMSIC test generation method are shown in Table 2. DFF represents the number of scanning units in the circuit under test. Chain represents the number of scan chains. Depth represents the number of scanning units per scan chain. TL represents the number of test patterns, and SFC and TFC represent stuck fault coverage and transition fault coverage respectively.

We used DFT_Compiler of synopsys to synthesize the CUT, Perl to implement test patterns generation algorithm to achieve test generation, test application, and TetraMAX to complete the fault simulation, the results are shown in Table 2. Comparing with the literature [6], BMSIC test program can achieve higher fault coverage under the same configuration. Comparing with the literature [21], we needed less test patterns to achieve high fault coverage. At the same time, we found that the same CUT under different test generation configuration resulted in different fault coverage, indicating that the fault coverage is related to test generation configuration.

Table 2. Comparison of fault coverage of the three test generation methods.

CUT	DFF	Chain	Depth	TL	LFSR		MSIC [6]		BMSIC	
					SFC	TFC	SFC	TFC	SFC	TFC
S13207	638	32	20	10,000	91.44	80.75	90.51	74.3	91.42	74.02
		36	18	10,000	92.01	80.33	86.63	71.11	92.6	73.57
		40	16	10,000	95.24	84.05	89.22	70.82	93.52	77.71
S15850	534	32	17	10,000	93.9	85.55	92.01	78.36	89.45	75.12
		36	15	10,000	93.82	85.55	91.23	76.79	91.79	77.01
		40	14	10,000	94.69	86.59	90.11	73.19	93.59	80.60
S35932	1728	40	44	10,000	99.55	97.04	97.34	86.28	99.97	95.99
		48	36	10,000	99.60	96.66	99.94	93.99	99.98	92.04
		56	31	10,000	99.56	96.34	97.77	88.7	99.98	94.53
S38417	1636	40	41	10,000	93.48	83.67	83.69	59.11	84.65	60.4
		48	35	10,000	93.68	83.18	85.33	61.68	85.22	61.58
		56	30	10,000	93.66	82.87	84.34	61.09	83.46	52.74
S38584	1426	40	36	10,000	95.99	90.51	93.39	76.6	97.32	81.31
		48	30	10,000	96.01	90.99	95.36	82.4	98.00	84.67
		56	26	10,000	97.17	92.15	95.23	82.11	98.16	90.04

4.2. Power Consumption Simulation

The power simulation results of the BMSIC test generation method are shown in Table 3. The test frequency was 100 MHz, and the power supply voltage was 1.1 V. Table 3 shows the total power consumption and peak power consumption caused by the three test generation methods: LFSR, MSIC, and BMSIC. From Table 3, the BMSIC test pattern generation circuit has obvious advantages in terms of the total power consumption and the peak power consumption compared with the LFSR generation method. The MSIC generation method was better in power consumption compared with BMSIC generation method. But the difference is not particularly obvious.

Table 3. Comparison of power simulation results of the three test generation methods.

CUT	DFF	Chain	Depth	Primepower					
				Total (μ*W*)			Peak (μ*W*)		
				LFSR	MSIC [6]	BMSIC	LFSR	MSIC [6]	BMSIC
S13207	638	32	20	116.61	105.89	107.78	6891.83	5535.75	5582.29
		36	18	116.39	104.75	107.72	6818.38	5737.82	5617.09
		40	16	116.59	104.51	108.20	7337.72	5536.47	5617.74
S15850	534	32	17	109.26	96.4	99.31	6633.73	5137.78	5429.68
		36	15	108.59	95.13	99.41	6518.92	5026.07	5396.98
		40	14	109.09	94.8	99.13	6656.53	5442.83	5345.9
S35932	1728	40	44	320.86	276.83	272.26	20,835.3	17,317.1	19,303.6
		48	36	322.54	275.91	277.25	21,014.8	14,695.9	19,864.5
		56	31	322.22	274.54	282.07	21,380.5	25,411.3	20,922.4
S38417	1636	40	41	347.57	280.81	286.98	20,349.8	17,630.4	17,503.9
		48	35	347.32	282.52	286.92	20,578.5	17,081.9	16,952.8
		56	30	346.68	280.41	289.17	19,979	17,425.5	17,150.1
S38584	1426	40	36	335.26	286.89	292.9	21,125.5	15,583.2	18,163.6
		48	30	335.46	287.13	293.95	20,058.9	15,768.9	17,835.2
		56	26	335.43	285.67	291.39	20,011.9	16,110.7	15,692.3

4.3. Area Overhead Evaluation

The hardware area cost of the three test patterns are shown in Table 4. The unit is the area of a two-input XOR gate. The "reduction" indicates the percentage reduction in area of BMSIC compared with MSIC. From the analysis of Table 4, BMSIC method had a great advantage in an equivalent scan configuration, and it can reduce the area overhead by about 50% in the best case.

Table 4. Area Overhead Comparison of the three test generation methods.

CUT	Chain	Depth	LFSR			MSIC [6]			BMSIC			Reduction (%)
			S	L	Area	S	L	Area	S	L	Area	
S13207	32	20	32	0	94	32	32	218	8	20	131	39.9
	36	18	36	0	103	36	36	243	9	18	131	46.09
	40	16	40	0	116	40	40	271	10	16	133	50.92
S15850	32	17	32	0	94	32	32	218	8	17	122	44.04
	36	15	36	0	103	36	36	243	9	15	122	49.79
	40	14	40	0	116	40	40	271	10	14	127	53.14
S35932	40	44	40	0	116	40	44	283	10	44	212	25.09
	48	36	48	0	139	48	48	325	12	36	207	36.31
	56	31	56	0	161	56	56	378	14	31	209	44.71
S38417	40	41	40	0	116	40	41	274	10	41	204	25.55
	48	35	48	0	139	48	48	325	12	35	205	36.92
	56	30	56	0	161	56	56	378	14	30	206	45.5
S38584	40	36	40	0	116	40	40	271	10	36	190	29.89
	48	30	48	0	139	48	48	325	12	30	190	41.54
	56	26	56	0	161	56	56	378	14	26	195	48.41

5. Conclusions

This paper proposes a low-cost test pattern generation method BMSIC-TPG based on our previous work MSIC-TPG, which can take into account both low power consumption and satisfactory fault coverage [6]. The hardware overhead of the proposed MSIC-TPG is reduced by inserting a broadcaster between the MSIC-TPG module and the CUT. The inserted broadcaster is responsible for distributing test patterns from a MSIC-TPG module to fill a larger number of scan chains. By the introduction of the broadcaster, one original scan chain can be split into several shorter scan chains in a balanced way. Analysis results show that BMSIC sequences have the favorable features of uniform distribution and low input transition density. Compared with MSIC-TPG, experimental results show that in most cases, hardware overhead is reduced by 50% and fault coverage is higher. This is achieved with a little increase in test power and no increase in test length to hit a target fault coverage. For the larger CUT, the performance of the proposed BMSIC-TPG in area overhead is better.

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