Article

Series-Connected High Frequency Converters in a DC Microgrid System for DC Light Rail Transit

Bor-Ren Lin

Department of Electrical Engineering, National Yunlin University of Science and Technology, Yunlin 640, Taiwan; linbr@yuntech.edu.tw; Tel.: +886-9-1231-2281

Received: 7 January 2018; Accepted: 18 January 2018; Published: 23 January 2018

Abstract: This paper studies and presents a series-connected high frequency DC/DC converter connected to a DC microgrid system to provide auxiliary power for lighting, control and communication in a DC light rail vehicle. Three converters with low voltage and current stresses of power devices are series-connected with single transformers to convert a high voltage input to a low voltage output for a DC light rail vehicle. Thus, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with a low voltage rating and a turn-on resistance are adopted in the proposed circuit topology in order to decrease power losses on power switches and copper losses on transformer windings. A duty cycle control with an asymmetric pulse-width modulation is adopted to control the output voltage at the desired voltage level. It is also adopted to reduce switching losses on MOSFETs due to the resonant behavior from a leakage inductor of an isolated transformer and output capacitor of MOSFETs at the turn-on instant. The feasibility and effectiveness of the proposed circuit have been verified by a laboratory prototype with a 760 V input and a 24 V/60 A output.

Keywords: DC microgrid; zero-voltage switching; half-bridge converter; light rail transit

1. Introduction

Direct current (DC) microgrids are studied to combine alternative current (AC) utility power, renewable energy sources, energy storage units and local DC and AC loads in order to reduce global warming and climbing temperature issues. The common DC voltage on DC microgrids can be 1500 V for traction vehicles; 760 V for light rail vehicles and industry applications; 380 V for residential and commercial buildings. For light rail transits, low frequency power transformers are used in conventional light rail vehicles to provide electrical isolation. The main drawback of line frequency transformers [1–3] is bulk volume. To avoid using bulky line frequency transformers, transformerless converter topologies [4–8] with primary-series and secondary-parallel connections have been proposed to lessen the blocking-voltage capability of active devices on the high voltage side and the current stress of power components on the low voltage side. Half-bridge (HB) or full-bridge (FB) converters have been widely adopted for medium power applications to provide a stable and low voltage output. Conventional FB converters and HB converters using high voltage rating devices such as insulated gate bipolar transistors (IGBTs) are widely adopted to convert a high voltage input to a low voltage output. However, the switching frequency of general IGBT devices is less than 50 kHz. To improve the low switching frequency problem of IGBT devices, multilevel converters [9–11] using Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices have been developed in medium power converters to reduce converter volume. However, the high switching frequency will also increase core losses on magnetic components and switching losses on power MOSFETs. Zero-voltage switching converters [12–15] have been proposed to achieve a low switching loss. Asymmetric pulse-width modulation [16–18], frequency modulation [19–21] and a phase-shift pulse-width modulation (PWM) scheme [22–24] are general PWM control schemes used in DC/DC converters to regulate load voltage.
and also realize the mechanism of the zero-voltage turn-on switching. Therefore, the high efficiency converters can be obtained. The asymmetrical PWM scheme can reset the magnetizing flux in every switching cycle. Therefore, the voltage spike on drain-to-source of power MOSFET can decrease the safety operation region and the electromagnetic interference can be reduced.

This paper presents a series-connected soft switching converter using a single transformer for light rail vehicle applications. The adopted circuit topology includes three series-connected HB circuits on the primary side to reduce the blocking-voltage stress of power MOSFETs. Thus, low turn-on resistance and low voltage rating MOSFETs can be adopted to lessen conduction losses on power devices. The input split voltage balance is achieved by two flying capacitors. The asymmetric PWM scheme is employed to control power switches. The output capacitor of power MOSFETs and the leakage inductor of the transformer are resonant at the transition interval. Thus, the mechanism of the zero-voltage turn-on switching is realized and the electromagnetic interference can be reduced. Current doubler rectifier topology is used on the low voltage side to achieve a ripple current cancellation. Therefore, the resultant ripple current at the output capacitor is reduced. Three HB circuits share one transformer on the primary side so that the primary currents of the three HB circuits are reduced to one-third of the primary current in a conventional HB converter. Therefore, the conduction losses on active switches are reduced and the circuit efficiency is improved. The feasibility of the proposed circuit is verified with a 1.44 kW converter. This paper is organized as follows: in Section 2, the circuit configuration and operation principle of the developed converter used in the DC microgrid are presented and discussed in detail. In Section 3, the circuit characteristics of the developed circuit are presented. Experimental results based on a laboratory prototype are shown and discussed in Section 4. Finally, Section 5 presents the conclusions.

2. Proposed Converter

The basic circuit structure of a DC microgrid is given in Figure 1. The bidirectional AC/DC converters are used between the AC utility system and the DC microgrid to stabilize the DC bus voltage. Renewable energy sources from solar cell panels and wind power generators provide clear energy to the DC microgrid system through the unidirectional DC/DC converters and the AC/DC converters. Energy storage units are used to store/release energy from/to the DC microgrid through the bidirectional DC/DC converters in order to stabilize the DC bus voltage. In order to increase the voltage reliability, the bipolar voltage system (+$V_{dc}$, $V_{dc}$, and neutral line) can be adopted on the DC microgrid. When a fault condition in one of the DC poles occurs, the DC power is still supplied to the local load by the other two wires and an auxiliary converter. It is clear that the reliability of the DC microgrid system is increased during fault condition. Therefore, three voltage levels (2$V_{dc}$, +$V_{dc}$ and −$V_{dc}$) can be used to provide industry and transportation with the 2$V_{dc}$ voltage level and future residential and commercial buildings with the +$V_{dc}$ or −$V_{dc}$ voltage level. To keep two voltage levels (+$V_{dc}$ and −$V_{dc}$) balanced during unbalanced loads, a voltage balancing circuit is normally needed to realize this goal. The DC/DC converter can be used to convert a high input voltage to a low output voltage and it does not relate to the bipolar voltage system. For a DC light rail vehicle, the input voltage is normally around 760 V. Power devices such as the 1500 V IGBT can be adopted in two-level power converters to supply auxiliary low voltage power for control units, telecommunication units and lighting systems in the light rail vehicle. The MOSFETs with a 600 V rating can be adopted in the three-level power converter to achieve the same goal but with a much higher switching frequency to reduce converter size. The studied converter is concentrated on power conversion for light rail vehicle applications. Figure 2a shows the basic block diagrams of power distribution in a conventional light rail vehicle. First, 750 $V_{dc}$ is converted to the three-phase AC voltage 380 $V_{ac}$ by the DC/AC inverter. Second, the AC/DC converter is adopted to convert 380 $V_{ac}$ to a low DC voltage in an auxiliary power distribution system to supply a necessary amount of DC voltage for the battery bank, lighting equipment, door equipment, control power units and communication equipment in a light rail vehicle system. The AC/DC/AC converter is also adopted to convert 380 $V_{ac}$ to a variable
AC voltage output for the AC motor drive. If the power of the DC light rail vehicle is supplied directly from the DC microgrid, then some power conversion stages can be saved to reduce costs and increase circuit efficiency. The basic power distribution diagrams in the proposed light rail vehicle are illustrated in Figure 2b. The auxiliary power in a light rail vehicle is directly converted from 760 V through a DC/DC converter. The AC motor drive and the air compressor are controlled by the DC/AC converters. Therefore, the AC/DC conversion can be saved to reduce costs and increase circuit efficiency and reliability.

Figure 1. Basic circuit structure of a DC microgrid.

Figure 2. Light rail transit. (a) Block diagram of the power distribution in a conventional light rail vehicle; (b) block diagram of the power distribution in the studied light rail vehicle.

The studied DC/DC converter is given in Figure 3. It directly converts a 760 V voltage input from the DC microgrid to a low voltage output by using low voltage rating power MOSFETs to provide auxiliary power in a light rail vehicle. The studied converter includes three HB circuits connected in a primary-series secondary-parallel with a single transformer. The primary sides of the HB circuits are connected in a series so that the voltage stress of the power switches Q1~Q6 is reduced to \( \frac{V_{in}}{3} \) and
the low turn-on resistance of power MOSFETs is adopted to reduce conduction losses and increase circuit efficiency. Each HB circuit provides \( P_i / 3 \) to the output load. Flying capacitors are widely used in a multilevel inverter to reduce voltage stress and balance input split voltages. Thus, two flying capacitors \( C_f1 \) and \( C_f2 \) are used on the high voltage side to achieve an input voltage balance of \( V_{C1} \sim V_{C3} \). The current doubler rectifier is used on the low voltage side to reduce the output ripple current. The driving signals of each HB circuit use asymmetric pulse-width modulation. Due to the resonant behavior between the output capacitor of the power MOSFETs and the primary leakage inductor at switch on/off instant, the power MOSFETs can be turned on at zero-voltage switching to reduce the switching loss. Figure 4 shows the timing sequence of switches \( Q_1 \sim Q_6 \) and the main PWM waveforms in the proposed converter. The operation principle and circuit analysis of the studied circuit are assumed under the following conditions: (1) the output capacitor \( C_o \) is large enough to be treated as a constant voltage \( V_o \), (2) power devices \( Q_1 \sim Q_6, D_1 \) and \( D_2 \) are ideal, (3) \( C_f1 = C_f2 = C_f, C_b1 = C_b2 = C_b3 = C_b, L_{r1} = L_{r2} = L_r \), and \( L_{m1} = L_{m2} = L_{m3} = L_m \), (4) \( n_1 = n_2 = n_3 = n_p / n_{ns} \), and (5) \( V_{Cb1} = V_{Cb2} = V_{Cb3} = V_{Cb} \) and \( V_{C1} = V_{C2} = V_{C3} = V_{Cf1} = V_{Cf2} = V_{Cf} \). The duty cycles of \( Q_1, Q_3 \) and \( Q_5 \) are \( d \). Conversely, the duty cycles of \( Q_2, Q_4 \) and \( Q_6 \) are \( 1 - d \). The equivalent circuits of the operating steps in the proposed circuit are shown in Figure 5. There are eight operating stages for every switching period.

![Figure 3. Circuit schematic of the studied converter.](image)

![Figure 4. Main waveforms during one switching period.](image)
**Step 1 [t0−t1]:** Before step 1, power switches Q1, Q3 and Q5 are conducting and the output current freewheels through D1 and D2. After time t0, iD1 is decreased to zero and D1 becomes reverse biased. i0 flows through D2. Power is transferred from V_in to R0 in this step. In step 1, V_C1 = V_C1, V_C2 = V_C2, V_Q2,ds = V_C1, V_Q4,ds = V_C2, V_Q6,ds = V_C3, v_Lm1 ≈ V_C1 - v_Cb1, v_Lm2 ≈ V_C2 - v_Cb2, v_Lm3 ≈ V_C3 - v_Cb3, v_La1 ≈ |V_C1 - v_Cb1|/n1 - V_o and v_La2 = -V_o. Thus, i_p1−i_p3 and i_La1 increase and i_La2 decreases. Since all circuit components in three HB circuits are identical and n1 = n2 = n3 = n_p/n_o, it can obtain v_Lm1 = v_Lm2 = v_Lm3 = n_v_F and i_p1 = i_p2 = i_p3 ≈ i_La0/(3n1). Since i_La1 increases and i_La2 decreases in this step, the ripple current of i_La1 + i_La2 is reduced.

**Step 2 [t1−t2]:** When Q3, Q1 and Q5 are turned off at time t1; the positive primary currents i_p1−i_p3 rapidly discharge C_Q2, C_Q4 and C_Q6, respectively. On the other hand, C_Q1, C_Q3 and C_Q5 are charged by i_p1−i_p3 respectively. The secondary winding voltage v_ms is decreased in this step.

**Step 3 [t2−t3]:** When C_Q2, C_Q4 and C_Q6 are discharged to v_Cb1, v_Cb2 and v_Cb3 respectively, then the secondary winding voltage v_ms = 0. Then the output current i0 freewheels through D1 and D2.

In this operation step, v_La1 = v_La2 = -V_o and i_La1 and i_La2 decrease.

**Step 4 [t3−t4]:** At time t3, C_Q2, C_Q4 and C_Q6 are discharged to zero voltage. Since i_p1(t3)−i_p3(t3) are all positive, the body diodes D_Q2, D_Q4 and D_Q6 are forward biased. Therefore, Q2, Q4 and Q6 can be turned on at this moment to realize a zero-voltage turn-on. Because i0 is still freewheeling through D1 and D2, it can obtain v_ms = 0, v_La1 = v_La2 = -V_o, v_Lr1 = -v_Cb1, v_Lr2 = -v_Cb2 and v_Lr3 = -v_Cb3. i_p1−i_p3, i_La1 and all i_La2 decrease. This step is ended when i_D2 = 0. During this freewheeling interval, the currents i_Lr1−i_Lr3 are decreased from i_La0/(3n1) to -i_La2/(3n1) and the current variation on L_r1−L_r3 is about i_Lo/(3n1). The duty loss in step 4 is obtained as (1) shows:

\[
d_{loss4} = \frac{\Delta t_{34}}{T_{sw}} = \frac{I_o L_{rs}}{3n_1 V_{C_b1}} \tag{1}
\]

**Step 5 [t4−t5]:** After t4, i_D2 is decreased to zero so that D2 is reverse biased. i0 flows through D1, L_o1 and L_o2. In step 5, power is transferred from V_in to R0, V_C1 = V_C2, V_C2 = V_C3, v_Q3,ds = V_C1, v_Q3,ds = V_C2, v_Q5,ds = V_C3, v_Lm1 ≈ -v_Cb1, v_Lm2 ≈ -v_Cb2, v_Lm3 ≈ -v_Cb3, v_La1 = -V_o and v_La2 ≈ v_Cb1/n1 - V_o. Thus, i_p1−i_p3 and i_La1 decrease and i_La2 increases.

**Step 6 [t5−t6]:** When Q2, Q4 and Q6 turn off at time t5, the negative primary currents i_p1−i_p3 rapidly charge C_Q2, C_Q4 and C_Q6, respectively. On the other hand, C_Q1, C_Q3 and C_Q5 are discharged by i_p1−i_p3 respectively. The secondary winding voltage v_ms is increased in this step.

**Step 7 [t6−t7]:** When C_Q2, C_Q4 and C_Q6 are charged to v_Cb1, v_Cb2 and v_Cb3 respectively at t6, it can obtain v_ms = 0. Thus, i0 freewheels through D1 and D2 in this step and v_La1 = v_La2 = -V_o.

**Step 8 [t7−t8 + T_{sw}]:** When C_Q1, C_Q3 and C_Q5 are discharged to zero voltage at t7, the body diodes D_Q1, D_Q3 and D_Q5 are forward biased. Power switches Q1, Q3 and Q5 can be turned on at this moment to realize zero-voltage turn-on. Since i0 still freewheels through D1 and D2, it can obtain v_ms = 0, v_La1 = v_La2 = -V_o and v_Lr1 = v_Lr2 = v_Lr3 = V_in/3 - v_Cb1. Thus, i_p1−i_p3 increase and i_La1 and i_La2 decrease. This step is ended when i_D1 = 0. During this freewheeling interval, i_Lr1−i_Lr3 increase from -i_La2/(3n1) to i_La0/(3n1). The duty loss in step 8 is obtained as (2) shows:

\[
d_{loss8} = \frac{I_o L_{rs}}{3n_1(V_{in}/3 - v_{C_b1})} \tag{2}
\]

At time t0 + T_{sw}, i_D1 is decreased to zero and this switching period is completed. Since the duty cycle of all switches equals 0.5, the voltage balance of C1, C2 and C3 is well achieved with two balance capacitors C1 and C2. If Q1, Q3 and Q5 are in the on-state and Q2, Q4 and Q6 are in the off-state, it obtains v_C1 = V_C1 and v_C2 = V_C2. If V_C1 > V_C2 or V_C1 < V_C2, then C1 charges or discharges C1 through Q1 and Q3. When Q1, Q3 and Q5 are in the off-state and Q2, Q4 and Q6 are in the on-state, it obtains v_C1 = V_C2 and v_C2 = V_C3. If V_C1 > V_C2 or V_C1 < V_C2, C1 charges or discharges C2 through Q2 and Q4. In a similar way, C2 can be used to balance V_C2 and V_C3. Therefore, V_C1−V_C3 are all controlled at V_in/3.
Energies 2018, 11, 266

3. Circuit Characteristics

The asymmetric PWM scheme is adopted to drive $Q_1$–$Q_6$. Based on the flux balance of primary inductors such as ($L_{r1}$ and $L_{m1}$), ($L_{r2}$ and $L_{m2}$) and ($L_{r3}$ and $L_{m3}$), the DC capacitor voltages $V_{C1}$–$V_{C3}$ in a steady state can be obtained as $V_{C1} = V_{C2} = V_{C3} = dV_{in}/3$, where $d$ is the duty cycle of $Q_1$, $Q_3$ and $Q_5$. In the same way, the output voltage can be derived from the flux balance of output inductors $L_{o1}$ and $L_{o2}$ in a steady state.

$$V_o = \frac{V_{in}}{3n_1}(1 - d) - \frac{I_o L_s f_{sw}}{3n_1^2} - V_f$$

where $V_f$ is the voltage drop on $D_1$ and $D_2$.

Figure 5. Operation steps of the power converter during one switching cycle (a) step 1 (b) step 2 (c) step 3 (d) step 4 (e) step 5 (f) step 6 (g) step 7 (h) step 8.
Since the average winding currents $i_{p1} \sim i_{p3}$ equal zero and $I_{L01} + I_{L02} = I_o$, the average inductor currents $I_{L01}$ and $I_{L02}$ are derived as $I_{L01} = (1 - d)I_o$ and $I_{L02} = dI_o$. The ripple currents on $L_{o1}$ and $L_{o2}$ are given in (4) and (5).

$$\Delta i_{L01} = \frac{V_o (1 - d + d_{loss,5}) T_{sw}}{L_{o1}} = \frac{(1 - d)V_o T_{sw} + \frac{V_o L_o I_o}{n_1 (1 - d) V_m}}{L_{o1}}$$

$$\Delta i_{L02} = \frac{V_o (d + d_{loss,5}) T_{sw}}{L_{o2}} = \frac{dV_o T_{sw} + \frac{V_o L_o I_o}{n_1 V_m}}{L_{o2}}$$

The asymmetric PWM is adopted to regulate load voltage. From Figure 4, the turn-on time of $D_1$ is related to the duty cycle of $Q_2$ and the turn-on time of $D_2$ is related to the duty cycle of $Q_1$. Therefore, the average diode currents $I_{D1}$ and $I_{D2}$ are expressed as $I_{D1} = (1 - d)I_o$ and $I_{D2} = dI_o$. The voltage stress of diodes $D_1$ and $D_2$ is related to the secondary winding voltage. The secondary winding voltage $V_{Ch1}$ is dependent on the input voltage $V_{in}$ and clamped voltage $V_{Ch1}$. Thus, the voltage stress of $D_1$ and $D_2$ can be given in (6) and (7).

$$v_{D1} = (1 - d)V_{in} / (3n_1)$$

$$v_{D2} = dV_{in} / (3n_1)$$

The conduction losses on rectifier diodes $D_1$ and $D_2$ are approximately equal to $I_o V_f$. If the transformer is constructed, then the magnetizing inductances $L_{n1} \sim L_{n3}$ are given. Thus, the ripple currents $i_{L1,m} \sim i_{L3,m}$ are obtained in (8).

$$\Delta i_{L1,m} = \Delta i_{L2,m} = \Delta i_{L3,m} \approx \frac{(V_{in} / 3 - V_{Ch1})(d - d_{loss,5}) T_{sw}}{L_{m1}} = \frac{d (1 - d) V_{in} T_{sw}}{3 L_{m1}} - \frac{I_o L_o}{3 n_1 L_{m1}}$$

Three HB circuits are connected in a series on the high voltage side to reduce the voltage stress of active switches. Therefore, it is able to obtain the voltage stress of each active switch clamped at $V_{in} / 3$. If the ripple currents on magnetizing inductors and output inductors are neglected, the root-mean-square (rms) currents $i_{Q1,rms} \sim i_{Q1,rms}$ can be derived as (9) and (10) show.

$$i_{Q1,rms} = i_{Q3,rms} = i_{Q5,rms} \approx \frac{(1 - d) I_o \sqrt{d}}{3 n_1}$$

$$i_{Q2,rms} = i_{Q4,rms} = i_{Q6,rms} \approx \frac{d I_o \sqrt{1 - d}}{3 n_1}$$

The conduction losses on $Q_1 \sim Q_6$ are approximately equal to $d (1 - d) I_o^2 R_{on} / (3 n_1^2)$, where $R_{on}$ is turn-on resistance of $Q_1 \sim Q_6$. The positive peak currents of $i_{p1} \sim i_{p3}$ at time $t_1$ are given in (11).

$$i_{p1}(t_1) = i_{p2}(t_1) = i_{p3}(t_1) \approx i_{L1,m} \max + \frac{i_{L1,m} \max}{3 n_1} \approx \frac{d (1 - d) V_{in} T_{sw}}{6 L_{m1}} - \frac{I_o L_o}{6 n_1 L_{m1}} + \frac{(1 - d) I_o}{3 n_1} + \frac{(1 - d) V_{in} T_{sw} + \frac{V_{in} T_{sw}}{n_1}}{6 n_1 L_{m1}}$$

Likewise, the negative peak currents of $i_{p1} \sim i_{p3}$ at time $t_5$ are given in (12).

$$i_{p1}(t_5) = i_{p2}(t_5) = i_{p3}(t_5) \approx i_{L1,m} \max + \frac{i_{L1,m} \max}{3 n_1} \approx -\frac{d (1 - d) V_{in} T_{sw}}{6 L_{m1}} + \frac{I_o L_o}{6 n_1 L_{m1}} - \frac{d I_o}{3 n_1} - \frac{d V_{in} T_{sw} + \frac{V_{in} T_{sw}}{n_1}}{6 n_1 L_{m2}}$$

The minimum primary current to realize zero-voltage turn-on switching of $Q_1, Q_3$ and $Q_5$ is given in (13).

$$i_{p1}(t_5) \geq \frac{V_{in}}{3} \sqrt{\frac{2 C_{Q}}{L_{r1}}}$$
Similarly, the minimum primary current to realize zero-voltage turn-on switching of $Q_2$, $Q_4$ and $Q_6$ is given in (14).

$$i_p(t_1) \geq \frac{V_{in}}{3} \sqrt{\frac{2C_Q}{L_{r1}}} \quad (14)$$

where $C_Q = C_{Q1} = C_{Q2} = C_{Q3} = C_{Q4} = C_{Q5} = C_{Q6}$.

4. Experimental Results

A laboratory prototype with 1.44 kW rated power was constructed and tested in order to verify the feasibility of the studied converter to supply the auxiliary power in a light rail vehicle from the DC microgrid system. The experimental circuit diagram of the developed converter is provided in Figure 6. The TL431 voltage regulator and photocoupler PC817 are used to regulate load voltage. The PWM UCC2893 is used to achieve asymmetric pulse-width modulation (APWM) generation. Pulse transformers are adopted to achieve electrical isolation and gate drive. The specifications of the experimental prototype are given in Table 1. The power rating of the magnetic transformer is the same as the transformer in the three-level converter and the two-level full-bridge converter. The turns-ratio of the transformer in the developed converter is one-third of the turns-ratio in the two-level full-bridge converter. The magnetizing voltage and primary turns of the transformer in the studied converter are only one-third of the magnetizing voltage and primary turns in the two-level full-bridge converter. The PC40 EER-42 magnetic core is used with 15 primary turns and 8 secondary turns to build the isolated transformer. The experimental results of the proposed converter while it supplies 1.44 kW to the output load under a 760 V input are shown in Figures 7–12. Based on the test results, the measured waveforms agree well with the theoretical waveforms as given in Figure 4. Figure 7 shows the gate voltages of $Q_1$–$Q_6$ at 20% and 100% loads. It is clear that $Q_1$, $Q_3$ and $Q_5$ have the same PWM waveforms. In the same manner, $Q_2$, $Q_4$ and $Q_6$ have the same PWM waveforms. The input split voltages and balance capacitor voltages at a full load are shown in Figure 8. From the experimental results, the input split voltages and two flying voltages are balanced well. The primary side currents of three HB circuits are illustrated in Figure 9. It is observed that the three primary currents are balanced well. Figure 10 gives the measured waveforms of three DC block capacitor voltages. It can be observed that the three voltages are balanced and the capacitor voltages are related to the duty cycle of $Q_1$, $Q_3$ and $Q_5$. Figure 11 shows the experimental waveforms of the secondary side currents. The ripple currents on $L_{o1}$ and $L_{o2}$ partially cancel each other so that the resultant ripple current on the load side is reduced. Figure 12 shows the test results of $Q_1$ and $Q_2$ at 20% and 100% loads. Before the switch is turned on, the switch current is negative to discharge the output capacitor $C_Q$ to zero voltage. Thus, the mechanism of the zero-voltage turn-on switching is clearly achieved for both $Q_1$ and $Q_2$ from a 20% load. It can also be observed that all drain voltages of $Q_1$ and $Q_2$ are clamped at $V_{in}/3$. Since the PWM signals of the three HB circuits are identical and the input split voltages are also balanced, $Q_3$–$Q_6$ can also be turned on at zero-voltage from a 20% load. Figure 13 shows the circuit efficiency of the studied converter under different load cases. The measured maximum efficiency is about 93.6%. The main advantage of the studied converter is the lower voltage rating of power switches compared to the conventional three-level converter with eight MOSFETs and the two-level full-bridge converter with four IGBTs. Considering the turns-ratio of the transformer, the root-mean-square current of the studied converter is the same as the three-level and two-level converters. However, the lower conduction resistance of MOSFETs with lower voltage rating is used in the developed converter. Therefore, the total conduction losses (six MOSFETs) in the studied converter can be reduced compared to the three-level converter with eight MOSFETs and the full-bridge converter with four IGBTs.
Table 1. Prototype Specifications.

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>$V_m$</td>
<td>760 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_o$</td>
<td>24 V</td>
</tr>
<tr>
<td>Output current</td>
<td>$I_o$</td>
<td>60 A</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_{sw}$</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Power switches</td>
<td>$Q_1$–$Q_6$</td>
<td>IRFP460</td>
</tr>
<tr>
<td>Rectifier diodes</td>
<td>$D_1$, $D_2$</td>
<td>MBR40100T</td>
</tr>
<tr>
<td>Split capacitors</td>
<td>$C_1$, $C_2$, $C_3$</td>
<td>330 μF/400 V</td>
</tr>
<tr>
<td>Flying capacitors</td>
<td>$C_{f1}$, $C_{f2}$</td>
<td>2.2 μF/630 V</td>
</tr>
<tr>
<td>Block capacitors</td>
<td>$C_{b1}$, $C_{b2}$, $C_{b3}$</td>
<td>750 nF/630 V</td>
</tr>
<tr>
<td>Turns ratio of T</td>
<td>$n_p$</td>
<td>$n_c$</td>
</tr>
<tr>
<td>Primary inductances</td>
<td>$L_{r1}$, $L_{r2}$, $L_{r3}$</td>
<td>30 μH</td>
</tr>
<tr>
<td>Magnetizing inductances</td>
<td>$L_{m1}$, $L_{m2}$, $L_{m3}$</td>
<td>0.8 mH</td>
</tr>
<tr>
<td>Output filter inductances</td>
<td>$L_{o1}$, $L_{o2}$</td>
<td>32 μH</td>
</tr>
<tr>
<td>Output filter capacitance</td>
<td>$C_o$</td>
<td>4400 μF/50 V</td>
</tr>
</tbody>
</table>

Figure 6. The experimental circuit diagram of the developed converter.

Figure 7. PWM signals of $Q_1$–$Q_6$ under (a) 20% load; (b) full load [$v_{Q1}$–$v_{Q6}$: 10 V/div; time: 2 µs].
Figure 8. Measured input capacitor voltages under full load [$V_{C1}$~$V_{C2}$: 200 V/div; time: 2 µs].

Figure 9. Test results of the primary side currents under (a) 20% load [$i_{p1}$~$i_{p3}$: 2 A/div; time: 2 µs]; (b) full load [$i_{p1}$~$i_{p3}$: 5 A/div; time: 2 µs].

Figure 10. Test results of the primary capacitor voltages under (a) 20% load [$V_{Cf1}$~$V_{Cf3}$: 100 V/div; time: 2 µs]; (b) full load [$V_{Cb1}$~$V_{Cb3}$: 100 V/div; time: 2 µs].
Figure 11. Measured secondary side currents at (a) 20% load \[i_{Q1}, i_{Q2}, i_{Lo1}, i_{Lo2}, i_{Lo1} + i_{Lo2}: 10 \text{ A/div; time: 2 \mu s}\]; (b) 100% load \[i_{Q1}, i_{Q2}, i_{Lo1} + i_{Lo2}: 50 \text{ A/div; } i_{Lo1}, i_{Lo2}: 20 \text{ A/div; time: 2 \mu s}\].

Figure 12. Measured switch voltages and current (a) \(Q_1\) at 20% load \[v_{Q1,d}, v_{Q1,g}: 10 \text{ V/div; } v_{Q1,d}: 200 \text{ V/div; } i_{Q1}: 2 \text{ A/div; time: 1 \mu s}\]; (b) \(Q_1\) at full load \[v_{Q1,d}, v_{Q1,g}: 10 \text{ V/div; } v_{Q1,d}: 200 \text{ V/div; } i_{Q1}: 10 \text{ A/div; time: 1 \mu s}\]; (c) \(Q_2\) at 20% load \[v_{Q2,d}, v_{Q2,g}: 10 \text{ V/div; } v_{Q2,d}: 200 \text{ V/div; } i_{Q2}: 2 \text{ A/div; time: 1 \mu s}\]; (d) \(Q_2\) at full load \[v_{Q2,g}: 10 \text{ V/div; } v_{Q2,d}: 200 \text{ V/div; } i_{Q2}: 10 \text{ A/div; time: 1 \mu s}\].

Figure 13. Test results of circuit efficiency.

5. Conclusions

In this paper, a series-connected HB converter with a single transformer is proposed for light rail transit applications. The proposed circuit’s main benefits are the low voltage rating of power semiconductors, low switching losses, high circuit efficiency and balance split voltages compared to conventional converter topologies used in light rail vehicles. The asymmetric PWM scheme is used to control power switches, regulate output voltage and achieve the mechanism of the zero-voltage
turn-on switching. The circuit analysis, operation principle and design example of the proposed circuit are presented and discussed in detail. Finally, the feasibility of the studied circuit is verified by experimental results with a 1.44 kW laboratory prototype. The current harmonics on the input side is dependent on the switching frequency and the load current. The large current harmonics will result in unstable voltage on the input DC voltage bus. Therefore, in a future study, the interleaved DC/DC converter of the studied circuit will be developed to reduce the input current harmonics.

Acknowledgments: This research is supported by the Ministry of Science and Technology, Taiwan, under contract MOST 105-2221-E-224-043-MY2. The author would like to thank Wei-Po Liu for his help in the experiment. The author would also like to thank the anonymous reviewers for their valuable comments and suggestions to improve the quality of the paper.

Conflicts of Interest: The author declares no potential conflict of interest.

References


