


Article

Theoretical and Experimental Investigation of the Voltage Ripple across Flying Capacitors in the Interleaved Buck Converter with Extended Duty Cycle

Peter Zajec * and Mitja Nemeč 

Faculty of Electrical Engineering, Department of Mechatronics, University of Ljubljana, Trzaska 25, 1000 Ljubljana, Slovenia; mitja.nemec@fe.uni-lj.si

* Correspondence: peter.zajec@fe.uni-lj.si; Tel.: +386-1-4768-479

Received: 25 March 2018; Accepted: 18 April 2018; Published: 21 April 2018



Abstract: The interleaved buck converter with an extended duty cycle is analyzed in terms of unexplored parasitic switching states that diminish the switch utilization and its safety due to high-magnitude charging and discharging currents. The analysis explains the origin of the states and their effects and demonstrates their correlation with the existing voltage ripple on flying capacitors. The article further demonstrates that the voltage ripple can no longer be arbitrarily chosen as parasitic states emerge whenever the ripple exceeds an identified critical value being equal to the twofold voltage drop on the diode. A simple design criterion for flying capacitance is proposed. For a limited set of battery-powered DC–DC converters, a solution permitting the use of smaller capacitance by adding an extra switch is proposed. The derived findings are verified using experimental and simulation results.

Keywords: DC–DC conversion; interleaved buck; parasitic switching states

1. Introduction

DC–DC converters, capable to operate at a high voltage conversion ratio between the input V_{in} and output voltages V_{out} , are gaining noticeable consideration in different applications [1,2], ranging from point-of-load converters to converters in several hybrid vehicle configurations. In these applications, power switches are commonly poorly utilized. Switch utilization is, in general, defined as the ratio between the output power consumed on a load and the product of the maximum voltage and current on the switch, thus being proportional to the duty cycle [3,4]. In the past, low switch utilization was successfully addressed in inductor-tapped solutions; with the only drawback of the increased blocking voltage [5–8]. In recent years, the voltage rating of the switch is commonly reduced by applying multi-level DC–DC converters, such as the one with a flying capacitor [9–14]. In this case, the switch utilization is increased at the price of increased control complexity. On the other hand, the switches with lower voltage ratings exhibit lower conduction and switching losses, consequently increasing the overall efficiency.

Traditionally, switch utilization can be enhanced by sharing the total power among converters operating in parallel. Such a converter is designated as a multi-phase converter [15–20]. Additional benefits can be further gained by interleaving as the current ripple through the output smoothing capacitor is decreased. In order not to exceed the current rating of the individual switch, the complexity of control becomes problematic not only due to the increased number of current transducers but mostly as the current has to be evenly shared both in the steady state and during transients.

The advantages of both concepts, i.e. multi-level and multi-phase, have been successfully combined in the interleaved multi-phase Buck converter with an extended duty cycle proposed in [19,20]. There, two different topologies are presented. Both feature almost the same benefits, differing in the number of switches per phase. In a topology with two metal oxide semiconductor field effect transistors (MOSFET) per output phase (analyzed in this paper—Figure 1), all MOSFETs (T_1 – T_4) are subjected to the same current (I_{load}/n , where n denotes the number of phases) and voltage ($V_{in}/2$) stress. Most importantly, the current sharing among phases takes place spontaneously. Accordingly, only the load current needs to be measured, thus make the analyzed topology an ideal example for high-current applications.

Regardless of the topology, flying capacitors are exposed to large current and thermal stress, which leads to a more rapid ageing of the component [21]. Its consequences are reduced capacitance and increased equivalent series resistance (ESR). Accordingly, when selecting capacitors, a wider design margin is needed in order to mitigate the capacitor's degradation and to guarantee error-free operation.

Commonly, when analyzing DC–DC converters, bulky capacitors are implied, assuming the voltage ripple on the capacitor is small enough compared to its average voltage. This is certain for output smoothing capacitor, which has the direct impact on the output voltage quality and on the electromagnetic interference (EMI). On the other hand, in practice, a larger voltage ripple is usually allowed across flying capacitors in order to decrease the required volume in high-density designs. No serious impacts on the basic operation of the converter owed to a higher voltage ripple on flying capacitors have been reported [9–14].

This paper offers an in-depth analysis of interleaved buck topology. The paper also derives a condition referring to the minimum capacitance that separates error-free operation from the appearance of the parasitic switching states, and discuss the effects if the condition is not met. The origin of the parasitic switching states is analyzed in detail as not yet reported in references dealing with this topology [19,20]. Furthermore, a simple solution that prevents the appearance of parasitic states and their effects is proposed and commented.

2. The Operating Principle of the Interleaved Buck Converter

Figure 1 depicts the original scheme of the two-phase interleaved buck consisting of four MOSFETs and freewheeling diodes D_{11} and D_{22} [19]. Consistently with the original paper, only the continuous conduction mode (CCM) operation is assumed.

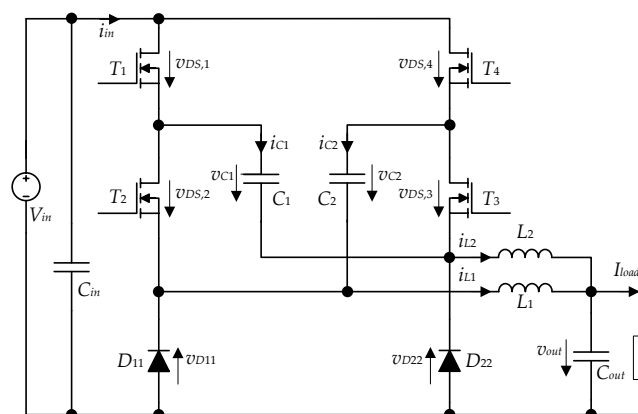


Figure 1. The interleaved two-phase buck converter with an extended duty cycle.

Accordingly, the converter enters four active switching intervals (identified by the conduction of a particular switch) that take part in a predefined sequence—either clockwise (CW sequence: T_4 – T_3 – T_2 – T_1) or counter-clockwise (CCW sequence: T_1 – T_2 – T_3 – T_4). Between two consecutive active switching intervals, the freewheeling interval (FW) occurs. In that interval, inductors' currents flow

through D_{11} and D_{22} . All active switching intervals have the same duty cycle (d_{sw}) which never exceeds 0.25. In the same paper, it is further demonstrated that, assuming the circuit symmetry, the average voltage across the flying capacitor (C_1, C_2) equals $V_{in}/2$, and the load current is equally shared among inductors. As a result, in steady-state operation, the output voltage is proportional to $V_{in} \cdot d_{sw}/2$. To sum up, all results and conclusions provided in [19,20] apply only to highly idealized cases due to the assumed bulkiness of C_1 and C_2 .

2.1. Deriving the Voltage Ripple on Flying Capacitors

During the operation, C_1 and C_2 are charged and discharged interchangeably by i_{L1} and i_{L2} as seen in Figures 2 and 3. As a result, they are inherently subjected to short current pulses of high magnitude that equal I_{L1} and I_{L2} respectively.

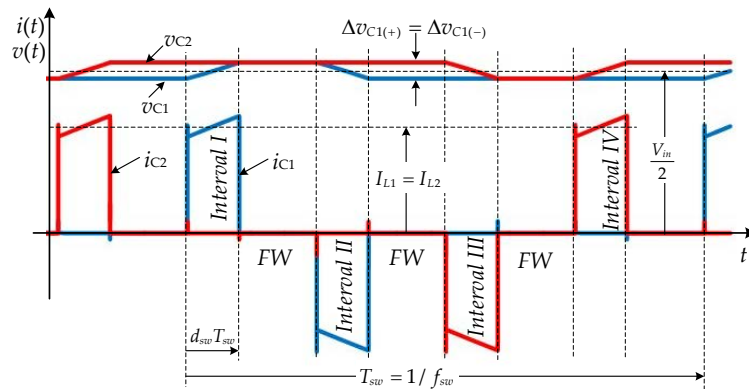


Figure 2. Simulation results showing voltages and currents that flow through flying capacitors (details regarding the simulation models built in LTspiceXVII can be found in Section 3).

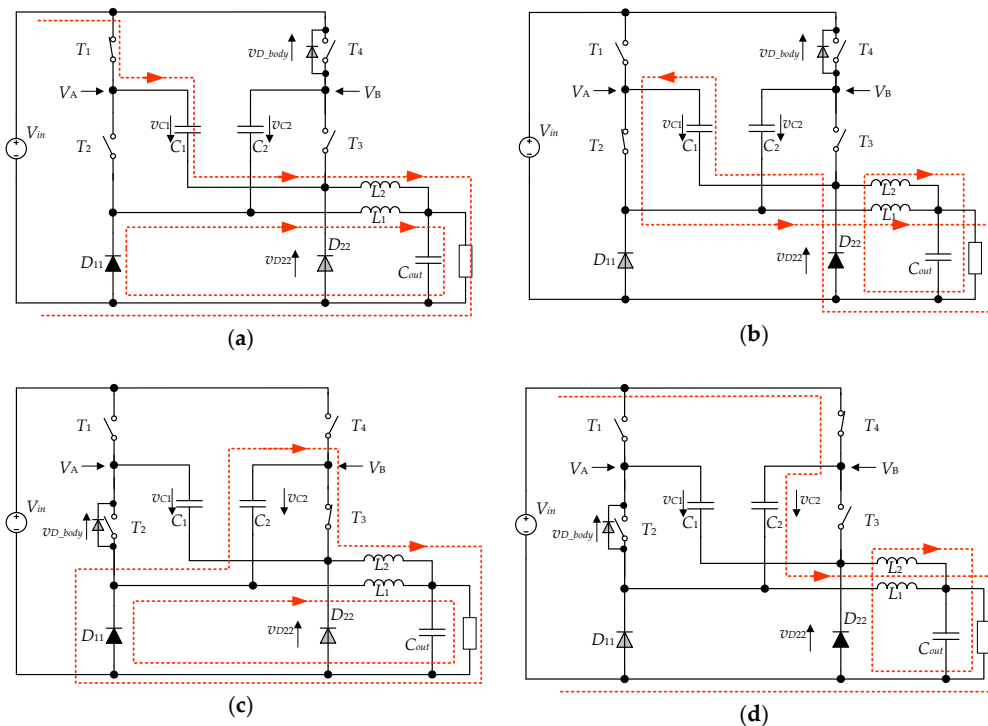


Figure 3. Equivalent circuits with indicated current paths (in red) when Δv_C (see text) is below a critical value in: (a) Interval I; (b) Interval II; (c) Interval III; (d) Interval IV.

In *Interval I*, the capacitor C_1 is charged by the inductor current i_{L2} . In *Interval II*, when T_2 is switched ON, C_1 is discharged by current i_{L1} .

Assuming a lossless capacitor v_{C1} remains unchanged during the FW interval, as well as in consecutive intervals when v_{C2} at first decays in *Interval III* (due to i_{L2}) and then in *Interval IV* rises back (due to i_{L1}). In the steady-state, the voltage increase and decrease on the individual flying capacitor are in equilibrium:

$$\begin{aligned}\Delta v_{C1(+)} &= \frac{I_{L2} \cdot d_{sw}}{C_1 \cdot f_{sw}} = \frac{I_{L1} \cdot d_{sw}}{C_1 \cdot f_{sw}} = \Delta v_{C1(-)} \\ \Delta v_{C2(+)} &= \frac{I_{L1} \cdot d_{sw}}{C_2 \cdot f_{sw}} = \frac{I_{L2} \cdot d_{sw}}{C_2 \cdot f_{sw}} = \Delta v_{C2(-)}\end{aligned}\quad (1)$$

Assuming symmetrical circuit the voltage ripples, expressed as a peak–peak value, are equal ($\Delta v_{C1} = \Delta v_{C2} = \Delta v_C$) on both flying capacitors.

In *Interval II* (Figure 3b), the diode D_{22} is forward-biased. Therefore, the potential in node A is equal to the sum:

$$V_{A,II} = -v_{D22} + v_{C1}. \quad (2)$$

By neglecting the voltage drop on MOSFET (T_2), the potential in node B is:

$$V_{B,II} = -v_{D22} + v_{C1} + v_{C2}. \quad (3)$$

Figure 2 demonstrates that at the end of *Interval I*, the capacitor voltages v_{C1} and v_{C2} tend to reach their maximum values ($V_{in}/2 + \Delta v_C/2$) and remain unchanged until the start of *Interval II*. Consequently, at the start of *Interval II*, V_B reaches its maximum as well:

$$V_{B,II\max} = -v_{D22} + V_{in} + \Delta v_C. \quad (4)$$

Providing that $V_{B,II\max}$ is lower than $V_{in} + v_{D_body}$, the body diode in MOSFET (T_4) remains reverse-biased. Thus, if an equal voltage drop across the body diode and the freewheeling diode is assumed, the voltage sum across flying capacitors ($V_{in} + \Delta v_C$) should be kept below $V_{in} + 2v_D$. The latest can be rephrased into the condition:

$$\Delta v_C \leq 2v_D, \quad (5)$$

where $2v_D$ is recognized as a critical value of the voltage ripple Δv_C .

In a similar way, at the start of *Interval IV* (Figure 3d), the body diode in MOSFET (T_2) could conduct only if the sum of flying capacitor voltages drops below its minimum $V_{in} - \Delta v_C$. In the meantime, node B is fastened to the positive supply, causing:

$$V_{B,IV} = V_{in}, \quad (6)$$

whereas the potential in node A remains unchanged compared to *Interval II*:

$$V_{A,IV} = -v_{D22} + v_{C1}. \quad (7)$$

However, as voltages on both flying capacitors have already reached their minimum ($V_{in} - \Delta v_C/2$), $V_{A,IV}$ drops to:

$$V_{A,IV\min} = -v_{D22} + \frac{V_{in} - \Delta v_{C1}}{2}. \quad (8)$$

By assuming equal voltage drops across the body diode and the freewheeling diode, the same condition already stated in Equation (5) determines whether the body diode in MOSFET (T_2) remains biased in reverse or it turns into conduction.

2.2. The Origin of the Parasitic Switching States

Referring to the derived Equations (2)–(8), it is evident that the maximum voltage ripple permitted on flying capacitors cannot be chosen arbitrarily during the design process. If the ripple exceeds $2v_D$, the parasitic switching state emerges as the body diode of the inactive MOSFET is forward-biased. Figure 4a shows an existing current path (dashed red line) during *Interval II* and an extra path (solid blue line) that appears through the body diode in T_4 .

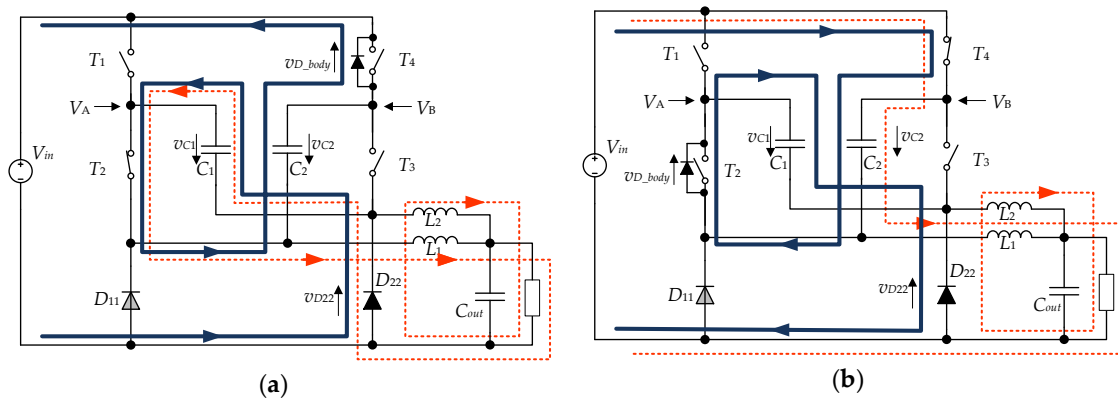


Figure 4. Equivalent circuits showing extra current paths (in blue) that occur when Δv_C exceeds the critical value: (a) in *Interval II**; (b) in *Interval IV**.

The extra current path emerges at the beginning of *Interval II* and exists only for a limited time, being denoted as *Interval II**. Figure 5 shows this phenomenon in detail. During this interval, a surplus charge, which has accumulated on flying capacitors, is abruptly discharged back to the voltage source.

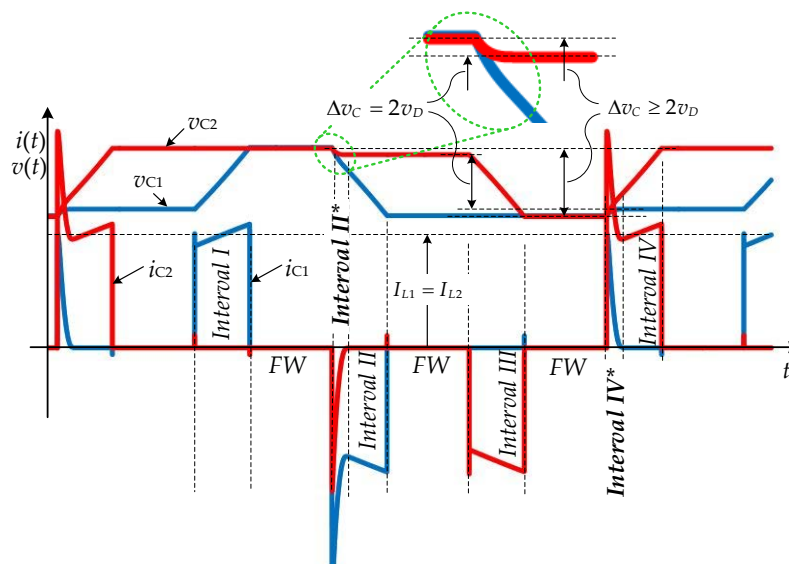


Figure 5. Simulation results showing flying capacitor currents and voltages with zoomed voltage waveforms in parasitic *Interval II**.

This overcharging does not jeopardize the validity of the derived Equations (2)–(8) as these define electric potentials in nodes A and B only in *Interval II* and *Interval IV*. In fact, at the end of *Interval I*, the flying capacitors could be charged to a higher voltage as shown in the zoomed part in Figure 5, depending on the parameters involved in Equation (1), thus forcing the voltage ripple over the critical

value. If this is the case, the capacitors discharge until their ripples drop below $2v_D$. If the ripples remain inside the boundaries, the error-free operation depicted in Figure 2 takes place.

The shape of the discharging current, which flows simultaneously through both flying capacitors, follows:

$$i(t) = \frac{V}{\omega_r L_p} e^{-\alpha t} \cdot \sin(\omega_r t); \alpha = \frac{R}{2L_p}; \omega_r^2 = \frac{1}{L_p C} - \left(\frac{R}{2L_p}\right)^2, \quad (9)$$

where V stands for the voltage difference seen in the zoomed section in Figure 5. The shape is defined by R - L - C parameters found in the depicted path (Figure 4a, blue line) where small resistances (R) and inductances (L_p), both contributed by parasitic components of circuit and flying capacitors (C), have a dominant impact on the magnitude and period of the signal. Its period could be as short as the conduction interval of power switches, whereas its magnitude can easily reach or even surpass the inductor current.

Figure 4b indicates a similar parasitic switching state which could occur when T_4 turns ON if in that instant the sum of voltages across C_1 and C_2 is too low to maintain the body diode of T_2 reverse-biased. In that case, the capacitors are abruptly charged from the power source through the forward-biased body diode of MOSFET T_2 . As D_{22} is forward biased by the freewheeling current forced by L_2 , the surge current (blue line) can be considered to flow in opposite direction thus decreasing the current through D_{22} .

It is apparent that such an operation is not desirable as conduction losses may increase considerably, but also since semiconductors and flying capacitors could be overstressed by the current. In addition, if the front side of the converter includes an overcurrent protection, its level should be high enough to prevent an unintentional tripping. Therefore, to prevent the occurrence of these states and their impacts, the capacitance should be set higher than the critical one:

$$C_{crit} = \frac{I_{load}}{2v_D \cdot f_{sw}} \cdot \frac{V_{out}}{V_{in}}. \quad (10)$$

Equation (10) is derived from Equation (1) by taking into account that the load current is equally shared among inductors and the voltage ratio V_{out}/V_{in} is proportional to $d_{sw}/2$. It is important to point out that the form of Equation (10) is not significantly different from equations that can be derived for an arbitrary converter with flying capacitors [9,11,13,14]. The critical capacitance in this particular converter is inherently limited by topology itself, as the ripple must not exceed the twofold voltage drop on the diodes ($2v_D$). This finding is the essential contribution to the original papers [19,20] in order to preserve an error-free operation.

3. Simulation and Experimental Results

Simulations have been performed using LTspiceXVII. The simulation model did not include any additional inductances besides those already present in the models of transistors and diodes.

Experimental verifications have been carried out in order to prove the theoretical reasoning and simulation results already partially presented when introducing the parasitic switching states and their effects in the previous section. The experimental setup including a custom-made converter with a TMS320F2806 DSP (Texas Instruments, Dallas, TX, USA) is presented in Figure 6. Table 1 summarizes the main parameters of the experimental setup.

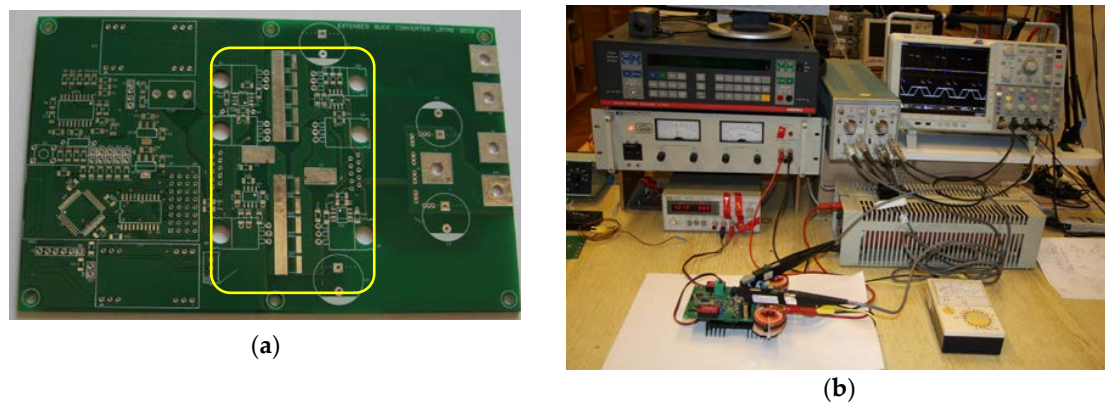


Figure 6. Pictures of the experimental setup: (a) an unpopulated printed circuit board (PCB) with a marked (yellow) section consisting of six MOSFETs and flying capacitors; (b) converter at the test bench.

Table 1. Parameters of the prototype converter and its simulation model.

Label	Description	Value
V_{in}	Input voltage	30 V
V_{out}	Output voltage	3 V
$I_{load,max}$	Load current	50 A
C_1, C_2	Flying capacitance	50 μ F
L_1, L_2	Inductance	55 μ H
f_{sw}	Switching frequency	33 kHz

The converter is deployed on a two-layer PCB. The topology is the same as in Figure 1 but the D_{11} and D_{22} were replaced with MOSFETs in order to increase the flexibility of converter thus enabling additional research. For measurements, these MOSFETs were permanently OFF to emulate the freewheeling diodes D_{11} and D_{22} . In order to reduce EMI to the lowest possible level, flying capacitors are placed in a close proximity of switching nodes with a high dv/dt , thus keeping the current loops that are subjected to pulses with a high di/dt short as well. In order to enable the current measurement through flying capacitors, the PCB was not equipped with multilayer ceramic capacitors (MLCC). Instead, they are placed on dedicated holders which are connected to the rest of the circuit by solid wires where a current probe (A6302 from Tektronix, Beaverton, OR, USA) can be clamped on. To simplify the tests, each MLCC holder was populated with three 15 μ F/50 V capacitors. According to the known current that flows through parallel capacitors, their capacitance was estimated at 30 μ F at an average capacitor voltage (15 V). For tests requiring a critical or higher capacitance, the difference was realized by fastening a temporary capacitor of an adequate capacitance.

The first test was carried out in order to verify the steady-state waveforms of the converter and its numerical model built in LTspiceXVII. Due to the additional inductance introduced by the aforesaid capacitor placement, tests have been performed at a reduced current capability ($I_{load,max*} = 20$ A) in order to reduce overvoltage on MOSFETs. In accordance with Equation (10), the critical capacitance amounts to 44 μ F. Figure 7a,b depict i_{C1} (blue) and i_{C2} (red) at different load currents and with a capacitance greater than C_{crit} specified in Equation (10). The shape and magnitude of both currents closely match simulation traces seen in the top part of Figure 7c,d, but there is slight asymmetry of magnitudes between currents due to mismatch of inductance and capacitor values.

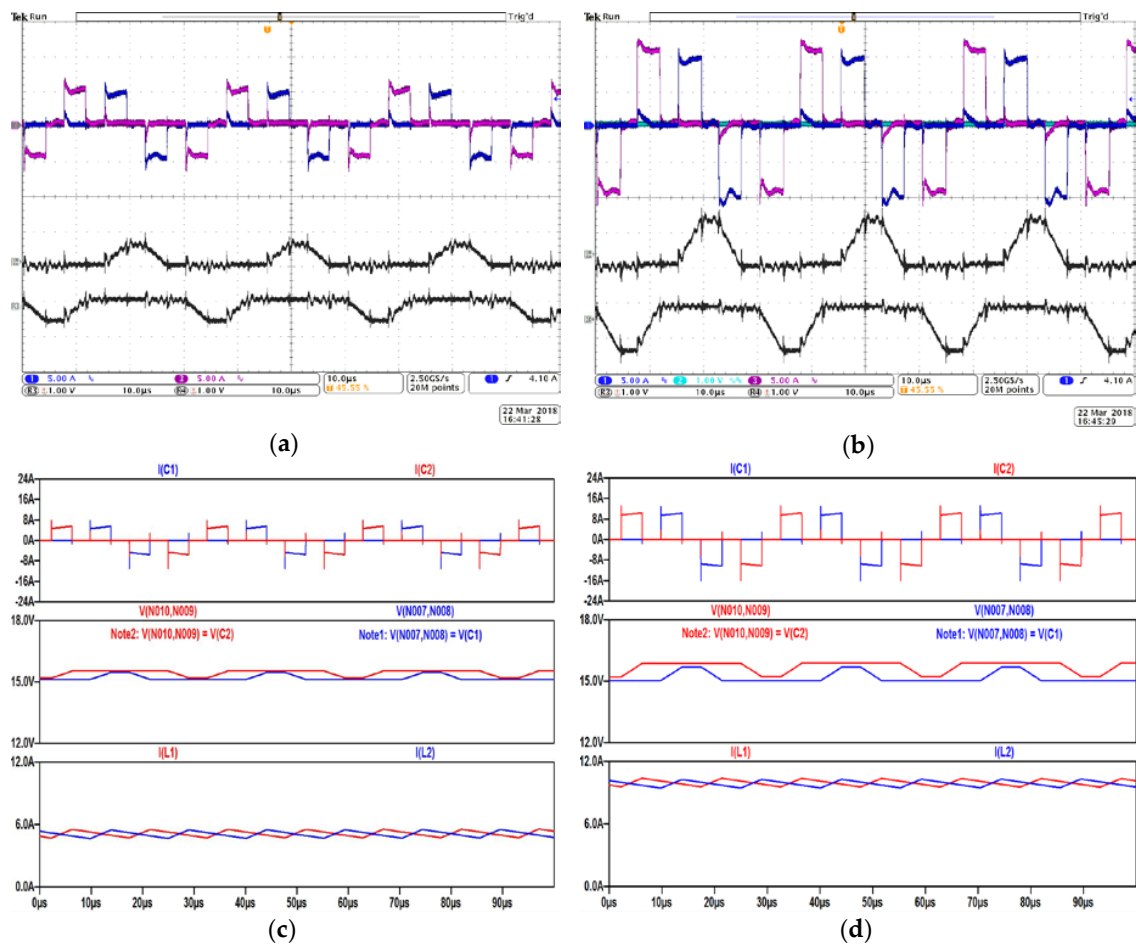


Figure 7. Experimental and simulation results obtained at $C_1 = C_2 = 60 \mu\text{F}$, ($C_{\text{crit}} = 44 \mu\text{F} @ I_{\text{load,max}}^* = 20 \text{ A}$). Flying capacitors' currents (blue: i_{C1} ; red: i_{C2}) and voltages (AC components only) on flying capacitors (top black: v_{C1} ; bottom black: v_{C2}), both measured at an average inductor current: (a) 5 A; (b) 10 A. Simulated results at an average inductor current: (c) 5 A and (d) 10 A: the upper part, flying capacitors' currents: the middle part, voltages on flying capacitors: the lower part, inductors' currents.

Current spikes, which appear in experimental traces whenever an individual MOSFET turns ON, are caused by the reverse recovery charge Q_{rr} of the freewheeling diodes. Owing to the increased inductance, the trailing edges of these spikes are additionally prolonged. In addition, a capacitive coupling due to the close proximity between switching nodes with a high dv/dt and the current probe rendered the shape of current measurements, too. When voltages—especially those referenced against one of the switching node—are measured with passive voltage probes, the quality of captured traces on oscilloscope (Tektronix–DPO 4034B) usually worsen substantially. As a result, voltages shown on oscilloscope window were not measured simultaneously with current traces. Instead, they were measured separately and then recalled from internal memories.

In addition, voltage ripples in the middle part of Figure 7c,d exhibit their dependency on the load current (traces at the bottom of the same figures) as identified in the analysis. As it can be noticed, the experimental voltage ripples (at the bottom part of the Figure 7a,b) match the simulated ones quite faithfully, both in the magnitude and the shape. The average value of the flying capacitor voltages differs from $V_{in}/2$, being theoretically derived with neglected voltage drops on MOSFETs and freewheeling diodes.

The effectiveness of the proposed analytical developments given by Equations (2)–(10) is further confirmed in Figure 8, where an experimental verification was carried out considering the violation of the critical value of flying capacitance. Compared to the simulation results in Figure 8a, it can be noticed that the experimental currents in Figure 8b exhibit a longer duration of parasitic intervals. Referring to Equation (9), this deviation can be explained as simulation did not include any additional parasitic inductances which were present in the circuit (PCB traces, transistor terminals, equivalent series inductance of capacitors, capacitor holder).

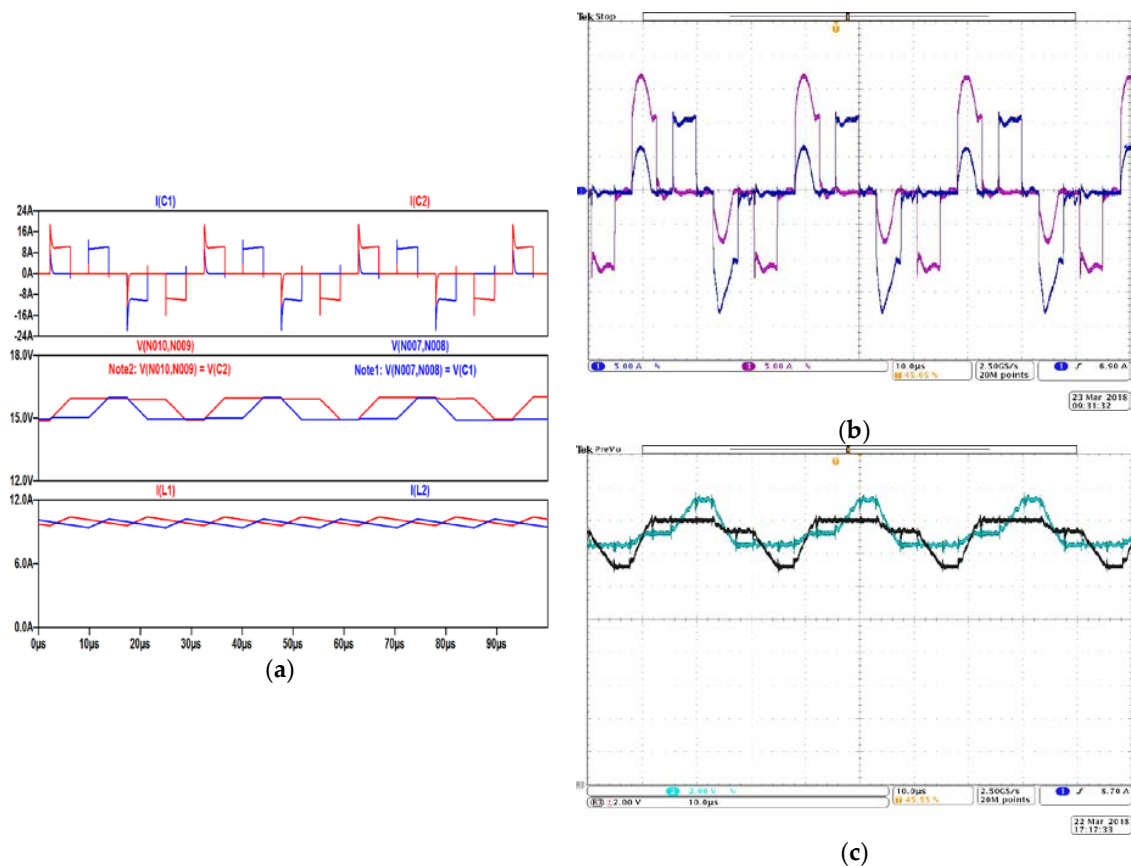


Figure 8. Simulation and experimental results obtained at an average inductor current 10 A and at $C_1 = C_2 = 35 \mu\text{F}$: (a) simulated results: the upper part, flying capacitors' currents: the middle part, voltages on the flying capacitors: the lower part, inductors' currents; (b) measured results: flying capacitors' currents (blue: i_{C1} ; red: i_{C2}); (c) voltages on the flying capacitors (blue: v_{C1} ; black: v_{C2}).

4. Discussion

All in all, the benefit of knowing the critical capacitance can be of higher importance in the converter with n larger than 2, particularly if the converter works at higher operational temperatures. There, the selection and placement of flying capacitors in a confined volume are strengthened in order to satisfy thermal and EMI specifications. Commonly, MLCCs of type X8R, X7R or X5R are implemented [22,23]. Nowadays, they can be produced with high-temperature grades (150 $^{\circ}\text{C}$) and with a high rated capacitance (22 $\mu\text{F}/100 \text{V}$) in a relatively small package of size 2220. On the other hand, MLCC faces a considerable voltage dependency. As a result, its rated capacitance could be met only at a reduced voltage. For high volumetric parts, the decrease of C with voltage can be greater than 50% of its rated value [23]. Furthermore, a current derating has to be taken into account in order to reduce the dissipating power inside of the flying capacitors. All this increases the chance that in space-confined designs the flying capacitance has to be chosen close to its critical value, thus increasing

the probability to violate Equation (10). Taking into account the ageing effects of MLCC as well [24–26], the aforesaid becomes even more likely. Furthermore, the situation becomes even worse if diodes D_{11} and D_{22} are replaced with a synchronous MOSFET, in order to boost the efficiency even further. In this case, the peak–peak voltage ripple across C_1 and C_2 falls under the voltage drop of a single body diode, basically halving the voltage ripple given in Equation (5).

As an additional remark, it was found out that, if the sequence changes from CCW to CW, parasitic switching states occur at the beginning of *Interval I* and *Interval III*. Since the body diodes of T_1 and T_3 are biased in the forward direction, the flying capacitors are again exposed to charging and discharging currents. All together, tests show that despite high expectations, the applicability of the converter could be significantly limited due to Equation (10).

Nevertheless, simulation results additionally exhibit that in the case of battery-powered converters—equipped with a MOSFET for battery reversal protection—the parasitic switching states vanish completely. Figure 9a,b show results obtained when extra MOSFETs were added in series with the top positioned MOSFETs T_1 and T_4 , forming a back-to-back switch.

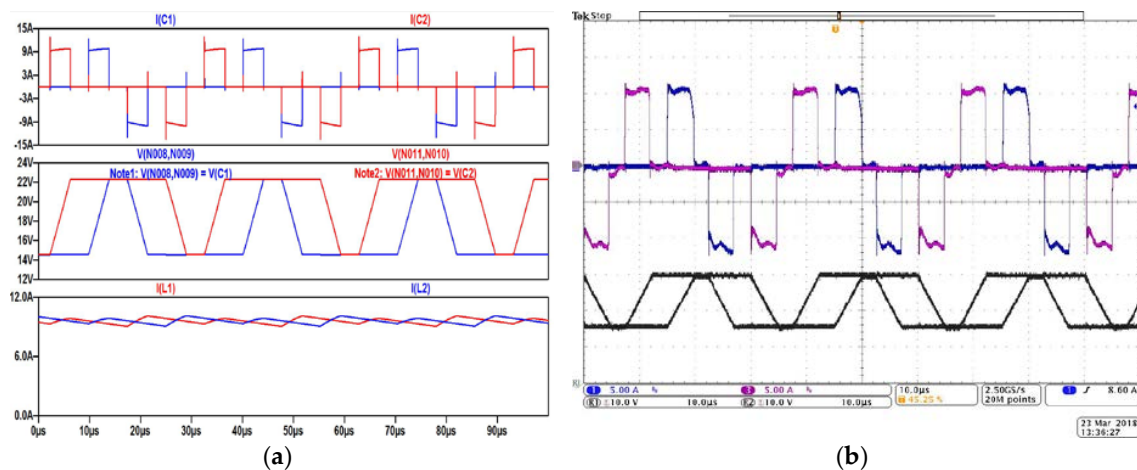


Figure 9. Comparison of results obtained at an average inductor current 10 A, with inserted extra switches and with $C_1 = C_2 = 5 \mu\text{F}$: (a) simulation results: the upper part, flying capacitors' currents: the middle part, voltages on flying capacitors: the lower part, inductors' currents: (b) measured results: the upper part, flying capacitors' currents (blue: i_{C1} ; red: i_{C2}): the lower part, voltages on flying capacitors (bottom black: v_{C1} ; top black: v_{C2}).

The extra MOSFETs are switched simultaneously with T_1 and T_4 . As a result, no discharging current could flow back to the voltage supply irrespective of the CW or CCW sequence. In this case, the flying capacitor is not required to fulfil Equation (5). Thus, a larger voltage ripple may be accepted. In fact, traces on the left and right side in Figure 9 correspond to a flying capacitance of just $5 \mu\text{F}$. Traces i_{C1} and i_{C2} are similar to those in Figure 7d obtained with a much larger capacitance ($60 \mu\text{F}$). Although the voltage ripples in Figure 9a,b are more than five times larger than the ones in Figure 7d, the load current is ideally shared among both inductors. In Figure 10, current sharing is proved even in the case when the resistance of one inductor has been intentionally increased to fivefold.

As it can be noticed in Figures 9 and 10, not only the ripple voltages increase, the average voltage across flying capacitors tends to increase as well. In this particular case, the converter remains functional at the price of an uneven voltage stress of the individual MOSFET (T_1 – T_4). Furthermore, as extra MOSFETs are switched simultaneously with T_1 and T_4 and at the zero-current condition, the total losses of the switches remain more or less unaffected. The control itself remains simple and straightforward. The additional MOSFETs are placed at the bottom side of PCB in order to be efficiently cooled and to keep the parasitic inductance as low as possible.

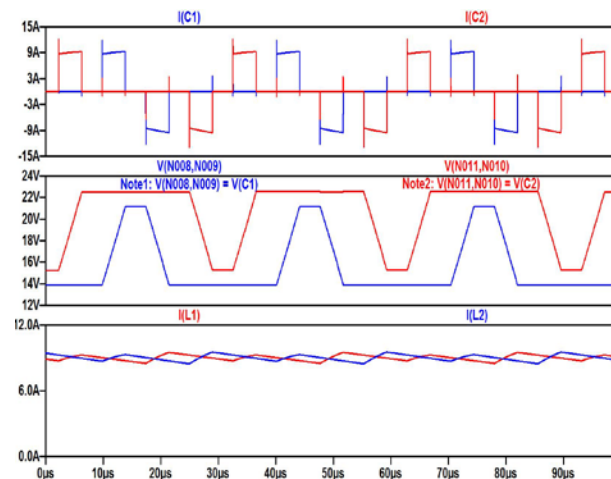


Figure 10. Simulation results obtained at an average inductor current 10 A, with inserted extra switches, with $C_1 = C_2 = 5 \mu\text{F}$ and with unsymmetrical inductors' resistances $R_{L2} = 5R_{L1}$: the upper part, flying capacitors' currents: the middle part, voltages on flying capacitors: the lower part, inductors' currents.

5. Conclusions

The voltage ripple in the interleaved buck converter with an extended duty cycle has been analyzed in this paper, as the converter has been recognized as an ideal candidate for high-current DC–DC applications from many points of view. Specifically, in contrast to other converters being referenced, it provides an equal current and voltage stress on all MOSFETs. And most importantly, it requires less current transducers as the current sharing in output inductors takes place automatically.

The analysis presented in this paper focuses on unexplored switching states which occur under specific conditions in the two-phase interleaved converter. As their occurrence has a significant negative impact on the converter operation, a critical capacitance was derived in order to avoid them. This has been verified with a simulation model and confirmed by the measurements performed on the prototype converter. Furthermore, a simple mitigation solution based on the additional switch per converter's phase is proposed and verified. The solution is justified for battery-powered converters enabling to install a smaller flying capacitance as required by Equation (10).

Author Contributions: Both authors contributed to all of the aspects of the manuscript. To emphasize a particular specific contribution, Peter Zajec wrote the paper, designed and performed the experiments. Mitja Nemeč wrote the code for the DSP and analyzed the simulation and experimental results.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Forouzesh, M.; Siwakoti, Y.P.; Gorji, S.A.; Blaabjerg, F.; Lehman, B. Step-Up DC-DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications. *IEEE Trans. Power Electron.* **2017**, *32*, 9143–9178. [[CrossRef](#)]
2. Du, S.; Wu, B. A Transformerless Bipolar Modular Multilevel DC-DC Converter With Wide Voltage Ratios. *IEEE Trans. Power Electron.* **2017**, *32*, 8312–8321. [[CrossRef](#)]
3. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*; Springer Science & Business Media: Berlin, Germany, 2007; ISBN 978-0-306-48048-5.
4. Schwingal, N.; Bernet, S. Power Semiconductor Loss Comparison of Low-Voltage, High-Power Two-Level and Three-Level Voltage Source Converters. In Proceedings of the PCIM Europe 2015, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 19–20 May 2015; pp. 1–9.

5. Park, J.H.; Cho, B.H. Nonisolation Soft-Switching Buck Converter With Tapped-Inductor for Wide-Input Extreme Step-Down Applications. *IEEE Trans. Circuits Syst. Regul. Pap.* **2007**, *54*, 1809–1818. [[CrossRef](#)]
6. Yao, K.; Ye, M.; Xu, M.; Lee, F.C. Tapped-Inductor Buck Converter for High-Step-Down DC-DC Conversion. *IEEE Trans. Power Electron.* **2005**, *20*, 775–780. [[CrossRef](#)]
7. Park, J.H.; Cho, B.H. The Zero Voltage Switching (ZVS) Critical Conduction Mode (CRM) Buck Converter With Tapped-Inductor. *IEEE Trans. Power Electron.* **2005**, *20*, 762–774. [[CrossRef](#)]
8. Williams, B.W. Unified Synthesis of Tapped-Inductor DC-to-DC Converters. *IEEE Trans. Power Electron.* **2014**, *29*, 5370–5383. [[CrossRef](#)]
9. Zhang, F.; Du, L.; Peng, F.Z.; Qian, Z. A new design method for high efficiency DC-DC converters with flying capacitor technology. In Proceedings of the Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06, Dallas, TX, USA, 19–23 March 2006.
10. Lei, Y.; Liu, W.C.; Pilawa-Podgurski, R.C.N. An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large voltage conversion ratios. In Proceedings of the 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, Canada, 12–15 July 2015; pp. 1–7.
11. Shenoy, P.S.; Lazaro, O.; Amaro, M.; Ramani, R.; Wiktor, W.; Lynch, B.; Khayat, J. Automatic current sharing mechanism in the series capacitor buck converter. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015; pp. 2003–2009.
12. Zhang, F.; Peng, F.Z.; Qian, Z. Study of the multilevel converters in DC-DC applications. In Proceedings of the 2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551), Aachen, Germany, 20–25 June 2004; pp. 1702–1706.
13. Parastar, A.; Gandomkar, A.; Seok, J.K. High-Efficiency Multilevel Flying-Capacitor DC/DC Converter for Distributed Renewable Energy Systems. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7620–7630. [[CrossRef](#)]
14. Jin, K.; Yang, M.; Ruan, X.; Xu, M. Three-Level Bidirectional Converter for Fuel-Cell/Battery Hybrid Power System. *IEEE Trans. Ind. Electron.* **2010**, *57*, 1976–1986. [[CrossRef](#)]
15. Chuang, C.F.; Pan, C.T.; Cheng, H.C. A Novel Transformer-less Interleaved Four-Phase Step-Down DC Converter With Low Switch Voltage Stress and Automatic Uniform Current-Sharing Characteristics. *IEEE Trans. Power Electron.* **2016**, *31*, 406–417. [[CrossRef](#)]
16. Pattnaik, S.; Panda, A.K.; Mahapatra, K.K. An Improved Multiphase converter for New Generation Microprocessr. In Proceedings of the Industrial and Information Systems, 2008, ICIIS 2008. IEEE Region 10 and the Third international Conference on, Kharagpur, India, 8–10 December 2008; pp. 1–5.
17. Harada, K.; Nishijima, K.; Nakano, T.; Nabeshima, T.; Sato, T. Analysis of Double Step-Down Two-Phase Buck Converter for VRM. In *Zuk. Durch Informationstechnik Schnell-Mobil-Intell. Informationstechnik Für Menschen-50 Jahre ITG Vorträge Jubil. Am 26 27 April 2004 Johann-Wolfgang-Goethe-Univ. Frankf. Am Main Mit CD-ROM*; VDE Verlag: Berlin/Offenbach, Germany, 2004; p. 497.
18. Gleissner, M.; Bakran, M.M. Design and Control of Fault-Tolerant Nonisolated Multiphase Multilevel DC-DC Converters for Automotive Power Systems. *IEEE Trans. Ind. Appl.* **2016**, *52*, 1785–1795. [[CrossRef](#)]
19. Jang, Y.; Jovanovic, M.M.; Panov, Y. Multiphase buck converters with extended duty cycle. In Proceedings of the IEEE Applied Power Electronics Conference (APEC'06), Dallas, TX, USA, 19–23 March 2006; pp. 38–44.
20. Jang, Y.; Jovanović, M. Non-isolated Power Conversion System Having Multiple Switching Power Converters. U.S. Patent 7,230,405, 12 June 2007.
21. Rating and Derating for Low-Voltage Multilayer Ceramic Capacitors (MLCCs). Available online: <https://napp.nasa.gov/files/25843/2013-Teverovsky-pres-MLCCsBME-n263.pdf> (accessed on 19 March 2018).
22. Stewart, J.; Neely, J.; Delhotal, J.; Flicker, J. DC link bus design for high frequency, high temperature converters. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 52–55.
23. Choi, D.H.; Randall, C.; Furman, E.; Ma, B.; Balachandran, U.B.; Zhang, S.; Lanagan, M. Energy and power densities of capacitors and dielectrics. In Proceedings of the 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), Chicago, IL, USA, 3–6 May 2015; pp. 52–55.
24. Biba, D.R.; Musuroi, S.; Svoboda, M. A new approach to lifetime and loading stress level estimation for Multilayer Ceramic Capacitors in Electronic Control Units. In Proceedings of the 2017 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM) 2017 Intl Aegean Conference on Electrical Machines and Power Electronics (ACEMP), Brasov, Romania, 25–27 May 2017; pp. 37–42.

25. Jiang, W.; Hu, Y.; Bao, S.; Lijie, S.; Yuwei, Z.; Cui, Y.; Qiang, L. Analysis on the causes of decline of MLCC insulation resistance. In Proceedings of the 2015 16th International Conference on Electronic Packaging Technology (ICEPT), Changsha, China, 11–14 August 2015; pp. 1255–1257.
26. Scarpulla, J.; Ayvazian, T.; Buell, W.; Campbell, M.; Dubitsky, A.; Lin, R.; Martin, W.; Moss, S.; Nuccio, S.; Yarbrough, A.; et al. Thin MLCC (multi-layer ceramic capacitor) reliability evaluation using an accelerated ramp voltage test. In Proceedings of the IEEE Accelerated Stress Testing Reliability Conference (ASTR), Pensacola Beach, FL, USA, 28–30 September 2016; pp. 1–12.



© 2018 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).