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Hybrid Multilevel Converters: Topologies, Evolutions and Verifications

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Abstract: Multilevel converters have good potential in high power and high voltage applications due to their advantages of reduced voltage or current stress on power devices. In recent years, hybrid multilevel converter (HMC) have attracted increasing attention since less equipment is required. In this paper, the topologies and evolutions of HMCs are presented, where five topology derivation ways are given by using basic cells in series-parallel/parallel-series. Some general topologies or structures that are used to generate higher levels are also deducted. Then many existing HMCs can be derived, and new topologies of the HMC might be inspired. The capabilities of neutral point and FC voltage balancing control are investigated. The performance of the selected FC-based HMCs is analyzed. Finally, the verifications of operation principle and control strategies for the derived HMCs are carried out.

Keywords: evolutions; hybrid multilevel converter; modulation; multilevel converters; voltage balancing control

1. Introduction

Multilevel converters have superior characteristics over two-level converters such as lower dv/dt, lower switching losses and better output quality [1–4]. With the capability of handling high voltage and high power, the multilevel converters (MLCs) are widely used in medium- and high-voltage (>3 kV) power conversion systems [1,2]. MLCs are also suitable in low-voltage (<380 V) power applications, due to the reduced output filter volume or enhanced fault-tolerant capability they may achieve [3,4].

Nowadays, the most common topologies of voltage source MLCs are the diode neutral-point-clamped (NPC) converter [5,6], flying capacitor converter (FCC) [7], cascaded H-bridge (CHB) converter [8,9] and modular multilevel converter (MMC) [10,11]. Three-level NPC converters have been widely used in high-power motor drives and renewable energy conversions. However, as the number of levels increases, the clamping diodes and unbalanced loss distributions will increase rapidly. Due to its merits of the absence of diodes and balanced loss distributions, the FCC is a good alternative for high-level applications. Nevertheless, a large number of flying capacitors (FCs) may reduce system reliability and increase the initial price. Hybrid multilevel converters (HMCs) are new emerging converters which have attracted more and more attention in some applications with high power or high reliability requirements, such as renewable power generation systems and electric aircraft [12–22]. In recent years, some HMCs including active NPC (ANPC) converters [13–17], three-level T-type converter (also known as neutral point piloted converter, NPPC) [18], nest NPC (NNPC) converter [19–21], and nest T-type NPC converter [22] have found industrial applications. Developing new multilevel topologies is still of great significance since most topologies may be

not suitable for new emerging applications and are difficult to implement in commercialized uses. For example, the three-level T-type converter was invented several decades ago [18], but it has only been studied and applied in recent years for low-voltage applications (e.g., photovoltaic grid-connected system) due to its low conduction losses and superior output quality [4,23,24]. There are several papers in the literature [1–6,9], focusing on the topology review of the multilevel converters, and their modulation and control strategies were reviewed in [25–27]. However, topology reviews and control strategy of HMCs have rarely been presented in the scientific literature.

The main contributions of this paper are to find derivation ways of HMC topology, especially for the FC-based HMCs. Five evolutions of the HMC are presented by using basic cells in series-parallel/parallel-series and adding/removing power devices, with which many existing and new HMC topologies can be derived. The capabilities of the neutral point (NP) voltage and FC voltage balancing control are investigated and taken into consideration in the topology derivation process. Finally, the fundamental operating principle of three derived HMCs is validated experimentally.

2. Hybrid Stacked Multicell Converters

A large number of multilevel converter topologies have been developed in recent decades to meet the requirement of different applications. Figure 1 shows the classification of multilevel converters, where five existing and emerging hybrid multilevel converters, including hybrid clamped, hybrid cascaded, hybrid FC-based ANPC, hybrid FC-based multicell, and hybrid sub-module multilevel converters are highlighted and discussed in this paper.

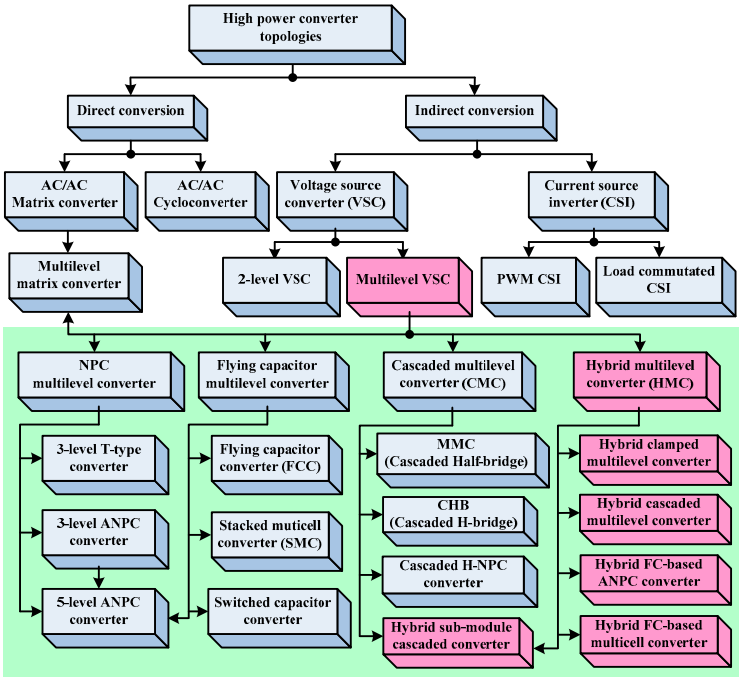


Figure 1. Classification of multilevel converters.

2.1. Basic Switching Cells

Figure 2 shows two-level and multi-level basic switching cells, named two-level (2L) cell, three-level H-bridge (3L HB) cell, three-level FC (3L FC) cell, three-level NPC (3L NPC) cell, three-level active NPC (3L ANPC) cell and three-level T-type (3L T-type) cell, respectively. Any HMCs can be derived by stacking the basic cells in adding or removing some devices. The basic cells included in an HMC topology may be one or more cell types, but the cell type is usually limited to two to simplify the topology and reduce the control complexity.

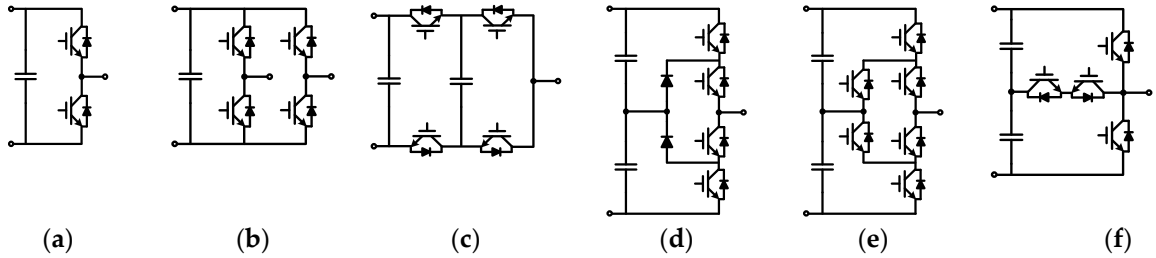


Figure 2. Basic switching cells. (**a**) 2L cell, (**b**) 3L HB cell, (**c**) 3L FC cell, (**d**) 3L NPC cell, (**e**) 3L ANPC cell, (**f**) 3L T-type cell.

2.2. Hybrid Clamped Multilevel Converters

The ANPC converter is a newly introduced HMC, which combines the advantages of NPC and FCC [13]. In this paper 3L ANPC is considered as basic cell, and from which other HMC such as 5L ANPC can be derived. To demonstrate the derivation principle, the derivation of basic 3L ANPC is also presented, as shown in Figure 3. The basic 3L NPC cell shown in Figure 3b can be seen as a combination of series 2L cell and two clamped diodes. The 3L ANPC is obtained by replacing the clamped diodes of 3L NPC with active switches, as shown in Figure 3c [13,14].

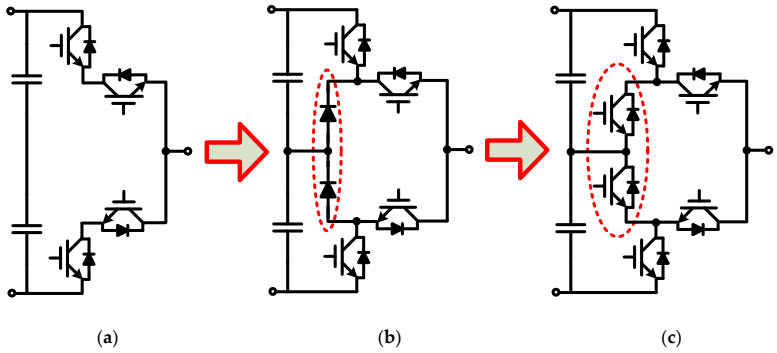


Figure 3. Derivation process of 3L ANPC converter. (**a**) 2L cell [28], (**b**) 3L NPC converter [5], (**c**) 3L ANPC converter [13].

Applying the same derivation principle, a 3L T-type cell with series switches can be seen as a basic cell which is used to derive stacked NPC converters. Figure 4 shows the derivation process of 3L active stacked NPC converter. The 3L stacked NPC converter is derived by adding two clamped diodes into a 3L stacked converter, and then 3L active stacked NPC is obtained by replacing the clamped diodes with active switches as shown in Figure 4b,c [28–30].

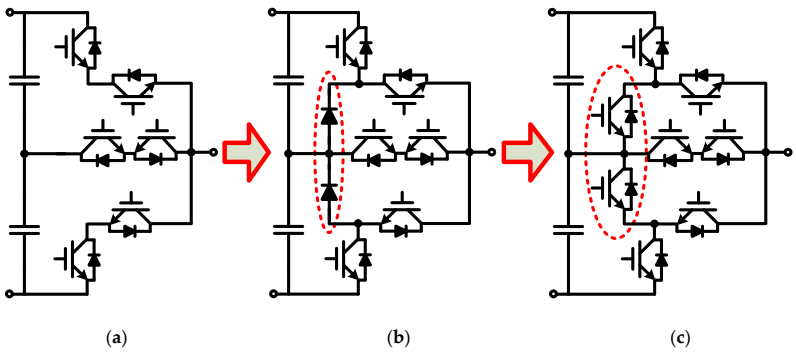


Figure 4. Derivation process of 3L active stacked NPC converters. (**a**) 3L stacked converter [28], (**b**) 3L stacked NPC converter [29], (**c**) 3L active stacked NPC converter [30].

The stacked multicell (SM) (also named nested neutral point piloted, NNPP) converter is a kind of HMC [28], and it owns some merits, such as modularity and inherent natural voltage balancing of FCs. Figure 5 shows the derivation process of 4L NNPC converter [22], and 5L SM converter [28]. The 4L NNPC converter shown in Figure 5b can be obtained with adding into a 3L FC one bidirectional active switch between the neutral point of the FCs and ac output terminal. The 5L SM converter can be obtained by adding a bidirectional active switch into the 4L NNPC between the neutral points of the FCs and dc-link capacitors, as shown in Figure 5c.

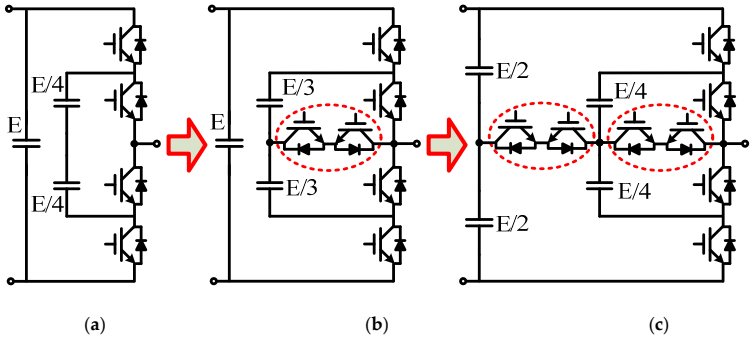


Figure 5. Derivation process of 5L SM converter. (**a**) 3L FC cell [7], (**b**) 4L NNPC converter [22], (**c**) 5L SM converter [28].

Figure 6 shows the derivation process of 5L SM converter and 4L π-type converter [31]. Figure 6 shows the 5L SM converter is formed by stacking two 3L T-type cells horizontally, and 4L π-type converter can be seen as a combination of two T-type cells vertically. More T-type cells should be stacked horizontally and vertically to extend the voltage levels, and then the corresponding general topologies are shown in Figure 6d,e.

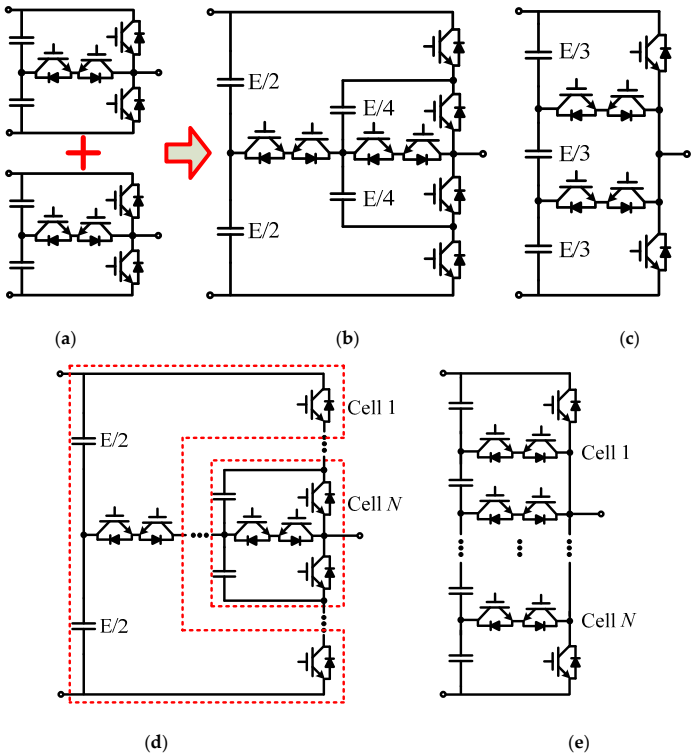


Figure 6. Derivation process of hybrid multilevel converters. (**a**) 3L T-type cell [18], (**b**) 5L SM converter, (**c**) 4L π-type converter [31], (**d**) general topology of SM converter, (**e**) general topology of π-type converter.

Figure 7 shows another derivation way of 4L NNPC converter [19]. The 4L NNPC is derived by nest stacking a 2L cell and a 3L NPC as shown in Figure 7. To illustrate the derivation principle, the output of the 2L cell is firstly separated into two terminals, and then connected with the dc-side terminals of 3L NPC. As 3L NPC is replaced with 3L ANPC and 3L T-type converter, 4L nest ANPC and 4L nest T-type NPC converter [22] are derived, respectively. Figure 8 shows three hybrid clamped topologies of 4L nest NPC converters.

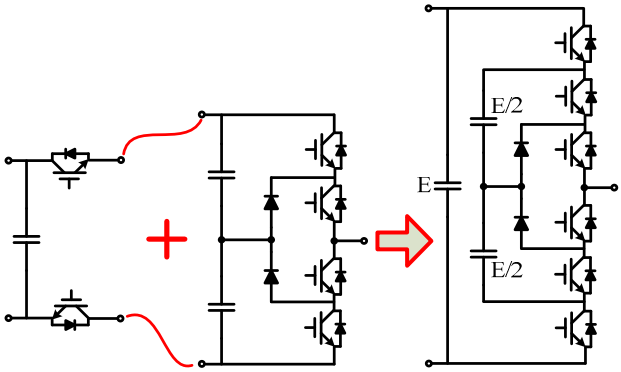


Figure 7. Derivation process of 4L NNPC converter.

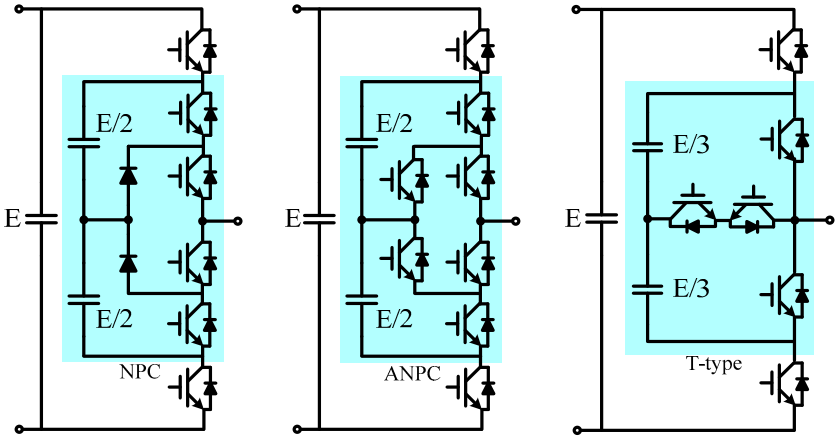


Figure 8. Hybrid clamped nest NPC converters. (**a**) 4L NNPC converter [19], (**b**) 4L nest ANPC converter, (**c**) 4L nest T-type NPC converter [22].

2.3. Hybrid Cascaded Multilevel Converters

Some HMCs are derived by cascading one or two types of basic cells in parallel or series. Figure 9 shows a 5L double flying capacitor ANPC (DFC-ANPC) converter [32] and a 9L symmetric hybrid converter [33] obtained by combing two 3L FC cells and one 2L/3L HB cell, respectively. The switches of 3L FC cells operate in high frequency (HF) while switches of the 2L/3L-HB cell operate in low frequency (LF). Due to the topology characteristics, redundant switching states are generated which can be selected flexibly to balance the FC voltage. 3L FC cells can be higher level cells, and 2L/3L-HB cell can also be higher-level cells (e.g., 3L NPC, 3L ANPC, and 3L T-type) to increase the voltage level [34]. Figure 10 shows general topologies of hybrid cascaded multilevel converters.

A large number of FC will reduce the power density of the specific converters. To increase the voltage level with reduced FC, 3L FC cells in Figure 9 can be replaced with 3L ANPC, and 3L T-type cells, the corresponding topologies are shown in Figure 11a,b, respectively [35,36]. The number of levels will be increased by cascading HB cells. To extend the voltage level, Figure 11c shows the general structure of the hybrid cascaded HB converter. It should be noted that the fundamental multilevel cell

can be any topology. For example, if the fundamental cell is 5L ANPC and one HB is cascaded, a 9L hybrid cascaded HB converter can be derived [37]. A 17L converter formed by cascading 3L FCC and HB cells is proposed in [38]. The modularity characteristic provides the hybrid cascaded HB converters with fault-tolerant capability, thereby enhancing the system reliability.

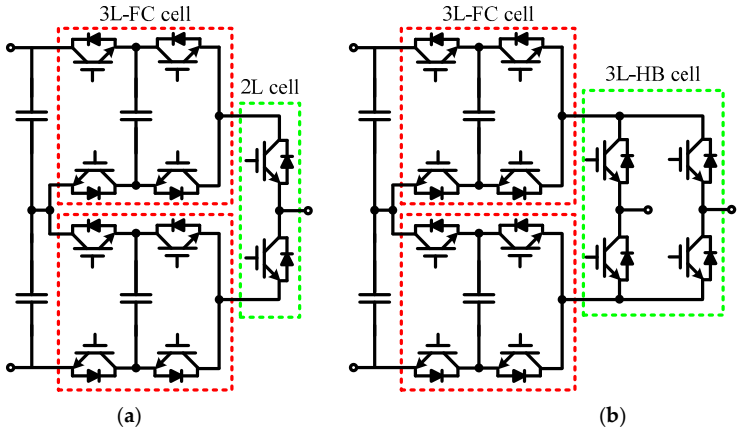


Figure 9. Hybrid multilevel converters based on cascading basic cells. (**a**) 5L DFC-ANPC converter [32], (**b**) 9L symmetric hybrid converter [33].

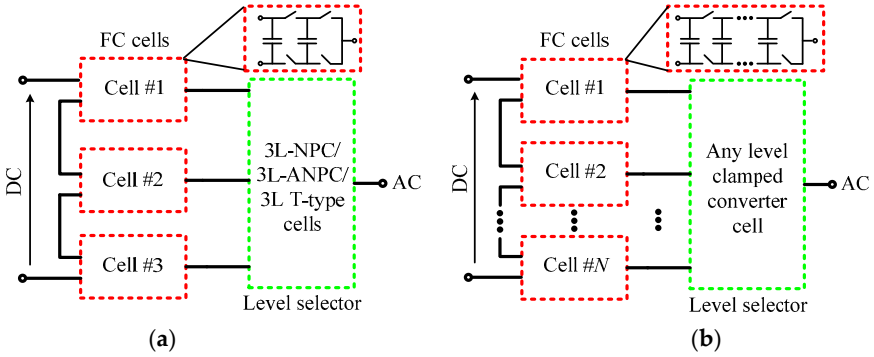


Figure 10. General topologies of hybrid cascaded multilevel converters by cascading (**a**) three 3L FC cells, (**b**) N-cell multilevel FC cells.

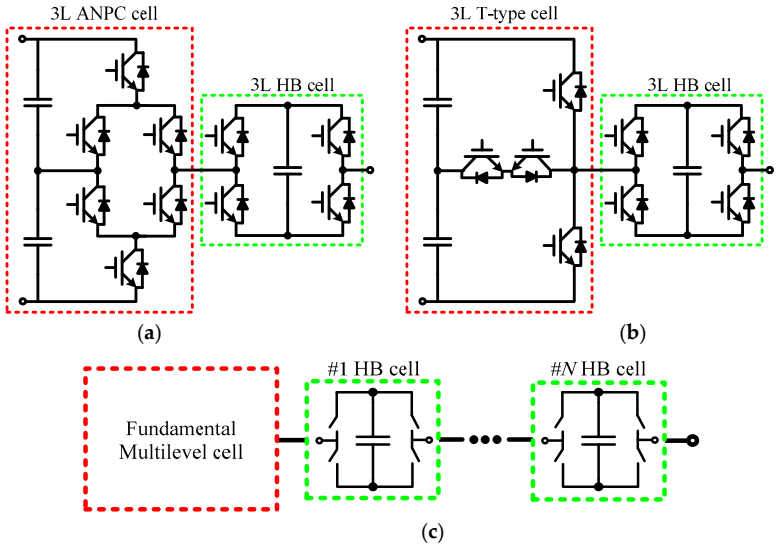


Figure 11. Hybrid cascaded HB converters (**a**) based on 3L ANPC cell [35], (**b**) based on 3L T-type cell [36], (**c**) general structure with N HB cells.

If an *m*-level fundamental cell id cascaded with *N* HB cells, the output voltage level can be calculated by:

$$L = 2^m \cdot (N - 1) + 1 \quad (1)$$

2.4. Hybrid FC-Based ANPC Multilevel Converters

The evolution of hybrid FC-based ANPC multilevel converters is shown in Figure 12. 5L ANPC can be seen as a combination of 3L ANPC cell and 2L cell [39], as shown in Figure 12a. Firstly, the ac side output of 3L ANPC is separated into two terminals, and then they are connected with dc-side terminals of the 2L cell. Similarly, if a 3L T-type cell substitutes 2L cell, a new 5L hybrid T-type ANPC (T-ANPC) converter is derived [40], as shown in Figure 12b. Figure 12c shows the general structure with *N* FC-based cells for generating higher levels, where 3L ANPC is recognized as a fundamental cell, and it can be other topologies. Figure 13 shows three general topologies of hybrid FC-based ANPC converters [39–41].

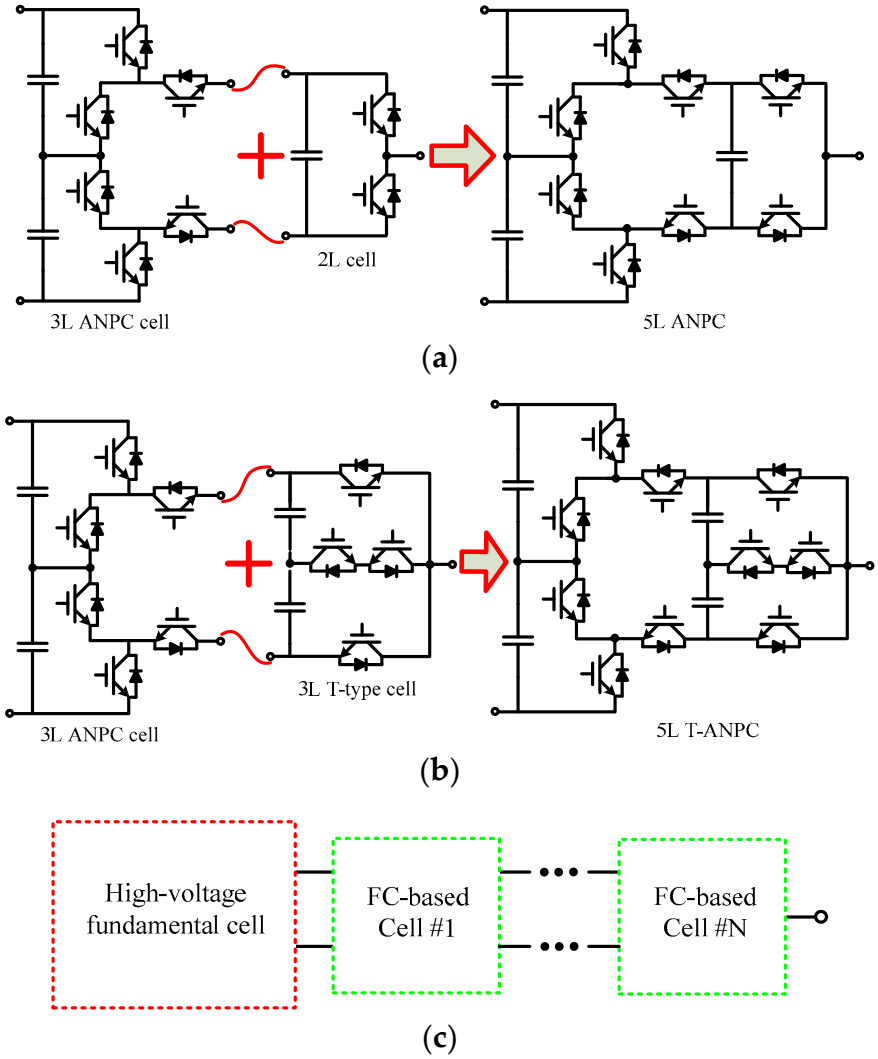


Figure 12. Derivation process of hybrid FC-based ANPC converters. (**a**) 5L ANPC, (**b**) 5L hybrid T-ANPC [40], (**c**) general structure with N FC-based cells.

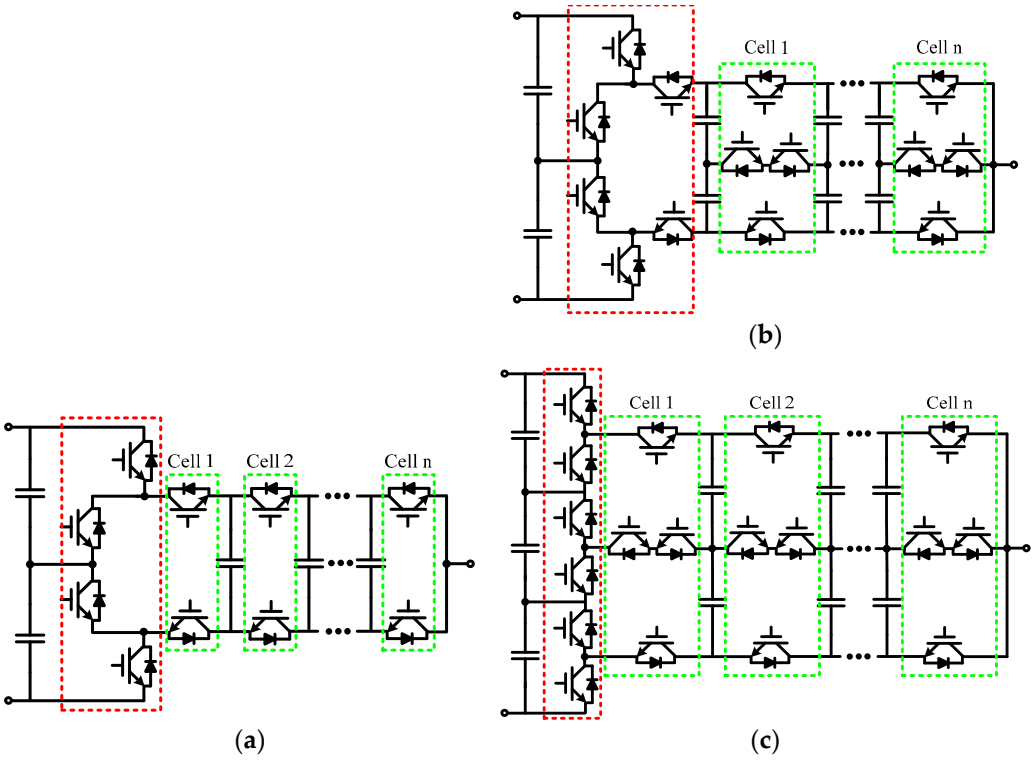


Figure 13. General topologies of hybrid multicell based ANPC converters. (**a**) (2n + 1)-level ANPC with n FC cells [39], (**b**) (4n + 1)-level hybrid T-ANPC with n T-type cells, (**c**) $(3 \times 2^{n-1} + 1)$-level hybrid ANPC converter with n T-type cells.

2.5. Hybrid FC-Based Multicell Converters

In order to reduce the required devices (including dc sources, switches, and FCs), several FC-based hybrid multicell converters, which are based on the original FCC and SM converters have been proposed in [42–50]. In [42,43], the number of dc sources was reduced to half by adding LF switches to the original SMC. In [44], a mixed stacked multicell converter was proposed to double the RMS value of output voltage, which is obtained by adding four LF switches to the SM converter.

To further reduce the number of LF and HF switches, hybrid FC-based multicell converters have been proposed based on the original FCC and SM converters by introducing only two LF switches, as shown in Figure 14a,b, respectively [45,46]. For obtaining an identical output level, the number of HF switches is reduced to half whereas the RMS value of the output voltage is doubled by comparing with their original topologies. Figure 14c shows the general structure that includes one LF cell and n FC-based HF cells. It should be noted that a higher number of levels can be obtained by stacking more LF and FC-based HF cells. By using this derivation method, a 17L reduced-component hybrid FC-based multicell converter is derived in [47]. Figure 15a shows a hybrid converter named duo-active-neutral-point-clamped multilevel converter, and it is derived by introducing one LF cell to the original ANPC [48,49]. Following the same derivation principle, a new hybrid converter can be obtained from the hybrid T-ANPC converter, as shown in Figure 15b. The general structure is shown in Figure 15c. The derivation ways in this section may reduce the number of HF switches, FCs, and meanwhile double the RMS value of output voltage (i.e., $2V_{dc}$) and improve the quality of output waveforms.

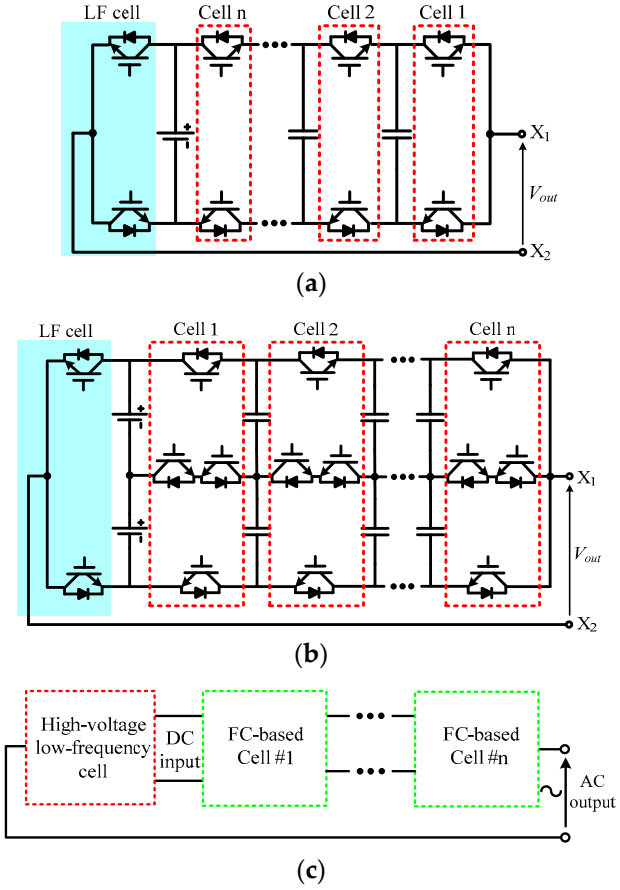


Figure 14. General topologies of hybrid FC-based multicell converters. (**a**) (2n + 1)-level double flying capacitor multilevel (DFCM) converter with n FC cells [45], (**b**) (4n + 1)-level reduced SM converter with n T-type cells [46], (**c**) general structure with n FC-based cells.

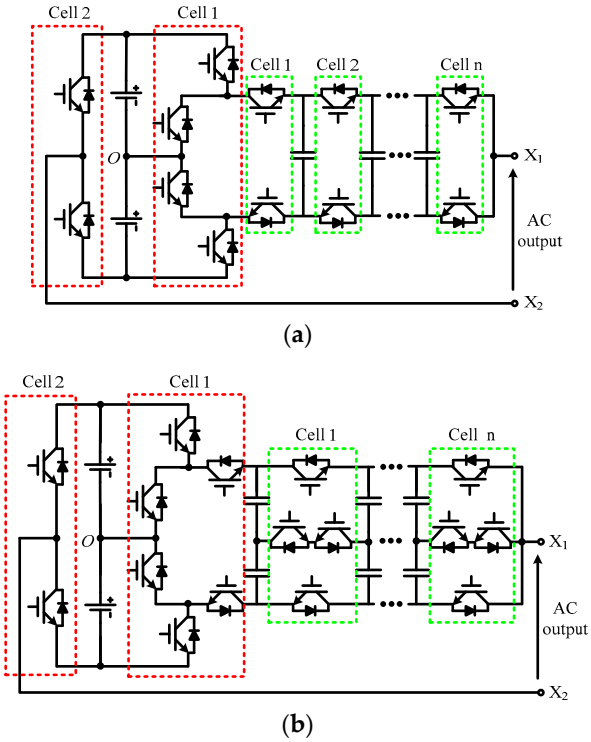
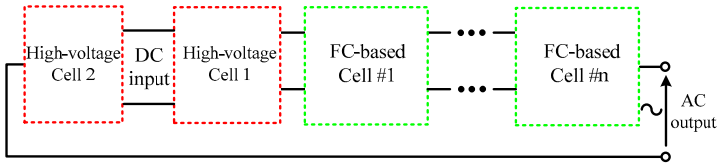


Figure 15. *Cont.*



(**c**)

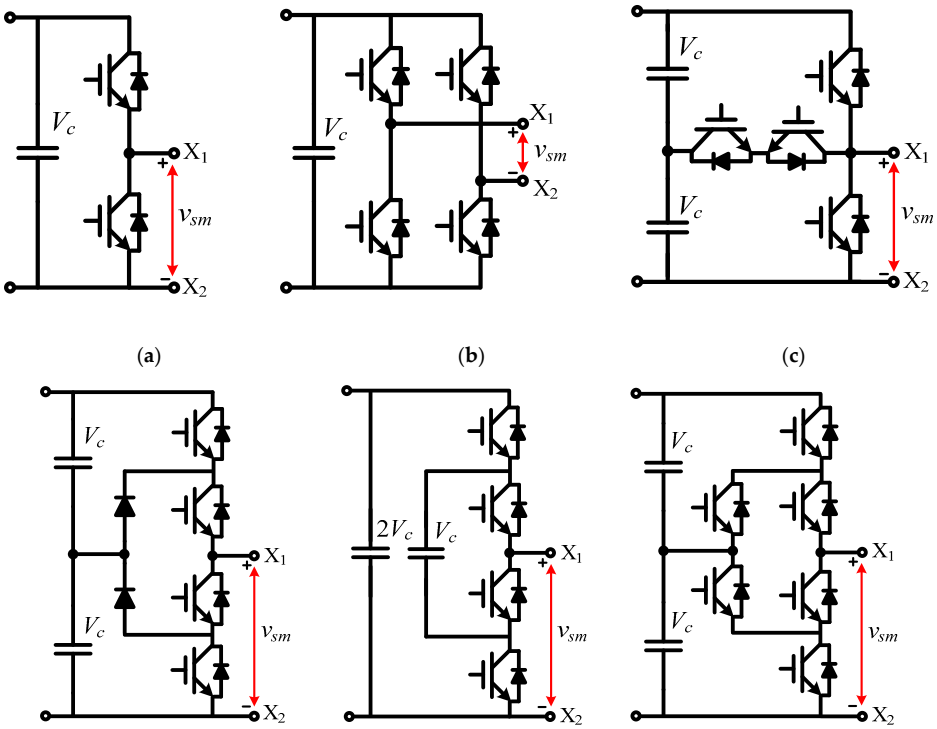
Figure 15. General topologies of hybrid ANPC H-bridge multilevel converters. (**a**) (4n + 1)-level hybrid ANPC H-bridge converter with n FC cells [49], (**b**) (8n + 1)-level hybrid T-ANPC H-bridge converter with n T-type cells, (**c**) simplified general structure with n FC-based cells.

2.6. Hybrid Sub-Module Multilevel Converters

For power converters, modularity means a cascaded connection of sub-module, which is an attractive solution to tolerant high-voltage and obtain high-quality waveforms [51,52]. During past decade, many modular multilevel converter (MMC) topologies have been proposed [53–69], and they are becoming attractive in both academic research and industrial applications.

2.6.1. Basic Cells

The sub-module of the MMC could be established by basic cells and connected in series and parallel to meet the requirement of specific applications, such as high-voltage dc transmission (HVDC), high power motor drive and so on. Figure 16 shows the structures of the basic cell, where 2L half-bridge sub-module (HBSM) and 3L full-bridge sub-module (FBSM) are most common used. The basic cells may adopt multilevel converter cell to increase the output voltage levels, such as 3L neutral-point-clamped sub-module (NPCSM) [5], 3L flying capacitor sub-module (FCSM) [7], 3L active NPC sub-module (ANPCSM) [13], and 3L T-type multilevel sub-module (TMSM) [18].



(**a**) (**b**) (**c**)

(**d**) (**e**) (**f**)

Figure 16. Structures of basic cell. (**a**) 2L HBSM, (**b**) 3L FBSM, (**c**) 3L TMSM, (**d**) 3L NPCSM, (**e**) 3L FCSM, (**f**) 3L ANPCSM.

2.6.2. Hybrid Sub-Modules

By combing the HBSM and FBSM cells, hybrid sub-modules can be derived to achieve desired functions and characteristics, as shown in Figures 17–19. A double-half-bridge-series sub-module (DHBSSM) is generated by the connection of two HBSM cells in series, as shown in Figure 17b [53]. Another asymmetrical double HBSM is shown in Figure 17c, which is derived by connecting two HBSM cells in parallel and can generate four-level output. The derived sub-modules by connecting two FBSM cells in series or parallel are shown in Figure 18 [54–56]. A hybrid-series-connected sub-module (HSSM) is obtained by combining HBSM and FBSM cells in series [57], as shown in Figure 19. It can output an asymmetric four-level voltage between output terminals.

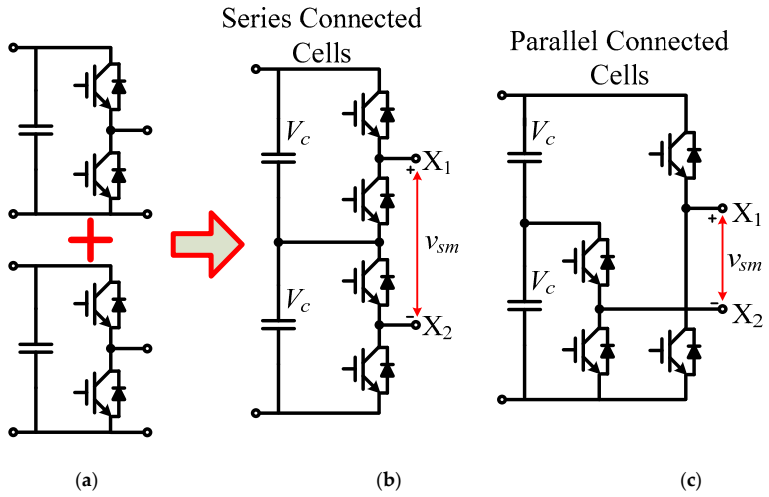


Figure 17. Derivation of multilevel sub-modules with HBSM cells. (**a**) basic cells, (**b**) DHBSSM, (**c**) Asymmetrical double HBSM.

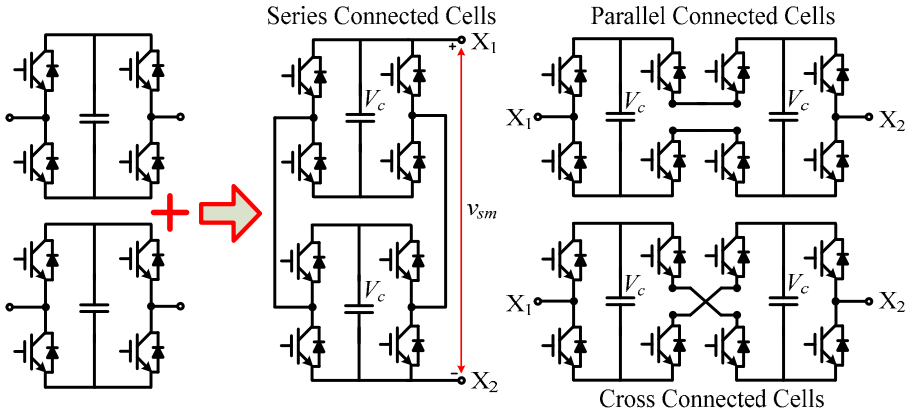


Figure 18. Derivation of multilevel sub-modules with FBSM cells.

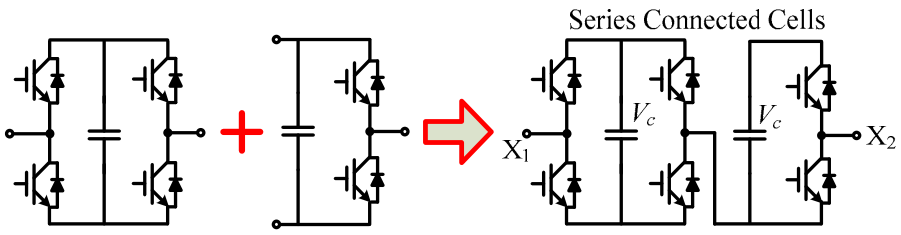


Figure 19. Derivation of hybrid-series-connected sub-module (HSSM) with FBSM and HBSM cells.

In order to promote reliability of HVDC transmission system with overhead lines, new hybrid sub-modules with inherent DC fault blocking capability have been proposed in [57–64]. The hybrid sub-modules with asymmetrical DC fault blocking capability includes HSSM, clamp-double sub-module (CDSM) [58], diode-clamp sub-module (DCSM) [59], and switched capacitor sub-module (SCSM) [60]. The hybrid sub-modules with symmetrical DC fault blocking capability includes FBSM, series-connected-double sub-module (SCDSM) [61], cross-connected-double sub-module (CCDSM) [62], clamp-circuit sub-module CCSM) [63], and active clamped T-type sub-module (ACTSM) [64]. Figure 20 gives the topology of some typical hybrid sub-modules.

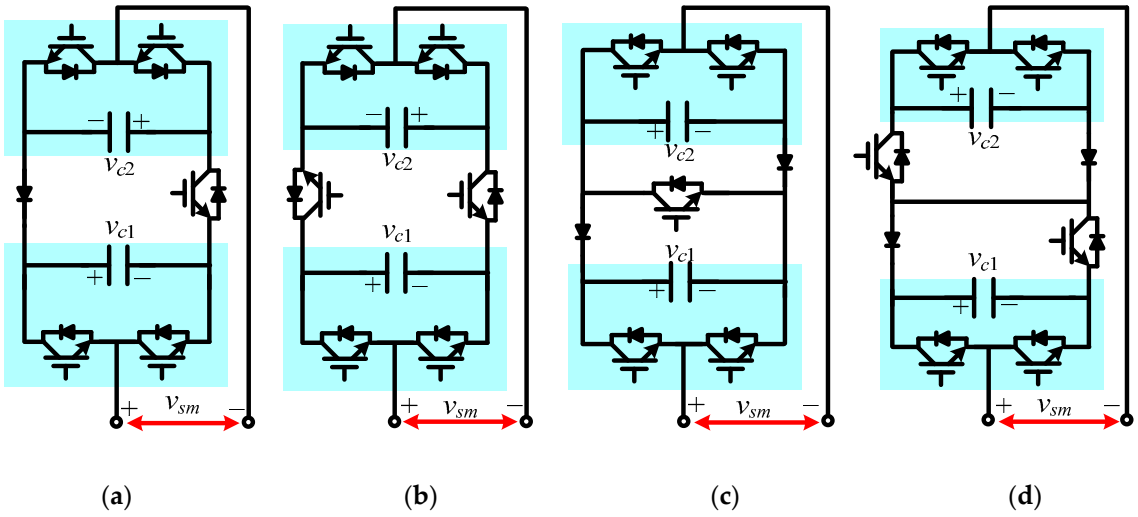


Figure 20. Topology of hybrid sub-modules with DC fault blocking capability. (**a**) SCDSM [61], (**b**) CCDSM [62], (**c**) CDSM [58], (**d**) CCSM [63].

Obviously, more devices are adopted in the single hybrid sub-module than the HBSM. However, the hybrid sub-module based MMC may be favorable in some specific applications, such as flexible HVDC transmission system with DC fault blocking capability, multiple voltage levels with minimizing devices.

Five topology evolutions and simplified general structures of HMCs have been illustrated above. Many existing and new HMCs can be obtained for various energy conversion systems. The voltage balancing properties of NP and FC are critical issues that should be taken into consideration during topology evolutions. Figure 21 shows the derivation process of the HMC which includes three steps: 1) Evolving new topologies based on basic cells; 2) Analysis of FC voltage balancing capability; 3) Analysis of dc-side NP voltage balancing capability.

It should be noted that the balance of dc-side NP voltage may be realized by three phases or back-to-back configurations, so the balance of FC voltage should be given more priority than that of NP voltage. Typically, the FCs should operate in high frequency mode, and only switching harmonics exist in the FC voltage. For a certain current direction, the redundant switching states can be selected flexibly to balance the FC voltage by charging or discharging the FCs over each switching cycle.

Due to its intrinsic redundancy and modularity, cascaded multilevel inverter (MLI) achieves high-quality outputs and high reliability [9]. The MLI has been recognized as an important alternative in medium-voltage applications, and many symmetrical and asymmetrical MLI topologies have been proposed by researchers. To boost the number of levels with reduced devices, a level doubling network (LDN) was proposed for the cascaded MLIs [65]. The LDN is achieved by adding a capacitor fed half bridge [65,66,69,70] or a full bridge [67,68] to the MLI topologies. The LDN doubles the voltage levels of a multilevel converter, and it is proven not to consume power during a fundamental cycle. The LDN may also be applicable to other single-phase and three-phase multilevel converters to increase the voltage levels, thereby reducing the size and cost of power filters [71,72].

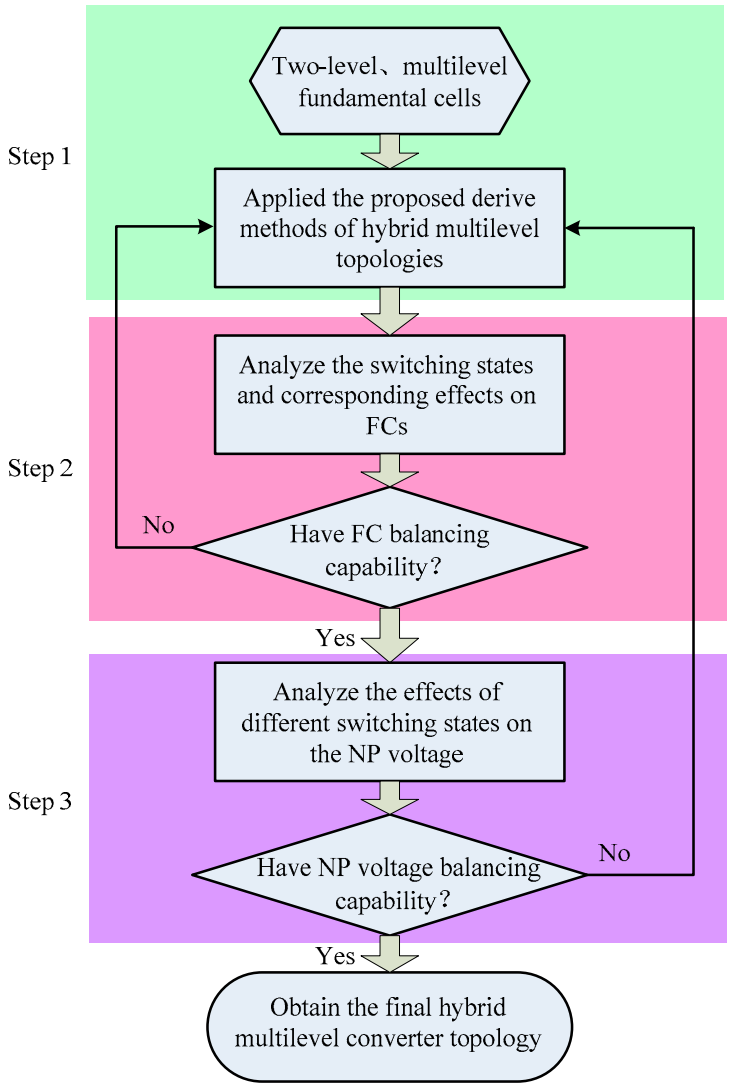


Figure 21. Derivation process of the HMCs.

3. Performance Evaluations of Hybrid FC-Based Multilevel Converters

The number of devices and their ratings are crucial for multilevel converters since they govern converter cost, control complexity, and system reliability. In this section, the most common used FC-based multilevel converters such as FCC, ANPC, SM and some emerging FC-based converters are evaluated. Table 1 shows comparison results among 9L hybrid FC-based multilevel converters, where the number of switches, FCs, dc sources, the peak-to-peak value of output voltage and total standing voltage are evaluated. The results show that the FCC and SM converters have less total standing voltages, but they require more HF switches and FCs. The topology shown in Figure 13b [40], which is the combination of ANPC and SM converters, requires more devices and total standing voltage. In [50], the hybrid cascaded multilevel converter does not require FC, but it needs four isolated dc sources and more switches. The topology arising from Figure 11c [34] reduces the total standing voltage with lower voltage devices, whereas it requires more FCs and HF switches. The modified 9L ANPC shown in Figure 9b [33] and in Figure 11c [37] requires an additional two more LF switches, and the total standing voltages are higher than the hybrid stacked multicell (HSM) converter presented in Figure 14b [46].

Table 1. Comparison of 9-level FC-based multilevel converters.

Topologies	Number of Devices				Output Voltage (p.u)	Total Standing Voltage (p.u)
	LF Switch	HF Switch	FC	dc Source		
FCC [7]	0	16	7	1	1	2
ANPC [13]	4	8	3	1	1	3
SM [28,40]	0	16	6	1	1	3
	4	10	4	1	1	6
[50]	4	8	0	4	2	6
[34]	2	12	3	2	1	4.5
[37]	4	8	2	1	1	7
[33]	4	8	2	1	1	6
HSM [46]	2	8	2	1	2	5

Note: DC source voltage is equal to V_{dc}, 1 p.u. = V_{dc}.

It can be seen from Table 1 that the HSM requires less device than other 9L FC-based multilevel converters. To further evaluate its characteristics, the comparison of capacitor stored energy against the common used FC-based multilevel converters FCC, ANPC, SM for generating an identical output voltage (9L, $2V_{dc}$, peak-to-peak value) is studied, as shown in Table 2. The result shows that the HSM converter has the lowest stored energy in capacitors. In high-voltage conversion systems, several low voltage rating switches may be connected in serious to block high voltage if a two-level converter is used. Similarly, low current rating switches may be connected in parallel to meet the high power output requirement. However, the parametric inconsistency may exist among the series- and parallel-connected switches, which may influence the converter performance. The multilevel converters can be used in high-voltage high-power applications while avoid direct series- or parallel connection. To obtain low cost and good performance, the switches with proper voltage ratings should be selected. Table 3 shows the comparison of voltage rating for FC-based multilevel converters.

Table 2. Capacitor stored energy for FC-based multilevel converters.

Topologies	Stored Energy in Capacitors
FCC [7]	$\varepsilon_{FCM} = \sum_{i=1}^{7} \frac{C}{2}\left(i\frac{V_{dc}}{4}\right)^2 + 2\cdot\frac{CV_{dc}^2}{2} = \frac{83}{8}CV_{dc}^2$
ANPC [13]	$\varepsilon_{ANPC} = \sum_{i=1}^{3} \frac{C}{2}\left(i\frac{V_{dc}}{4}\right)^2 + 2\cdot\frac{CV_{dc}^2}{2} = \frac{23}{16}CV_{dc}^2$
SM [28]	$\varepsilon_{SM} = 2\cdot\sum_{i=1}^{4} \frac{C}{2}\left(i\frac{V_{dc}}{4}\right)^2 = \frac{15}{8}CV_{dc}^2$
HSM [46]	$\varepsilon_{HSM} = 2\cdot\sum_{i=1}^{2} \frac{C}{2}\left(i\frac{V_{dc}}{4}\right)^2 = \frac{5}{16}CV_{dc}^2$

Note: output voltage is 9 level, peak-to-peak value is $2V_{dc}$.

Table 3. Comparison of voltage ratings for 9-level FC-based multilevel converters.

Topologies	IGBTs				FCs				DC Source		
	V_{dc}	$V_{dc}/2$	$V_{dc}/4$	$V_{dc}/8$	$V_{dc}/4$	$V_{dc}/8$	$3V_{dc}/8$	$V_{dc}/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/8$
FCC [7]	0	0	0	16	0	28	0	0	1	0	0
ANPC [13]	0	4	0	8	1	1	1	0	0	2	0
SM [28]	0	0	8	16	2	2	2	0	0	2	0
HSM [46]	2	4	4	0	2	0	0	2	0	2	0

Note: DC source voltage is equal to V_{dc}.

In some specific applications, higher level converters are required to obtain good output quality of waveforms. Therefore, the comparisons of device count are made for the aforementioned general FC-based multilevel converter topologies. Table 4 shows the comparison results of switches and FCs for generating an output voltage with n levels. To make it more comprehensive, Figure 22 shows the

curves of the number of switches and FCs versus the increase of voltage level. Theoretically, the power quality of output waveforms will be improved with the increase of the voltage levels, and then the filter size and cost can be optimized. In practical applications, a proper level should be selected for a specific converter to obtain the desire performance.

Table 4. Comparisons of n-level FC-based multilevel converters.

Topologies	FC cell	Number of Devices		
		LF switch	HF switch	FC
FCC [7]	$n-1$	0	$2(n-1)$	$n-2$
SM [28]	$n-1$	0	$2(n-1)$	$n-3$
[40]	$(n-1)/2$	6	$n-1$	$(n-1)/2$
[41]	$2[\log_2(n-1)/3]+2$	6	$4[\log_2(n-1)/3]+4$	$2[\log_2(n-1)/3]$
HSM [46]	$(n-1)/2$	2	$n-1$	$(n-5)/2$

Note: $N_{\text{level}} = n$, and n is odd; DC source voltage is V_{dc}.

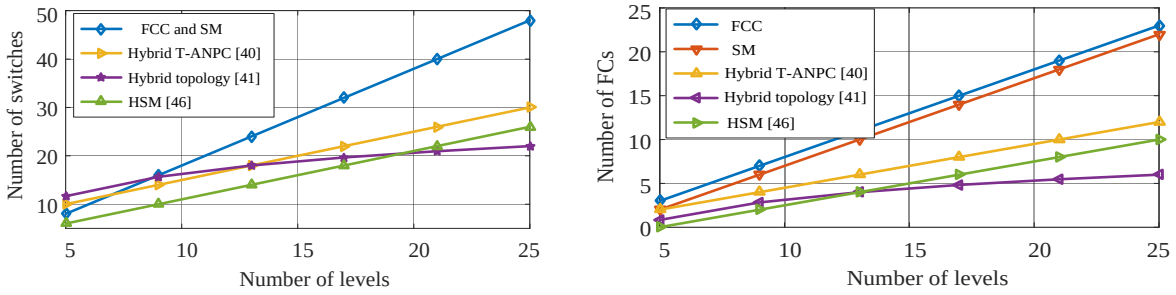


Figure 22. Comparisons of devices among FCs-based multilevel converters. (**a**) Number of switches, (**b**) number of FCs.

For high-voltage applications such as HVDC, a relative high voltage level may be selected for MMCs [51–64,73–77] to meet the required current total harmonic distortion (THD), standing voltages and dv/dt. For medium and low-voltage applications, five and fewer level converters for ANPC [13–17], SM [28], HSM [46] and other FC-based multilevel converters might be optimal at current technical conditions. In recent decades, multilevel converters have been proposed and some converters have been commercialized in motor drivers, flexible alternating current transmission system (FACTS), and HVDC. According to the researches in [1–9,25–27,78], the advantages, disadvantages, modulation techniques, as well as the applications of these commercial converters, are summarized in Table 5.

Table 5. Performance summary of multilevel converters.

Topology	Advantage	Disadvantage	Modulation Technique	Commercial Products
NPC [1–6]	① Simple structure; ② Equalized blocking voltage of power switches.	① Unequal distribution of power losses; ② DC-link voltage balance limits the converter to three-level topology.	① PWM carrier modulation (based zero-sequence injection); ② SVPWM method (based space vector selection).	SM150 (Siemens), ACS1000 (ABB) FACTs, motor driver.
FCC [7,25–28]	① Modular structure; ② Owning a high number of redundant states.	① The poor dynamic response of dc voltage balancing; ② Large amounts of flying capacitors reduce the system reliability.	① Phase-shifted carrier PWM (achieves neutral balancing of flying capacitors).	ALSPA VDM6000 (Alstom) FACTs, motor driver.

Table 5. *Cont.*

Topology	Advantage	Disadvantage	Modulation Technique	Commercial Products
CHB [8,9]	① Modular structure; ②. Owning fault tolerant capability.	① Require independent dc source; ② Isolated transformers increase the system volume.	① Phase-shifted carrier PWM (achieves equalization of power losses).	GH180 (Siemens), PCS6000 (ABB) FACTs, motor driver.
MMC [52–75]	① Modular structure; ② Easy to achieve fault tolerant operation.	① Low frequency voltage oscillation of floating capacitors; ②. Complex data acquisition and communication for each power cell.	① Nearest level modulation (achieves equalization of power losses and dc voltage balance).	SM120 (Siemens) HVDC, wind power application.
T-type NPC [18,23–27]	① Simple structure; ② Low conduction losses.	① Outer switches have to withstand the entire dc-link voltage; ② Not suitable for a high-voltage range	① PWM carrier modulation (based zero-sequence injection); ② SVPWM method (based space vector selection).	Solar Ware Samuri (TMEIC) PV application.
NNPP (SM converter) [28,42–44]	① Modular structure; ② Owning **a** high number of redundant states.	① Unequal blocking voltage of switches. ② Large amounts of flying capacitors reduce the system reliability.	① Phase-shifted carrier PWM (achieves neutral balancing of flying capacitors).	MV6 (GE) Motor driver.
Active NPC [13–17]	① Simple structure; ② Easily extendable to a higher level by stacking flying capacitor cells.	① Unequal usage of switches and flying capacitors. ② Require series switches to handle high voltage.	① Hybrid phase-shifted PWM (low frequency for high voltage switches and high frequency for flying capacitor cells)	ACS2000 (ABB) Motor driver.

4. Modulation and Control Strategies

4.1. General Operation and Control Structure

For each multilevel converter, it is required to develop specific modulation and control strategies to generate proper switching signals for gate drivers according to various control targets. The literature [26,27] studied the well-known modulation and control strategies for the HMCs. Figure 23 shows the general operation and control structure of FC-based multilevel converters for achieving different control targets. In Figure 23, the operation and control structure process can be divided into three steps. The first step is achieving the specific control targets by outer and inner control loops, and then the reference signal v^* of the output voltage can be obtained. For example, in motor drive applications the control loops are designed to regulate the speed, and in the case of grid-connected compensators, the target will be harmonic current or reactive power.

The second step including voltage balancing control of NP and FC is optional according to different topologies and applications. The third step is PWM modulation (i.e., SPWM and SVM algorithms) which is used to generate the switching signals S_i, (i denotes the number of switches) for the converters. It should be noted that step 2 may be included in step 3 when intelligent control such as model predictive control (MPC), sliding mode control is applied. Meanwhile, the modulator will not be required.

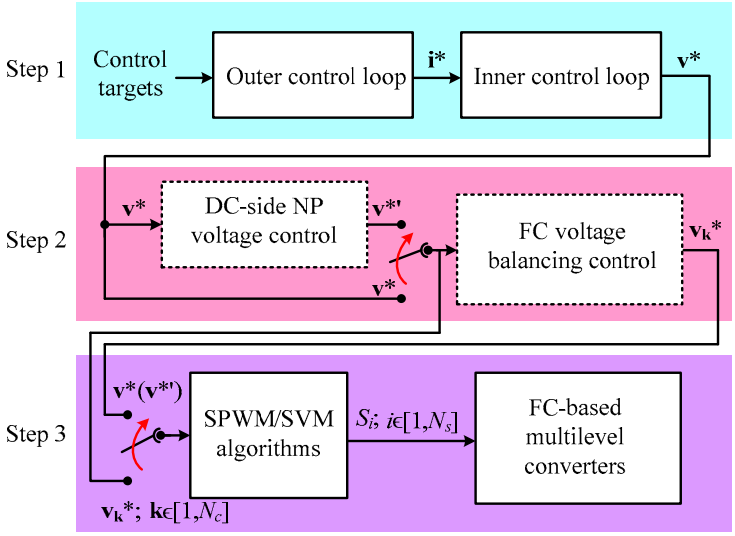


Figure 23. General operation and control structure of the HMCs.

4.2. Pulse Width Modulation Algorithms

Each multilevel converter topology requires proper modulation algorithms in order to achieve minimum losses with highest output performance. The modulation approaches of multilevel converters can be classified into multi-carrier based and vector-based methods, and they are two different methods and have been verified to be equivalent [26,78,79]. Carrier-based pulse width modulation (PWM) is widely used in FC-based multilevel converters and can achieve natural voltage balance of the FCs. Two popular PWM methods named level-shifted PWM (LS-PWM) and phase-shifted PWM (PS-PWM) have been widely used for modulating multilevel converters depending on how the carriers are distributed [80]. Due to the asymmetrical structure of the HMCs, the traditional modulator should be modified for obtaining good performance. For example, the ANPC converter can adopt a hybrid PWM method which is a combination of PS-PWM and LS-PWM methods [81]. In the ANPC and hybrid T-ANPC converters, the switches standing high voltage are operated in LF mode, and the switches standing low voltage are operated in HF mode [82]. Other modulation methods may be more suitable for some specific applications, such as nearest level voltage control (NLC) for modular multilevel converter [83], preprogrammed PWM for low frequency (below 1 kHz) high-power applications (in MW range) [84].

4.3. DC-Link NP Voltage Control

Theoretically, the average currents that flow into and out of the NP should be identical over each fundamental cycle (i.e., 50 Hz) to ensure the voltage balance of the NP [4]. Taking 5L ANPC converter as an example, the output voltage and phase current can be shown in Figure 24. Here the phase current is sinusoidal and in phase with the output voltage (unity power factor) with the modulation index m = 0.9. If the voltage level is E while the output is connected to the NP, the current direction is positive which denotes the current flow out of the NP. If the level is -E while the output is connected to the NP, the current is negative and flows into the NP. The currents that flow into and out of the NP are identical in the duration of -E and E as shown in Figure 24. Similarly, for voltage level 0, the total current that flows through the NP is equal to zero. Therefore, the total current that flows through the NP is equal to zero in each fundamental cycle, which denotes that the NP voltage can be naturally balanced over under a unity power factor.

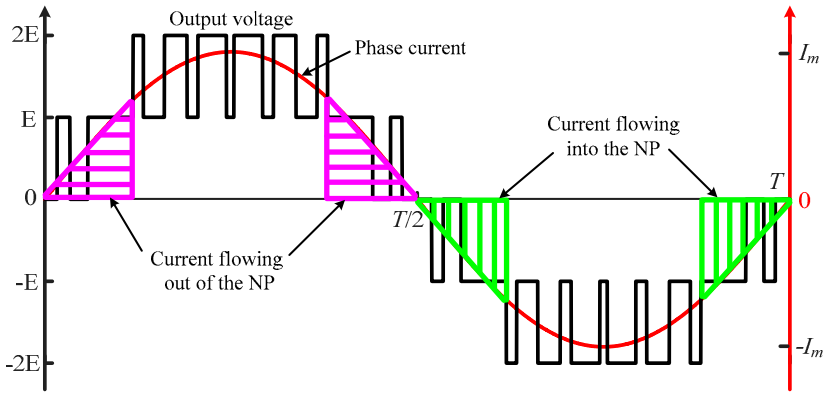


Figure 24. Voltage balancing principle of dc-side NP for 5L converter under the unity power factor.

This analysis principle is also applicable to other multilevel converters with one or more NPs under conditions of any power factors. It should be noted that the voltage balance of the NP is also related with the modulation index, the analysis of NP voltage controllable zone with regards to power factor and modulation index can be found in [85,86].

In the carrier-based modulations, the NP voltage balance problem can be solved by using zero-sequence voltage injection methods [87,88]. In [89], the theoretical analysis and control of the NP voltage balance were put forward for 5L ANPC based on the PS-PWM algorithm. In SVM-based methods, the voltage balance of NP is usually achieved by adjusting the redundant space vectors and their time durations [90]. In [91], an active voltage balancing method was proposed for 5L NNPP converter, which is implemented by using dynamic models. Zero-sequence injection in carrier-based methods and redundant space vector selection in SVM-based methods are verified to be equivalent.

4.4. FC Voltage Balancing Control

For most of FC-based multilevel converters, the FC voltages are balanced by selecting redundant switching states in a single phase. The redundant state selections occur in each switching cycle, and the FC C_f is designed as:

$$C_f = \frac{I_m}{\Delta V_f} \frac{1}{f_s} \tag{2}$$

where, I_m is the peak value of the phase current i_x ($x = a, b, c$), ΔV_f is the allowed voltage ripple of the FC, f_s is the switching frequency.

Numerous voltage balancing control methods have been proposed for FC-based multilevel converters [92–98]. These methods can be classified into two groups: nature voltage and active voltage balancing methods. Nature voltage balancing methods were put forward based on PS-PWM [92,93] and PD-PWM [94,95]. They are easy to be implemented, but the control performances depend on the load power factor and switching frequency. Active voltage balancing methods can be found in [96–98]. In [96], an SVM-based voltage balancing method was proposed, and it is only applicable to three-phase systems. In [97,98], the active voltage balancing method was proposed for 5L SM converter based on the PD-PWM and PS-PWM algorithms, respectively.

The capacitor voltage (including FC and NP) balancing control methods are classified into "single phase method" and "three-phase method" [4]. For the FC-based multilevel converters (e.g., FCM, ANPC, and SM), the voltage balance of FC and NP can be achieved by selecting redundant switching states, which is "single-phase method". For the converters with no redundant states, there is no possibility to use the "single-phase method", so for some NPC converters such as 3L NPC [5], 3L T-type [18] and 4L π-type converters [31] which have no FC and redundant state, the voltage balance of NP can be realized by minimizing the objective cost function $\Delta\varepsilon$. It is defined as:

$$\min\Delta\varepsilon = \min\left\{\sum_{x=a,b,c}\sum_{j=1}^{n}\left(v_{Cxj} - \frac{V_{dc}}{n}\right)i_{Cxj}\right\} \tag{3}$$

where n is the number of capacitors, i_{Cj} is the capacitor current, V_{dc} is the total dc-link voltage, V_{Cj} and i_{Cj} are the capacitor voltage and current, respectively.

5. Operation of Derived HMCs

The hybrid FC-based ANPC converter and hybrid FC-based multicell converter have the advantages of high redundancy, flexible in FC voltage control, easy to balance NP voltage and high capability in tolerant control. So three typical FC-based HMCs are discussed in the following parts.

Figure 25 shows a three-phase hybrid T-ANPC converter connected with *RL*-load. Assuming the dc-bus voltage is V_{dc}, if the reference voltage of the FCs C_{f1} and C_{f2} is set as $V_{dc}/4$ and $V_{dc}/6$, 5L and 7L output voltage will be generated, respectively. The operating principle and control strategy for 5L hybrid T-ANPC were discussed in [40]. The switching states, output voltage and corresponding effects on the FCs of 5L and 7L hybrid T-ANPC converter are shown in Tables 6 and 7, respectively. It is shown in Table 6 that there are redundant switching states which have same output voltage (such as V_2 and V_3) except for V_1 and V_{12} and the redundant switching states can be appropriately selected to balance the FC voltages. If the FC voltages are both controlled at $V_{dc}/6$, v_{ao} can be formulated with switching signals. It has

$$v_{ao} = \frac{1}{2}V_{dc}S_1 + \frac{1}{6}V_{dc}(S_3 + S_{11} + S_{12}) - \frac{1}{2}V_{dc} \tag{4}$$

where S_1, S_3, S_{11}, and S_{12} are switching signals of the switches T_1, T_3, T_{11}, and T_{12}, respectively.

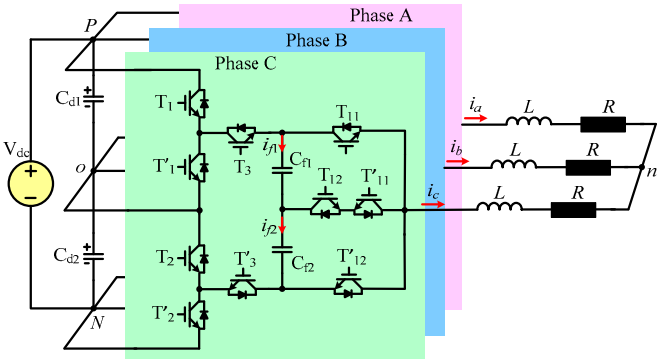


Figure 25. Three-phase hybrid T-ANPC converter connected with *RL*-load.

Table 6. Operation of 5L hybrid T-ANPC converter.

Switching State	LF Switches	HF Switches	Output Voltage	i_{f1}	i_{f2}	C_{f1}, C_{f2} ($i_a > 0$)	
	S_1 S_2	S_3 S_{11} S_{12}	v_{ao}				
V_1	1 1	1 1 1	$V_{dc}/2$	—	—	—	—
V_2	1 1	1 0 1	$V_{dc}/4$	i_a	—	C	—
V_3	1 1	0 0 1	$V_{dc}/4$	—	$-i_a$	—	D
V_4	1 1	1 0 0	0	i_a	i_a	C	C
V_5	1 1	0 0 0	0	—	—	—	—
V_6	0 0	1 1 1	0	—	—	—	—
V_7	0 0	0 1 1	0	$-i_a$	$-i_a$	D	D
V_8	0 0	0 0 1	$-V_{dc}/4$	—	$-i_a$	—	D
V_9	0 0	1 0 1	$-V_{dc}/4$	i_a	—	C	—
V_{10}	0 0	0 0 0	$-V_{dc}/2$	—	—	—	—

"C" represents FC charging; "D" represents FC discharging; "—" represents no current flow through FC.

Table 7. Operation of 7L hybrid T-ANPC converter.

Switching State	LF Switches	HF Switches	Output Voltage	i_{f1}	i_{f2}	C_{f1}, C_{f2} ($i_a > 0$)	
	S_1 S_2	S_3 S_{11} S_{12}	v_{ao}				
V_1	1 1	1 1 1	$V_{dc}/2$	—	—	—	—
V_2	1 1	1 0 1	$V_{dc}/3$	i_a	—	C	—
V_3	1 1	0 1 1	$V_{dc}/3$	$-i_a$	$-i_a$	D	D
V_4	1 1	1 0 0	$V_{dc}/6$	i_a	i_a	C	C
V_5	1 1	0 0 1	$V_{dc}/6$	—	$-i_a$	—	D
V_6	1 1	0 0 0	0	—	—	—	—
V_7	0 0	1 1 1	0	—	—	—	—
V_8	0 0	0 1 1	$-V_{dc}/6$	$-i_a$	$-i_a$	D	D
V_9	0 0	1 0 1	$-V_{dc}/6$	i_a	—	C	—
V_{10}	0 0	1 0 0	$-V_{dc}/3$	i_a	i_a	C	C
V_{11}	0 0	0 0 1	$-V_{dc}/3$	—	$-i_a$	—	D
V_{12}	0 0	0 0 0	$-V_{dc}/2$	—	—	—	—

"C" represents FC charging; "D" represents FC discharging; "—" represents no current flow through FC.

A 9L HSM converter can be arranged similar as s H-bridge converter, as shown in Figure 26. The main circuit consists of LF cell and two T-type HF cells, where switches of the LF cell operate in fundamental frequency, and the switches of the HF cell operate in HF PWM mode. If the dc source voltage is V_{dc}, the voltage of FCs C_{f1} and C_{f2} should be maintained at $V_{dc}/4$. Table 8 shows the switching states, output voltage and effects on the FCs. The output voltage v_a can be synthesized to obtain nine levels ($\pm V_{dc}$, $\pm 3V_{dc}/4$, $\pm V_{dc}/2$, $\pm V_{dc}/4$, 0) by selecting the proper switching state among eighteen states (V_1~V_{18}). These state redundancies can be selected flexibly to charge or discharge FCs for maintaining balanced FC voltages. According to Table 8, the output voltage v_a can be formularized by:

$$v_a = -V_{dc}S_1 + \frac{1}{4}V_{dc}(S_{11} + S_{12} + S_{21} + S_{22}) \tag{5}$$

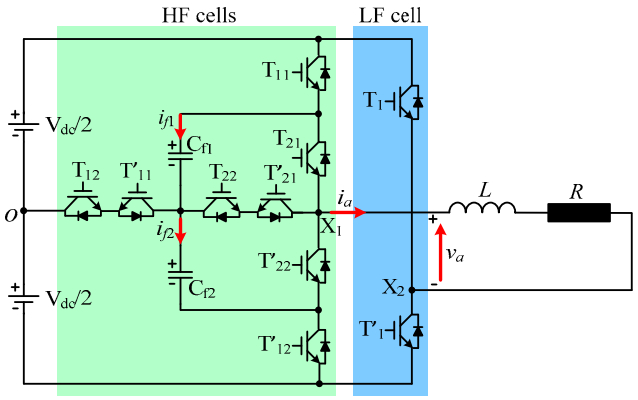


Figure 26. Single-phase 9L HSM converter connected with *RL*-load.

Table 8. Operation of 9L HSM converter.

Switching State	LF-Cell Switch	HF-Cell Switches	Output Voltage	i_{f1}, i_{f2}		C_{f1}, C_{f2} ($i_a > 0$)	
	S_1	S_{11} S_{12} S_{21} S_{22}	v_a				
V_1	0	1 1 1 1	V_{dc}	—	—	—	—
V_2	0	1 1 0 1	$3V_{dc}/4$	i_a	—	C	—
V_3	0	0 1 1 1	$3V_{dc}/4$	$-i_a$	—	D	—
V_4	0	0 1 0 1	$V_{dc}/2$	—	—	—	—
V_5	0	0 0 1 1	$V_{dc}/2$	$-i_a$	$-i_a$	D	D
V_6	0	1 1 0 0	$V_{dc}/2$	i_a	i_a	C	C
V_7	0	0 1 0 0	$V_{dc}/4$	—	i_a	—	C
V_8	0	0 0 0 1	$V_{dc}/4$	—	$-i_a$	—	D

Table 8. *Cont.*

Switching State	LF-Cell Switch	HF-Cell Switches	Output Voltage	i_{f1}, i_{f2}		C_{f1}, C_{f2} ($i_a > 0$)	
	S_1	S_{11} S_{12} S_{21} S_{22}	v_a				
V_9	0	0 0 0 0	0	—	—	—	—
V_{10}	1	1 1 1 1	0	—	—	—	—
V_{11}	1	0 1 1 1	$-V_{dc}/4$	$-i_a$	—	D	—
V_{12}	1	1 1 0 1	$-V_{dc}/4$	i_a	—	C	—
V_{13}	1	0 1 0 1	$-V_{dc}/2$	—	—	—	—
V_{14}	1	1 1 0 0	$-V_{dc}/2$	i_a	i_a	C	C
V_{15}	1	0 0 1 1	$-V_{dc}/2$	$-i_a$	$-i_a$	D	D
V_{16}	1	0 0 0 1	$-3V_{dc}/4$	—	$-i_a$	—	D
V_{17}	1	0 1 0 0	$-3V_{dc}/4$	—	i_a	—	C
V_{18}	1	0 0 0 0	$-V_{dc}$	—	—	—	—

"D" represents capacitor discharging; "C" represents capacitor charging; "—" represents no current flow through FC.

6. Experimental Validations

In this section, the operating principle, modulation and control strategies of three selected FC-based HMCs are validated experimentally. The experimental platform consists of main circuit, voltage and current sensing circuits, controller and PWM driving circuits. The insulated-gated bipolar transistors (IGBTs) IHW15N120E1 and electrolytic capacitors with 820 μF are adopted in the main circuit. A real-time MicroLAB board/module is used to implement the ADC samplings, logical calculations, and control strategies. The dc bus is supplied with a constant dc source, and the ac side terminals are connected to a resistor load through a filtering inductor (L = 4.3 mH, R = 15 Ω).

6.1. Five-Level Hybrid T-ANPC Converter

The hybrid T-ANPC converter is an interesting HMC, and it can operate in different FC voltage ratings $V_{dc}/4$ and $V_{dc}/6$ to generate 5L and 7L voltage, respectively. This feature enables it to obtain higher levels with reduced total standing voltage of switches and FCs. For 5L and 7L hybrid T-ANPC converters, the voltage balance of the FCs is achieved by selecting the redundant switching states at each switching cycle, and the dc-link NP voltage is balanced by using the zero-sequence voltage injection method.

Figure 27 shows steady-state experiment results of 5L hybrid T-ANPC converter connected with three-phase linear *RL*-load. Here, the dc source voltage V_{dc} is 80 V, and a hybrid PS-PWM strategy with carrier frequency f_c = 2 kHz, modulation index m = 0.9 is adopted to generate desired voltage levels. At each voltage level, the FC voltages are balanced and maintained at $V_{dc}/4$ by selecting appropriate switching states according to the current directions and voltage deviations of the FCs. 5L phase voltage and 9L line-to-line voltage are obtained well, as shown in Figure 27a,b. The load currents are close to a sinusoidal waveform, and FC voltages of A and B phases are balanced well, as shown in Figure 27c,d.

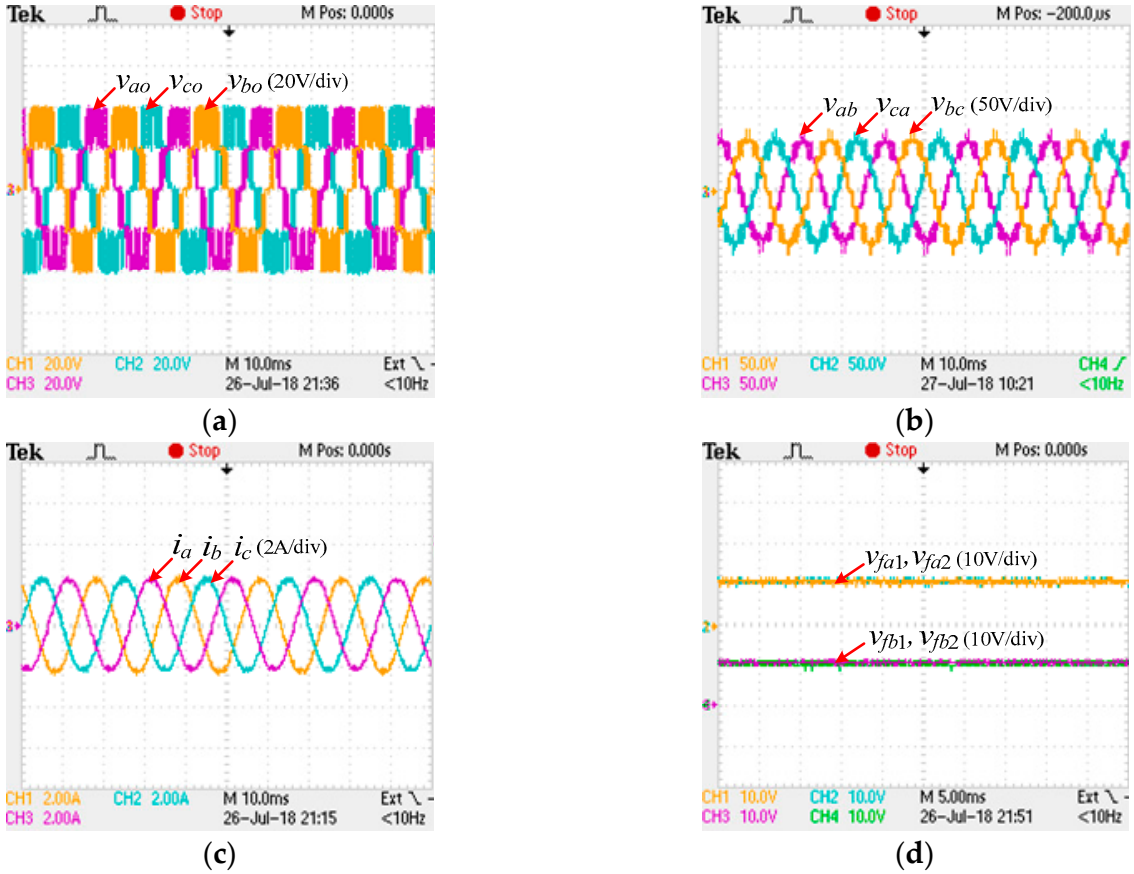


Figure 27. Steady-state experiment results of three-phase 5L hybrid T-ANPC converter with *RL*-load (m = 0.9 and f_c = 2 kHz). (**a**) Phase voltages, (**b**) line-to-line voltages, (**c**) load currents, (**d**) FC voltages of A and B phases.

6.2. Seven-Level Hybrid T-ANPC Converter

If the FC voltages v_{fx1}, v_{fx2} are controlled at $V_{dc}/6$, the hybrid T-ANPC converter will generate seven levels, as shown in Table 7. The voltage balance of the FCs can also be achieved by selecting redundant switching states while the NP voltage is balanced by using the zero-sequence voltage injection. The experiment results of 7L hybrid T-ANPC converter are shown in Figure 28, where the phase voltage and line-to-line voltages are 7 levels and 13 levels, respectively. The FC voltages of A and B phases are balanced and maintained at their desired value, with some HF switching harmonics are observed. Figure 29 shows the experiment results of dc-link capacitor voltages for 5L and 7L hybrid T-ANPC converter. It can be seen in Figure 29 that the capacitor voltages of two converters are both balanced well. The above experiment results verify the effectiveness of the control strategies for the hybrid T-ANPC converters.

The power quality of output waveforms is evaluated for the hybrid T-ANPC converter. Figure 30a,b show FFT spectra of the phase current i_a for 5L and 7L hybrid T-ANPC converters, respectively. As shown in Figure 30, the hybrid T-ANPC converter with two FC voltage ratings has low total harmonic distortion (THD) as 3.64% and 3.13%, respectively.

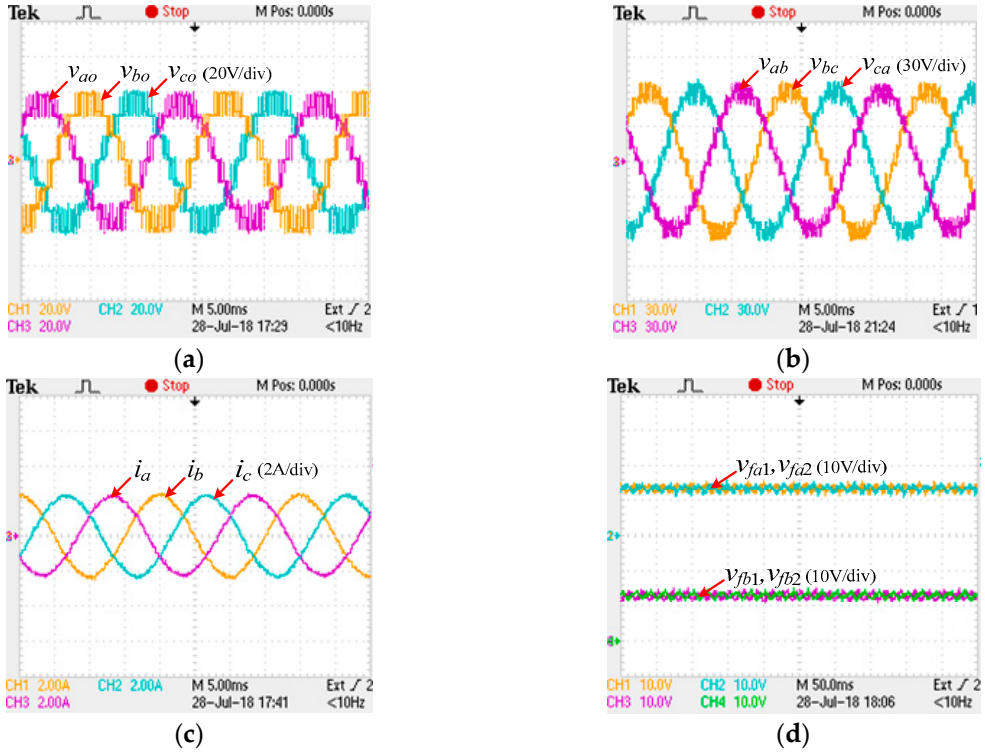


Figure 28. Experiment results of three-phase 7L hybrid T-ANPC converter with *RL*-load (m = 0.9 and f_c = 2 kHz). (**a**) Phase voltages, (**b**) line-to-line voltages, (**c**) load currents, (**d**) FC voltages of A and B phases.

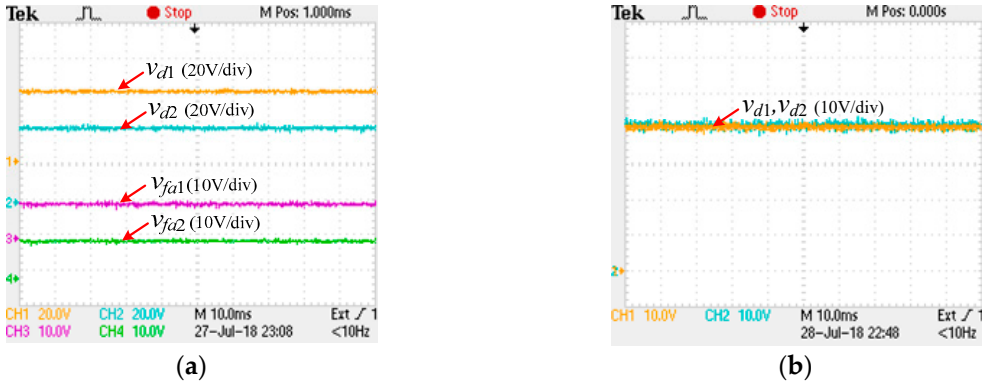


Figure 29. Experiment results of dc-link capacitor voltages for (**a**) 5L hybrid T-ANPC converter, (**b**) 7L hybrid T-ANPC converter.

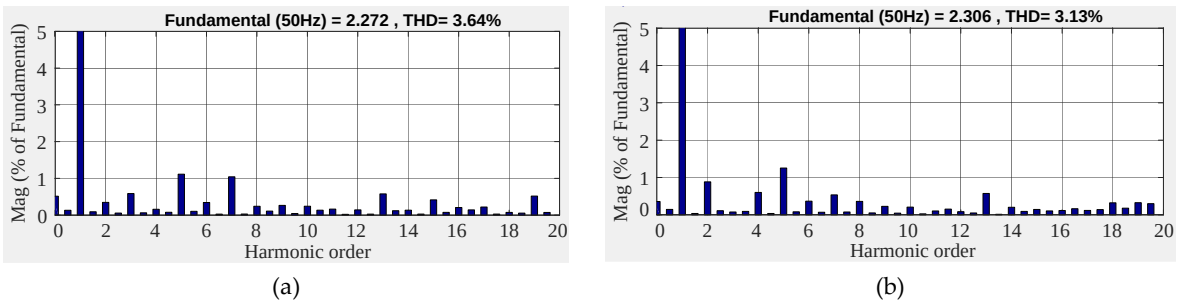


Figure 30. FFT spectrums of phase current i_a for (**a**) 5L hybrid T-ANPC converter, (**b**) 7L hybrid T-ANPC converter.

6.3. Nine-Level Hybrid Stacked Multicell Converter

To verify the modulation and control strategy of the HSM converter shown in Figure 26, a low-scale experimental platform based on single-phase 9L HSM converter with two T-type cells is constructed where the dc source voltage V_{dc} is 50 V and the reference voltage of FCs C_{f1}, and C_{f2} is set as $V_{dc}/4$. The ac side output terminals X_1 and X_2 are series connected with a resistor load through a filtering inductor (L = 4.3 mH, R = 15 Ω). A finite control-set MPC approach is developed for this 9L HSM converter to balance FC voltages and maintain desired outputs, and then no PWM modulator and the linear regulator is required. Thus the control complexity is simplified.

Figure 31 shows steady-state experiment results of 9L HSM converter with the MPC strategy. Figure 31a shows the switching signal S_1 of T_1 is same with fundamental frequency (50 Hz) while S_{11}, S_{12}, and S_{21} of switches T_{11}, T_{12}, and T_{21} in HF cells are in high frequency. Figure 31b shows the output voltage v_{ao} between terminal X_1 and o. The phase voltage v_{ao} and load current i_a are shown in Figure 31c. Figure 31d shows the voltage deviations Δv_{f1} and Δv_{f2} of FCs ($\Delta v_{f1} = v_{f1} - V_{dc}/4$; $\Delta v_{f2} = v_{f2} - V_{dc}/4$), phase current and its reference signal. It can be seen in Figure 31d that the voltage derivations and current tracking error are quite small and only high-frequency components are observed. Therefore, good steady-state performances of the MPC for 9L HSM converter are verified by the experiment results. Figure 32 shows the transient state experiment results of 9L HSM converter with linear *RL*-load. Figure 32a shows experiment results with the output frequency f_{out} changing from 50 Hz to 100 Hz. It can be seen that the desired phase voltage and load current are obtained well, and no voltage spikes are observed in the FC voltage even during transient process. As can be seen in Figure 32b, the capacitor voltages can be able to maintain balance with a slope increase of V_{dc} from 0 to 50 V.

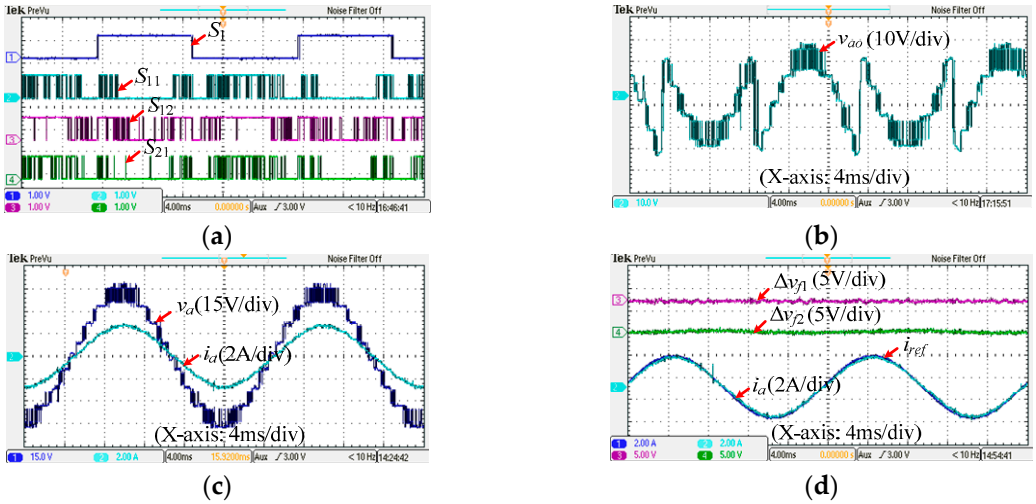


Figure 31. Steady-state experiment results of single-phase 9L HSM converter connected with linear *RL*-load. (**a**) Switching signals, (**b**) Output voltage v_{ao} between X_1 and o, (**c**) phase voltage v_a and load current i_a, (**d**) deviations of FC voltages and load current.

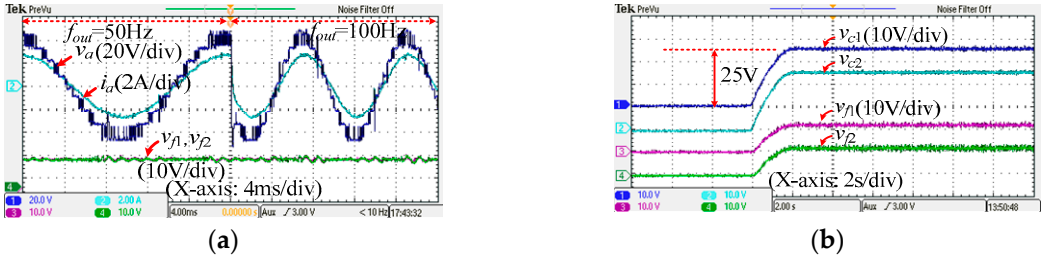


Figure 32. Transient-state experiment results of single-phase 9L HSM converter connected with linear *RL*-load. (**a**) Phase voltage v_{ao} and load current i_a, (**b**) dc-link capacitor voltages v_{c1}, v_{c2} and FC voltages v_{f1}, v_{f2}.

7. Conclusions

The topologies and evolutions of HMCs are studied in this paper. Five derivation methods are proposed to form hybrid topologies by using basic cells in series-parallel/parallel -series and adding/canceling devices. Some general topologies that are used to generate higher levels are also deduced. Then most of existing HMCs can be derived, and further new HMC topologies might be inspired that are applicable to specific emerging areas in the future years. The comparisons and evaluations of some typical HMCs are investigated, in terms of required devices, standing voltages of switches, stored energies of FCs and topology characteristics. The modulation techniques and control strategies of the HMCs are reviewed, and the balance capability of the NP voltage and FC voltage are investigated. Finally, the operation principle of hybrid T-ANPC converters and 9L HSMC are demonstrated and experimentally validated. Experimental results verify the effectiveness of the control strategies.

Author Contributions: J.Z. conceived and designed the study; S.X. preformed experiments and edited the draft with guidance from J.Z.; Z.D. checked the language of manuscript. J.Z. and X.H. made a significant contribution to the revisions of manuscript.

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