High-Efficiency Design and Control of Zeta Inverter for Single-Phase Grid-Connected Applications

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Abstract: The conventional zeta inverter has been used for single-phase grid-connected applications. However, it has high switching losses to operate at high switching frequency in the continuous conduction mode (CCM). To address this drawback, this paper suggests a high-efficiency zeta inverter using active clamp and synchronous rectification techniques. The proposed inverter utilizes the active clamp circuit for reducing switching losses. The non-complementary switching scheme is adopted for not only clamping the switch voltage stresses, but also alleviating the circulating energy. In addition, the synchronous rectification is implemented for reducing the body diode conduction of power switches. By using the silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs), the switching performance of the proposed inverter is improved. Its operation principle and control strategy are presented. A 220-W prototype has been designed and tested to evaluate the performance of the proposed inverter.

Keywords: zeta inverter; active clamp; synchronous rectification; power efficiency

1. Introduction

With the fast growth of renewable energy markets, many single-stage isolated inverters have been developed for single-phase grid-connected applications [1–9]. Among them, the zeta inverter [7–9] has been gaining attention due to the advantages of its low grid current ripple and low circuit component count, compared to other single-stage inverters such as flyback inverters [1–4] and Cuk inverters [5,6]. Of course, although the zeta inverter has large current ripples at the dc side, similar to the flyback inverter, it has been widely adopted for single-phase photovoltaic applications [7–9] due to its simple and flexible circuitry.

As the zeta inverter operates at a constant switching frequency, it has two operation modes: discontinuous conduction mode (DCM) and continuous conduction mode (CCM). The DCM zeta inverter has been used for low-power applications [7]. The grid current is easily controlled, as its control transfer function for the grid current is linear in DCM [8]. However, as the power level increases, the DCM zeta inverter suffers from high conduction losses. The DCM zeta inverters need to be connected in parallel to alleviate conduction losses.

When the zeta inverter operates in CCM, it can withstand a higher power level than the DCM zeta inverter. The CCM zeta inverter has been suggested in [9]. Figure 1 shows its circuit diagram, which is equivalent to the circuit diagram in [9]. It consists of the primary circuit \( (S_{P1}, L_m, L_{lk}) \) and the secondary circuit \( (C_S, S_{S1} \sim S_{S4}, L_g) \). \( T \) is a high-frequency transformer, which has the magnetizing inductor \( L_m \) and the leakage inductor \( L_{lk} \). The CCM zeta inverter has achieved higher efficiency than the DCM zeta inverter by lowering conduction losses [9]. However, the CCM zeta inverter suffers from high switching losses. In the primary circuit, the switch \( S_{P1} \) operates at a high switching frequency to regulate the grid current \( i_g \). When \( S_{P1} \) is turned off, a high voltage spike is generated due to the energy stored in the leakage inductor \( L_{lk} \), which increases switching losses [10].
The secondary circuit provides the current path to fold the grid voltage \( v_g \) and gives the freewheeling path for the grid current \( i_g \). The switches \( S_{S1} \sim S_{S4} \) operate at grid frequency according to the polarity of \( v_g \). \( S_{S2} \) and \( S_{S3} \) are always turned on for the positive grid cycle, while \( S_{S1} \) and \( S_{S4} \) are always turned on for the negative grid cycle. For the positive grid cycle, when \( S_{P1} \) is turned on, \( i_g \) flows through \( S_{S2} \) and \( S_{S3} \). As \( S_{P1} \) is turned off, \( i_g \) flows through \( S_{S2}, S_{S3}, D_{S1}, \) and \( D_{S4} \). \( D_{S1} \) and \( D_{S4} \) are the body diodes, which are turned on for the freewheeling of \( i_g \). However, when \( S_{P1} \) is turned on again, \( D_{S1} \) and \( D_{S4} \) are not turned off instantly due to the slow reverse recovery process [11]. The reverse recovery currents of \( D_{S1} \) and \( D_{S4} \) cause high voltage spikes across \( D_{S1} \) and \( D_{S4} \). They are also transferred to the primary circuit, which increases the turn-on switching losses of \( S_{P1} \). It is worse when high-voltage silicon (Si) metal oxide semiconductor field effect transistors (MOSFETs) are adopted, because their body diodes have poor reverse recovery characteristics. These drawbacks limit the practical use of the CCM zeta inverter, despite its advantages.

This paper proposes a high-efficiency zeta inverter to cope with the above-mentioned drawbacks. Figure 2 shows the circuit diagram of the proposed inverter. The active clamp circuit has been used for reducing switching losses in the primary circuit. The active clamp circuit has the auxiliary switch \( S_{P2} \) and the clamp capacitor \( C_p \). Conventionally, the auxiliary switch \( S_{P2} \) operates complementary to the main switch \( S_{P1} \) [12]. As the energy stored in \( L_k \) is absorbed in \( C_p \), the switch voltages are clamped to a constant voltage. However, this conventional method increases the circulating current in the primary circuit. It causes additional power losses due to high circulating energy. To address this drawback, the non-complementary switching scheme [13] has been adopted. In the non-complementary method, \( S_{P2} \) is turned on for a short time before \( S_{P1} \) is turned on. As the leakage energy is recycled with reduced circulating current, power losses associated with the circulating energy can be minimized in the proposed inverter.

![Figure 1. Circuit diagram of the zeta inverter.](image1)

![Figure 2. Circuit diagram of the proposed inverter.](image2)
In the secondary circuit, the synchronous rectification [14] is used for reducing the body diode conduction of MOSFETs. With synchronous rectification, \( S_{S1} (S_{S2}) \) and \( S_{S4} (S_{S3}) \) are turned on for the positive (negative) grid cycle when \( S_{P1} \) is turned off. It allows \( i_g \) to freewheel through the MOSFET channels instead of the body diodes. It avoids the body diode conduction, increasing the power efficiency, because the voltage drop across the on-state resistance of the MOSFET is lower than the forward voltage drop of the body diode [15]. The silicon carbide (SiC) MOSFET has been utilized for the synchronous rectification of \( S_{S1} \sim S_{S4} \). Due to the advantages over Si MOSFETs such as wider bandgap and higher electric field capacity [16], it improves the switching performance of the proposed inverter.

This paper is organized as follows. Section 2 describes the operation principle of the proposed inverter in the steady-state condition, along with the analysis of active clamp and synchronous rectification techniques. It also describes the control strategy for the CCM operation of the proposed inverter. Section 3 discusses the experimental results to verify the performance of the proposed inverter. Section 4 presents the conclusion of this paper.

2. Proposed Inverter

2.1. Operation Principle

Figure 3 shows the circuit diagram of the proposed inverter, which shows the reference directions of currents and voltages. The proposed inverter consists of the primary circuit (\( S_{P1}, S_{P2}, C_p, L_m, L_{lk} \)) and the secondary circuit (\( C_s, S_{S1} \sim S_{S4}, L_g \)). The active clamp circuit consists of \( S_{SP2} \) and \( C_p \). \( T \) is a high-frequency transformer, which has the magnetizing inductor \( L_m \) and the leakage inductor \( L_{lk} \). It is assumed that \( L_m \gg L_{lk} \). Its turns ratio \( n \) is \( N_S / N_P \). \( N_P \) is the primary winding turns. \( N_S \) is the secondary winding turns. All of the power switches are considered ideal except for their body diodes. \( V_d \) is the dc input voltage. \( v_g \) is the grid voltage. \( L_m \) and \( L_g \) are large enough so that the currents \( i_{Lm} \) and \( i_g \) are continuous during one switching period \( T_s \), respectively. \( C_p \) and \( C_s \) are large enough so that the voltages \( V_{Cp} \) and \( V_{Cs} \) are constant during \( T_s \), respectively. \( V_{Cs} \) is considered as \( |v_g| \) because the secondary circuit provides the current path to fold \( v_g \).

![Figure 3. Circuit diagram of the proposed inverter with reference directions of currents and voltages.](image)

Figure 4 shows the switching circuit diagrams of the proposed inverter during \( T_s \) for the positive grid cycle. Figure 5 shows the switching waveform diagrams of the proposed inverter during \( T_s \) for the positive grid cycle. \( V_{gate,P1} \) and \( V_{gate,P2} \) are the gate signals for \( S_{P1} \) and \( S_{P2} \), respectively. \( V_{gate,S1} \sim V_{gate,S4} \) are the gate signals for \( S_{S1} \sim S_{S4} \), respectively. \( S_{P1} \) and \( S_{P2} \) operate with a constant high switching frequency \( f_s \) (\( \approx 1/T_s \)). \( S_{P2} \) is turned on for a short time before \( S_{P1} \) is turned on. For the positive grid cycle, \( S_{S2} \) and \( S_{S3} \) are always turned on. \( S_{S1} \) and \( S_{S4} \) operate complementary to \( S_{P1} \). The proposed inverter has four switching modes during \( T_s \) for the positive grid cycle, which are outlined below.
Figure 4. Switching circuit diagrams of the proposed inverter during $T_s$ for the positive grid cycle: (a) Mode 1; (b) Mode 2; (c) Mode 3; and (d) Mode 4.
Figure 5. Switching waveform diagrams of the proposed inverter during $T_s$ for the positive grid cycle.

Mode 1 [$t_0$–$t_1$]: At $t = t_0$, $S_{P1}$ is turned on. $L_m$ and $L_{lk}$ store the energy from $V_d$. $i_{Lm}$ increases linearly at the rate of $\frac{di_{Lm}}{dt} = \frac{V_d}{(L_m + L_{lk})}$. The voltage across the secondary winding of $T$ is $\frac{nL_mV_d}{(L_m + L_{lk})}$. $i_g$ increases linearly at the rate of $\frac{di_g}{dt} = \frac{nL_mV_d}{(L_m + L_{lk})} / L_g$.

Mode 2 [$t_1$–$t_2$]: At $t = t_1$, $D_{P2}$ is turned on as $S_{P1}$ is turned off. The energy stored in $L_{lk}$ is stored in $C_P$. The switch voltage $V_{P1}$ is clamped to $V_{Cp}$. $S_{S1}$ and $S_{S4}$ are turned on in this mode. As the voltage
across the secondary winding of $T$ is $v_g$, $i_{Lm}$ decreases linearly at the rate of $di_{Lm}/dt = -v_g / nL_m$. As $i_g$ freewheels through $S_{S1} - S_{S4}$, $i_g$ decreases linearly at the rate of $di_g / dt = -v_g / L_g$.

Mode 3 [$t_2$-$t_3$]: At $t = t_2$, $D_{P2}$ is turned off as $i_{Cp}$ becomes zero. The switch voltage $V_{P1}$ is clamped to $V_d + v_g / n$. The switch voltage $V_{P2}$ is clamped to $V_{Cp} + V_d + v_g / n$. $i_{Lm}$ and $i_g$ keep decreasing linearly as in Mode 2.

Mode 4 [$t_3$-$t_4$]: At $t = t_3$, $S_{P2}$ is turned on for transferring the energy stored in $C_p$ to the grid. The absorbed leakage energy is recycled to the grid. The switch voltage $V_{P1}$ is clamped to $V_{Cp}$. $i_{Lm}$ and $i_g$ keep decreasing linearly as in Mode 2.

From Mode 2 to Mode 4, the following current relations are obtained as $i_{Cg} = -i_{S1} - i_{S3} = -i_{S2} - i_{S4}$ and $i_g = i_{S2} - i_{S1} = i_{S4} - i_{S3}$ with respect to the nodes $P$, $N$, $A$, and $B$. Next, the switching cycle begins as $S_{P1}$ is turned on, and $S_{P2}$, $S_{S1}$, and $S_{S4}$ are turned off. For the negative grid cycle, $S_{S1}$ and $S_{S4}$ are always turned on. $S_{S2}$ and $S_{S3}$ operate complementary to $S_{P1}$. The operation principle for the negative grid cycle is not described here, because it can be explained analogously as the operation principle for the positive grid cycle.

### 2.2. Active Clamp Circuit

In the active clamp circuit, $S_{P2}$ is turned on for a short period before $S_{P1}$ is turned on. The absorbed leakage energy is recycled as the energy stored in $C_p$ is transferred to the grid. Figure 6 shows the detailed timing diagrams for $V_{g_{ate,P1}}$, $V_{g_{ate,P2}}$, and $i_{Cp}$. $T_{ON}$ is the turn-on time of $S_{P1}$. $T_{OFF}$ is the turn-off time of $S_{P1}$. $T_{DP2}$ is the turn-on time of $D_{P2}$. $T_{SP2}$ is the turn-on time of $S_{P2}$. As $S_{P2}$ is turned on, the capacitor current $i_{Cp}$ can be represented as:

$$i_{Cp}(t) = -\frac{V_{Cp} - V_d - |v_g|/n}{L_{ik}} t. \tag{1}$$

![Figure 6. Detailed timing diagrams for $V_{g_{ate,P1}}$, $V_{g_{ate,P2}}$, and $i_{Cp}$.](image)

By the charge balance for the capacitor $C_p$ during $T_s$, the areas A and B for two current waveforms should be equal to:

$$\frac{1}{2} i_{P1,pk} T_{SP2} = V_{Cp} - V_d - |v_g|/n T_{DP2} \tag{2}$$

where $i_{P1,pk}$ is the peak value of $i_{P1}$. Supposing that $T_{DP2} = T_{SP2}$, the capacitor voltage $V_{Cp}$ is represented as:

$$V_{Cp} = V_d + \frac{|v_g|}{n} + \frac{L_{ik} i_{P1,pk}}{T_{SP2}}. \tag{3}$$
Also, the circulating energy $E_{Cir}$ during $T_{SP2}$ is represented as:

$$E_{Cir} = \frac{(V_{CP} - V_d - |v_g|/n)^2}{2L_{lk}}T_{SP2}.$$  \hspace{1cm} (4)

The circulating energy $E_{Cir}$ will be smaller as $T_{SP2}$ is getting shorter. However, in the active clamp method using the complementary switching scheme [12], the circulating energy is related with the turn-off time $T_{OFF}$, which is much longer than $T_{SP2}$. Thus, the non-complementary switching scheme results in higher power efficiency by reducing the circulating energy.

2.3. Synchronous Rectification with SiC MOSFETs

Figure 7 shows the detailed switching circuit diagrams for the operation principle of the secondary circuit for the positive grid cycle. Figure 7a shows the switching circuit diagram of the secondary circuit in the previous inverter in Figure 1. $i_g$ freewheels through the body diodes $D_{S1}$ and $D_{S4}$ when $S_{P1}$ is turned off. When $S_{P1}$ is turned on, $D_{S1}$ and $D_{S4}$ are not turned off immediately because of the slow reverse recovery process [11]. Then, the diode reverse recovery currents cause high voltage spikes across $D_{S1}$ and $D_{S4}$. Also, the diode reverse recovery currents are transferred to the primary circuit through the transformer, which causes high current spikes for $S_{P1}$. On the other hand, Figure 7b shows the switching circuit diagram of the secondary circuit in the proposed inverter. When $S_{P1}$ is turned off, $S_{S1}$ and $S_{S4}$ are turned on. $i_g$ freewheels through the MOSFET channels instead of the body diodes, which minimizes the conduction of the body diodes. When $S_{P1}$ is turned on again, $S_{S1}$ and $S_{S4}$ are turned off without the reverse recovery process of the body diodes.

![Figure 7](image_url)

**Figure 7.** Detailed switching circuit diagrams for the operation principle of the secondary circuit for the positive grid cycle: (a) previous inverter; and (b) proposed inverter.

When $S_{S1}$ and $S_{S4}$ are turned off, the voltage across the secondary winding of $T$ is $nL_mV_d/(L_m + L_{lk})$. The switch voltage stresses $V_{S1}$ and $V_{S4}$ are represented as:

$$V_{S1} = V_{S4} = \left|v_g\right| + \frac{nL_mV_d}{L_m + L_{lk}}.$$  \hspace{1cm} (5)

The switch voltage stresses $V_{S2}$ and $V_{S3}$ are identical to $V_{S1}$ and $V_{S4}$ in Equation (5). Suppose that the system parameters are given as $V_d = 48 \text{ V}$, $n = 4.5$, and $v_g = 220 \text{ Vrms}$ with negligible leakage inductor. The switch voltage stress is approximately calculated as 527 V without considering any voltage oscillations. Practically, the use of high voltage (>700 V) MOSFETs is inevitable to withstand the switch voltage stresses for a high switching frequency. However, when Si MOSFETs are adopted for $S_{S1} \sim S_{S4}$, the proposed inverter will suffer from high conduction losses due to the high on-state resistances of Si MOSFETs. Thus, the SiC MOSFET is an attractive alternative to the Si MOSFET for high-frequency and high-voltage applications. Due to its advantages over Si MOSFETs such as
its wider bandgap and higher electric field capacity, it improves the switching performance of the proposed inverter, increasing the power efficiency.

2.4. Control Strategy

Supposing that the leakage inductor is negligible, the volt-second balance for \( L_g \) during \( T_s \) gives the following voltage equation as:

\[
\frac{V_d}{D} n = \frac{v_g}{1 - D} (1 - D) T_s = 0
\]

where \( D \) is the duty cycle of \( S_{P1} \). By rearranging Equation (6), we have the relation between \( v_g \) and \( V_d \) as:

\[
\frac{v_g}{V_d} = n \frac{D}{1 - D} \tag{7}
\]

Assuming no power losses in the inverter circuit, we have the relation between \( i_d \) and \( i_g \) as:

\[
\frac{i_d}{i_g} = n \frac{D}{1 - D} \tag{8}
\]

where \( i_d \) is the input current. Suppose that \( C_p \) keeps the charge balance, \( i_d \) is considered as \( i_{P1} \) during \( T_s \). Then, the following current relations are represented as:

\[
i_d = i_{P1} = k D i_{Lm} \tag{9}
\]

where \( k \) is a proportional factor. From equations (8) and (9), we have the relation between \( i_{Lm} \) and \( i_g \) as:

\[
i_{Lm} = \frac{n}{k(1 - D)} i_g \tag{10}
\]

The average voltage for \( L_m \) during \( T_s \) can be represented with respect to the deviation \( \Delta i_{Lm} \) of \( i_{Lm} \) as:

\[
V_d D - \frac{|v_g| n}{V_d} (1 - D) = \frac{\Delta i_{Lm}}{T_s} \tag{11}
\]

From Equation (11), \( D \) can be represented as:

\[
D = \frac{|v_g|}{|v_g| + n V_d} + \frac{n}{|v_g| + n V_d} \left( \frac{L_m \Delta i_{Lm}}{T_s} \right) \tag{12}
\]

By using equations (7) and (10), \( D \) in Equation (12) can be written as:

\[
D = D_n + D_c = \frac{|v_g|}{|v_g| + n V_d} + \frac{n L_m}{k V_d T_s} \Delta i_g \tag{13}
\]

where \( D_n \) is the nominal duty cycle, and \( D_c \) is the control duty cycle as:

\[
D_n = \frac{|v_g|}{|v_g| + n V_d} = \frac{V_g |\sin \omega t|}{V_g |\sin \omega t| + n V_d}, \tag{14}
\]

\[
D_c = \frac{n L_m}{k V_d T_s} \Delta i_g.
\]

\( V_g \) is the absolute peak value of \( v_g \). \( \omega \) is the angular frequency of \( v_g \). Supposing that \( v_g \) is measured exactly with a phase-locked loop (PLL) \[17\], \( D_n \) plays the role of providing the nominal voltage compensation. By using \( D_n \), the non-linear system in Equation (11) is transformed to the first-order linear system, which can be controlled by the control duty cycle \( D_c \). In order to regulate
the grid current \( i_g \) with low harmonic currents, \( D_c \) is implemented by a proportional-resonant (PR) control [18] whose ideal transfer function \( C_{PR}(s) \) is:

\[
C_{PR}(s) = k_p + \frac{k_r s}{s^2 + \omega_c^2}
\]

(15)

where \( k_p \) and \( k_r \) are the PR control gains, respectively. However, it is unable to realize the PR controller in Equation (15) with an infinite gain. Thus, the following non-ideal transfer function is adopted in practice as:

\[
C_{PR}(s) = k_p + \frac{2k_r \omega_c s}{s^2 + 2\omega_c s + \omega_c^2}
\]

(16)

where \( \omega_c \) is the angular frequency at the cutoff frequency of the controller. In addition, the harmonic compensators can be added to the PR controller to minimize the harmonic currents for the selective harmonic frequencies [19]. Its transfer function \( C_{HC}(s) \) is expressed as:

\[
C_{HC}(s) = \sum_{h=3,5,7} \frac{2k_{rh} \omega_c s}{s^2 + 2\omega_c s + (h\omega_c)^2}
\]

(17)

where \( h \) is the harmonic order and \( k_{rh} \) is the resonant control gain for each harmonic frequency. Since the third, fifth, and seventh harmonics are significant under the grid environment, the third to seventh harmonic compensators are implemented. The harmonic compensators provide high gains at the selected harmonic frequencies, helping minimize the steady-state error and the disturbance by the selected frequency components. Figure 8 shows the control block diagram of the proposed inverter. \( I_{g}^* \) is the peak magnitude of the current reference \( i_g^* \). The duty cycle \( D \) is generated by summing \( D_n \) and \( D_c \).

![Figure 8. Control block diagram of the proposed inverter.](image)

3. Experimental Results

A 220-W prototype system has been designed and tested to evaluate the performance of the proposed inverter. Table 1 shows the system parameters and the circuit components. As a SiC MOSFET, UJC1206k (UnitedSiC) has been used for \( S_{51} \sim S_{54} \). As a digital signal controller, dsPIC30F6015 (Microchip) has been used for implementing the current controller and generating the duty cycle signals for all of the power switches. Figure 9 shows the picture of the prototype system. The prototype system includes the power circuit and the control circuit. Even though it is not optimized for the commercialized level, it is expected that the proposed inverter could achieve high power density if it is implemented with advanced devices such as gallium nitride (GaN) devices [20] and planar transformers [21].
Table 1. System parameters and circuit components.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Quantity</th>
<th>Value</th>
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<tbody>
<tr>
<td>$V_d$</td>
<td>dc input voltage</td>
<td>48 V</td>
</tr>
<tr>
<td>$v_g$</td>
<td>grid voltage</td>
<td>60 Hz/220 Vrms</td>
</tr>
<tr>
<td>$f_s$</td>
<td>switching frequency</td>
<td>50 kHz</td>
</tr>
<tr>
<td>$L_m$</td>
<td>magnetizing inductor</td>
<td>60 µH</td>
</tr>
<tr>
<td>$L_{lk}$</td>
<td>leakage inductor</td>
<td>0.5 µH</td>
</tr>
<tr>
<td>$N_p$</td>
<td>primary winding turns</td>
<td>14</td>
</tr>
<tr>
<td>$N_s$</td>
<td>secondary winding turns</td>
<td>63</td>
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<tr>
<td>$C_p$</td>
<td>clamp capacitor</td>
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</tr>
<tr>
<td>$S_{P1}, S_{P2}$</td>
<td>primary switches</td>
<td>IXFK150N30P3</td>
</tr>
<tr>
<td>$C_s$</td>
<td>secondary capacitor</td>
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</tr>
<tr>
<td>$S_{S1} \sim S_{S4}$</td>
<td>secondary switches</td>
<td>UJC1206K</td>
</tr>
<tr>
<td>$L_g$</td>
<td>filter inductor</td>
<td>2.0 mH</td>
</tr>
</tbody>
</table>

Figure 9. Picture of the prototype system.

The proposed inverter has been simulated to verify its operation principle. It has been simulated by the physical security information management (PSIM) software for the system parameters in Table 1. Figure 10 shows the simulation waveforms of the proposed inverter. The steady state operation of the proposed inverter can be verified from Figure 10a-d. Figure 10e,f show the simulation waveforms of the proposed inverter in the transient state condition. Figure 10e shows $v_g$ and $i_g$ as the output power changes from 110 W to 220 W. Figure 10f shows $v_g$ and $i_g$ as the output power changes from 220 W to 110 W.

Figure 11 shows the experimental waveforms of the previous inverter in Figure 1. The previous inverter has been designed and tested for the same system parameters as the proposed inverter. It uses the same circuit components in Table 1, except that STW40N95K5 (STMicroelectronics), as a Si MOSFET, has been adopted for $S_{S1} \sim S_{S4}$. Figure 11a shows the gate signal $V_{gate,P1}$ and the switch voltage $V_{P1}$ for $S_{P1}$. When $S_{P1}$ is turned off, $V_{P1}$ has a high voltage spike, which results from the energy stored in the transformer leakage inductor. Figure 11b shows the gate signal $V_{gate,P1}$ and the switch current $i_{P1}$ for $S_{P1}$. When $S_{P1}$ is turned on, $i_{P1}$ has a high current spike, which results from the reverse recovery current of the body diodes in the secondary circuit.
Figure 10. Simulation waveforms: (a) $V_{gate,P1}$, $V_{gate,P2}$, $V_{P1}$, and $V_{P2}$; (b) $V_{gate,P1}$, $V_{gate,P2}$, $i_{P1}$, and $i_{P2}$; (c) $i_{g}$, $i_{S2}$, and $i_{S3}$; (d) $i_{g}$, $i_{S1}$, and $i_{S4}$; (e) $v_{g}$ and $i_{g}$ from 110 W to 220 W; and (f) $v_{g}$ and $i_{g}$ from 220 W to 110 W.

Figure 11. Experimental waveforms of the previous inverter: (a) $V_{gate,P1}$ and $V_{P1}$; and (b) $V_{gate,P1}$ and $i_{P1}$.

Figure 12 shows the experimental waveforms of the proposed inverter. Figure 12a shows $V_{gate,P1}$, $V_{gate,P2}$, and $V_{P1}$. Figure 12b shows $V_{gate,P1}$, $V_{gate,P2}$, and $V_{P2}$. As shown in Figure 12a,b, $V_{P1}$ and
$V_{P2}$ are maximally clamped to the capacitor voltage $V_{Cp}$. Figure 12c shows $V_{gate,P1}$, $V_{gate,P2}$, and $i_{P1}$. The switch current $i_{P1}$ in Figure 12c has lower current spike than the switch current $i_{P1}$ in Figure 11b because of the synchronous rectification of the secondary circuit. Figure 12d shows $V_{gate,P1}$, $V_{gate,P2}$, and $i_{Cp}$. It is observed that the capacitor charging and discharging currents are well balanced in the proposed inverter.

![Figure 12](image)

**Figure 12.** Experimental waveforms of the proposed inverter: (a) $V_{gate,P1}$, $V_{gate,P2}$, and $V_{P1}$; (b) $V_{gate,P1}$, $V_{gate,P2}$, and $V_{P2}$; (c) $V_{gate,P1}$, $V_{gate,P2}$, and $i_{P1}$; and (d) $V_{gate,P1}$, $V_{gate,P2}$, and $i_{Cp}$.

Figure 13 shows the experimental waveforms in the secondary circuit for the positive grid cycle. Figure 13a shows $V_{S1}$ in the previous inverter. It is observed that there is high voltage oscillation across $S_{S1}$, which results from the slow reverse recovery process of the body diode of the Si MOSFET. Figure 13b shows $V_{gate,S1}$ and $V_{S1}$ in the proposed inverter. With synchronous rectification, the SiC MOSFET channel has been used for the rectification. It is shown that voltage oscillation across $S_{S1}$ has been much alleviated due to the fast switching operation of the SiC MOSFET. The switch currents $i_{S1}$, $i_{S2}$, $i_{S3}$, and $i_{S4}$ are shown from Figure 13c–f with respect to $i_{g}$ in the proposed inverter.

Figure 14 shows the experimental waveforms of the proposed inverter. Figure 14a shows $v_{g}$ and $i_{g}$ as the proposed inverter supplies 110 W into the grid. Figure 14b shows $v_{g}$ and $i_{g}$ as the proposed inverter supplies 220 W into the grid. As $i_{g}$ is in phase with $v_{g}$, the power factor is measured as 0.99 in Figure 14.

Figure 15 shows the measured power efficiency curves. The curve A shows the measured power efficiency of the previous inverter. It has achieved the peak efficiency of 93.5% at the rated power. The curve B shows the measured power efficiency of the proposed inverter when the synchronous rectification has been implemented without the active clamp circuit. The proposed inverter has improved the power efficiency, achieving the peak efficiency of 94.2% at the rated power. The curve C shows the measured power efficiency of the proposed inverter when both active clamp and synchronous rectification techniques have been implemented. The proposed inverter has achieved the peak efficiency of 95.0% at the rated power by using active clamp and synchronous rectification techniques.
Figure 13. Experimental waveforms in the secondary circuit for the positive grid cycle: (a) $V_{S1}$ in the previous inverter; (b) $V_{gate,S1}$ and $V_{S1}$ in the proposed inverter; (c) $i_g$ and $i_{S2}$ in the proposed inverter; (d) $i_g$ and $i_{S3}$ in the proposed inverter; (e) $i_g$ and $i_{S1}$ in the proposed inverter; and (f) $i_g$ and $i_{S4}$ in the proposed inverter.

Figure 14. Experimental waveforms of the proposed inverter: (a) $v_g$ and $i_g$ as the proposed inverter supplies 110 W into the grid; and (b) $v_g$ and $i_g$ as the proposed inverter supplies 220 W into the grid.

Figure 15. Measured power efficiency curves.
Figure 16a shows the measured power efficiency curves up to 440 W. The prototype system has shown the peak efficiency of 95.0% at 220 W. The efficiency decreases gradually as the output power level goes up from 300 W to 440 W. The prototype system has achieved the efficiency of 94.3% at 440 W. Figure 16b shows the measured power efficiency curves for 50 kHz and 100 kHz, respectively. As the switching frequency increases, the power efficiency decreases because of the switching losses. In order to improve the power efficiency and the power density further, the circuit design scheme should be advanced by considering the GaN devices [20] and the planar transformers [21] for megahertz operations.

![Figure 16. Measured power efficiency curves: (a) power efficiency curves up to 440 W; and (b) power efficiency curves for different switching frequencies.](image)

4. Conclusions

This paper has proposed a high-efficiency zeta inverter using active clamp and synchronous rectification techniques for single-phase grid-connected applications. The operation principle of the proposed inverter has been described. The active clamp and synchronous techniques adopted in the proposed inverter have been explained. The non-complementary switching scheme has been applied to the active clamp circuit. It effectively reduces the switching losses and circulating current in the primary circuit. The synchronous rectification with SiC MOSFETs alleviates switching losses in the secondary circuit. The control strategy for the CCM operation of the proposed inverter has been presented. A 220-W prototype system has been designed and tested to evaluate the performance of the proposed inverter. Experimental results have shown that the proposed inverter has improved the power efficiency by reducing switching losses, compared to the previous inverter.

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**References**

